MODEL D3400
DUAL- AND QUAD-DISK DRIVES

MODEL NO. D3481

SERIAL NO. 1126057S2

MODEL D3400
DUAL- AND QUAD-DISK DRIVES

PERTEC COMPUTER CORPORATION
PERIPHERALS DIVISION

9600 IRONDALE AVENUE, CHATSWORTH, CA 91311

OPERATING AND SERVICE MANUAL NO. 108116

FOREWORD

This manual provides operating and service instructions for D3000 Series Disk Drives, Models D346X and D348X, manufactured by Pertec Computer Corporation, Peripherals Division (PCC PD), Chatsworth, California.

The content includes a detailed description, specifications, installation instructions, and checkout of the disk drive. Also included are theory of operation and preventive maintenance instructions. Section VII contains photo parts lists, a recommended spare parts list, and schematics.

All graphic symbols used in logic diagrams conform to the requirements of ANSI-Y32.14 and all symbols used in schematic diagrams are as specified in ANSI-Y32.2.

SERVICE AND WARRANTY

This Pertec Computer Corporation (PCC) product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PCC Peripherals Division or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

The Peripherals Division of PCC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PCC Peripherals Division agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PCC Peripherals Division and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list.

Contact your local PCC Service Division office for servicing and maintenance on all PCC equipment except flexible disk drives. Flexible disk drives must be returned to the Peripherals Division factory Repair Depot for servicing.

Please contact the following groups for assistance with your specific problem.

SERVICE DIVISION SUPPORT

For all servicing requirements on PCC Peripherals Division equipment, please contact your local PCC Service Division office. Additionally, the Service Division offers maintenance contracts, service contracts, third party maintenance contracts, etc.

PERIPHERALS DIVISION SUPPORT

NORTH AMERICA: 21111 Erwin Street, Woodland Hills, California 91367, (213) 999-2020

Our Woodland Hills facility is staffed to provide assistance in the following areas.

ORDER ADMINISTRATION

- For submitting your equipment orders.
- For obtaining delivery schedules on your equipment.
- For any other information on your orders. (Note also that your local sales office can answer these questions.)

TRAINING SUPPORT

- Contact the Training Coordinator for class schedules, for classes to be held at your facilities, or for having a customized training program developed.

SPARES SUPPORT

- Spares Order Administration for submitting your spare requests (except Emergency).
- Spares Logistics Administrators to answer any questions on spares (including assistance in determining part numbers).

NORTH AMERICA: 9600 Irondale Avenue, Chatsworth, California 91311, (213) 882-0030

Our Chatsworth facilities are staffed to provide assistance in the following areas.

REPAIR DEPOT

- For all questions related to equipment sent back or being sent back to the Repair Depot. This includes schedules, repair costs, or refurbishments.
- All equipment being returned for repair should be sent to PCC Peripherals Division Repair Depot, 20400 Plummer Street, Chatsworth, California, 91311.

TECHNICAL SUPPORT

- For equipment troubleshooting assistance.
- For applications information.
- For any other information or questions, or if you need assistance and you just don't know who to call.

EMERGENCY SPARES

- For spare parts that are required immediately.

EUROPE: 10 Portman Road, Reading, Berkshire RG3 1DU, England
Phone Reading (734) 582115 / TWX 847-101

Users of PCC Peripherals Division equipment in Europe should direct all inquiries on the subjects listed for North America to the Reading office.

Servicing of all PCC Peripherals Division equipment is coordinated through the Reading office, including U.S. OEMs that ship systems to Europe.

PACIFIC

Users of PCC Peripherals Division equipment in Australia, Japan, New Zealand, and South America should direct all inquiries on the subjects listed for North America to their local PCC representatives.

PROPRIETARY NOTICE

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the D3000 Series Disk Drive, Models D346X and D348X, manufactured by Pertec Computer Corporation, Peripherals Division (PCC PD), Chatsworth, California.

1.1.1 MODEL IDENTIFICATION

To simplify identification of D3000 Series Disk Drives, Figure 1-1 illustrates the breakdown of code combinations employed.

Referring to Figure 1-1, the following illustrates the ease of identification, using Model D3462-I064-CWU-(XXXXX) as an example.

(1) D3 is the basic prefix on all D3000 Series.

(2) 4 in the third position indicates 2200 bpi.

(3) 6 in the fourth position indicates a 5440-type cartridge plus 3 fixed disks are used.

(4) 2 in the fifth position indicates a spindle speed of 2400 rpm.

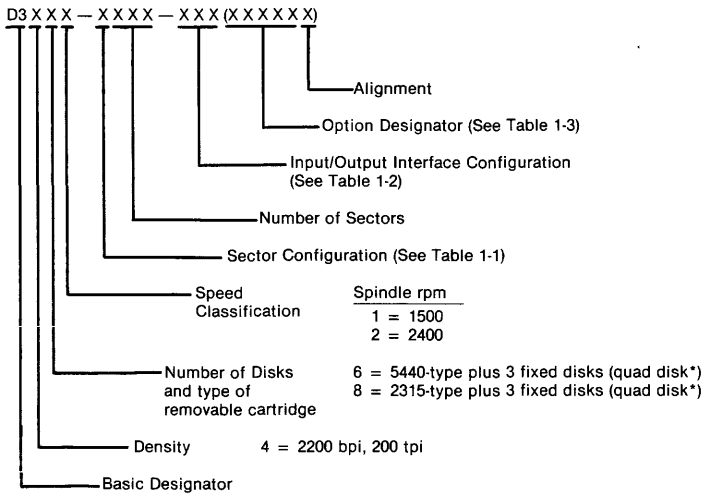
(5) I in the sixth position indicates that the 5440-type cartridge to be used has a normal index notch only.

(6) 064 in the seventh, eighth, and ninth positions indicates a 64-sector device.

(7) Letters in the tenth, eleventh and twelfth positions indicate a special input and output interface configuration.

(8) Letters appearing in the 13th thru 17th positions indicate the options, selected by the user, in Table 1-3.

(9) Letter in the eighteenth position indicates CE Alignment Track designation (see Table 1-3).



*Note that throughout this manual the words disk and platter are interchangeable.

Figure 1-1. Model Identification

Table 1-1
Sectoring Configuration

Type of Cartridge to be Utilized	Type of Sectoring to be Utilized	Applicable Configuration Designator
5440-type cartridge with normal index notch only	Electronic	IXXX
5440-type cartridge specially modified with sector and index notches	Electronic	EXXX
	Mechanical	MXXX
2315-type cartridge with normal sector and index slots	Electronic	EXXX
	Mechanical	MXXX

Table 1-2
Input/Output Interface Configuration Options

XXU	Indicates that in this model disk drive, the thumbwheel Unit Number Select Switch is active so that the drive can be assigned positions 1 thru 4, as desired.
XXS	Indicates that the disk drive is always selected and the Unit Number Select Switch is ignored.
XWX	Indicates that the disk drive incorporates the Write Protect function.
NXX	Indicates that no interface option is included.
SXX	Indicates a special interface.
XSC	Indicates a special disk configuration which requires reference to a specific order documentation for description and characteristics.

Table 1-3
Functional Options

CONFIGURATION DIGIT 1

	EXTENSION PLATTER SELECT		DUAL UNIT EMULATE		TERM V FEED THRU		LOGIC BOARD JUMPERS															
	I/O	Unit	1&2	3&4	Yes	No	W2	W3	W6	W10	W11	W12	W13	W14	W15	W18	W20	W22	W23	W24	W25	W26
A	X					X	X			X			X		X	X	X			X	X	X
B		X	X			X	X				X		X	X		X	X	X		X	X	X
C		X		X		X	X			X		X		X		X	X		X	X	X	X
D	X				X		X	X		X			X		X	X	X			X		
E		X	X		X		X	X			X		X	X		X	X	X		X		
F		X		X	X		X	X		X		X		X		X	X		X	X		
H																						
I																						
J																						
K																						
L																						
M																						
N		X	X	X		X	X				X	X		X		X	X	X	X	X	X	X
P		X	X	X	X		X	X			X	X		X		X	X	X	X	X		
Q																						
R																						

CONFIGURATION DIGIT 2

	MALFUNCTION SIGNAL SELECT GATED		SPECIAL INTERFACE			REMOTE START STOP GATED		LOGIC BOARD JUMPERS					
	Yes	No	None	Safe	Run	Yes	No	W1	W7	W8	W9	W16	W17
A	X		X				X					X	
B		X	X				X						X
C	X			X			X	X		X		X	
D		X		X			X	X		X			X
E	X				X		X	X			X	X	
F		X			X		X	X			X		X
H	X		X			X			X			X	
I		X	X			X			X				X
J	X			X		X		X	X	X		X	
K		X		X		X		X	X	X			X
L	X				X	X		X	X		X	X	
M		X			X	X		X	X		X		X

CONFIGURATION DIGIT 3

	GROUND ISOLATION		LOGIC BOARD JUMPERS	
	Yes	No	W4	W5
A		X		X
B	X		X	

1.2 PURPOSE OF EQUIPMENT

The disk drive has the capability of recording digital data on IBM 2315- or 5440-type cartridges utilizing the double frequency method of recording. Spindle speeds up to 2400 rpm and data storage of up to 203 megabits are provided by the D3000 Series Disk Drive. Data recorded on the removable media can be recovered when played back on any D3000 Series having the same cartridge type, density, format, and speed.

The D3000 is a rotating magnetic memory capable of storing and retrieving data in digital form. The storage media is an aluminum disk coated on both surfaces with a layer of ferro magnetic material suspended in a binder. Data are stored serially in concentric tracks on both surfaces of the disk.

The basic drive is available as a quad-disk or split-quad device. Where disk-drive space is at a premium, the quad-disk models can be configured electrically to act like two separate dual-disk drives sharing a common head positioning system; this is generally referred to as a split-quad disk drive. As many as four disk drives can be operated by a single controller. This is accomplished by a common Input/Output interface bus, sometimes referred to as a daisy-chain.

All models are capable of accepting removable media with the removable disk enclosed in a cartridge assembly. Depending on the model, the disk drive will accept either the top loading 5440-type or the front loading 2315-type cartridge. Quad-disk models have provisions for the removable cartridge and three fixed disks enclosed within the drives, enclosed within the drive housing.

The disk drive is intended for use in conjunction with a formatter or controller to provide rapid-access mass-memory for small and medium size computers.

An integral power supply is included in the disk drive and operates directly from single phase power.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The top loading configuration of the D3000 Disk Drive utilizes a 5440-type cartridge and is shown in Figure 1-2; the front loading configuration utilizes a 2315-type cartridge and is shown in Figure 1-3.

All electrical and mechanical components necessary to operate the disk drive are mounted within the drive housing. The housing is designed to be mounted in a standard 482.6 mm (19-inch) EIA rack.

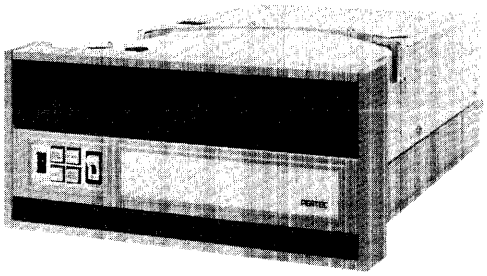


Figure 1-2. D3000 Disk Drive, Top Load Model

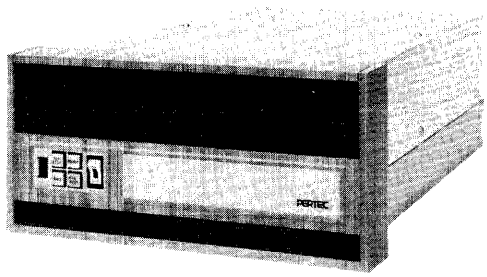


Figure 1-3. D3000 Disk Drive, Front Load Model

All models are equipped with the necessary electronics to provide recording and retrieval of stored data.

Access to the interior of the disk drive is gained by removing the dust cover. This cover is mounted to the base assembly and protects the interior of the drive from dust and other environmental contaminants.

The operational controls, which include indicators that are illuminated when the relevant functions are being performed, are mounted on the front control panel. These controls are accessible to the operator at all times. Power is supplied through a strain-relieved cord which has a standard 3-prong plug. Interface signals are routed through the interface cables to input/output connectors located within the drive housing.

The major electronic assemblies are located near the rear of the drive. These assemblies are mounted to allow ready access without the use of extender cards or other special tools.

1.4 FUNCTIONAL DESCRIPTION

Data storage is accomplished by utilizing the non-contact method of magnetic recording. The disk recording media is rotated at a constant speed and the recording heads, capable of either reading or writing, are flown over the surface of the disk on a gas film bearing and positioned to the appropriate track by the use of a voice-coil type of linear motor positioner. This type of disk drive, which utilizes a single head per surface, is referred to as a moving-head disk drive.

Addressing of the stored data is accomplished by specifying the desired head position and the applicable segment of the disk surface. The read/write electronics are capable of non-simultaneous reading or writing of data on a single surface at a given time.

Figure 1-4 is a functional block diagram of the disk drive, which consists of the disk drive control logic, start-and-stop control, and the necessary select and enable gating.

The positioner servo electronics comprise a major functional block. As the disk rotates at a fixed speed and the recording heads are flown over the disk surface, the positioner is controlled in both the velocity and position modes. The positioner moves to the correct address under control of the positioner servo control electronics. Data are then written on (or read from) the desired surface by selecting the corresponding head through the head-select network.

The read/write electronics are sub-divided into three functional blocks consisting of the head-select network, the write electronics, and the read channel. Write data causes write current to be switched according to the pulse train on the WRITE DATA SIGNAL line. The storage surface will then be magnetized accordingly.

During retrieval of the stored data, the corresponding head is again selected by the head-select network and the signal obtained from the read/write head is processed by the read channel into separate READ DATA and READ CLOCK signals for transmission via the interface. The particular segment of the disk which is passing under the read/write head is specified by the sector pulse and the sector count lines from the sector electronics.

Control of the rotational speed of the disk is accomplished by the speed control electronics group which establishes a known, fixed speed for the disk rotation within ± 1 percent speed tolerance. The sector electronics block provides pulses at the interface which electrically subdivide the disk into a number of sectors for the purpose of addressing data stored on the disk. Figure 1-5 illustrates the subdivision of a disk into 8 sectors by means of mechanical sectoring.

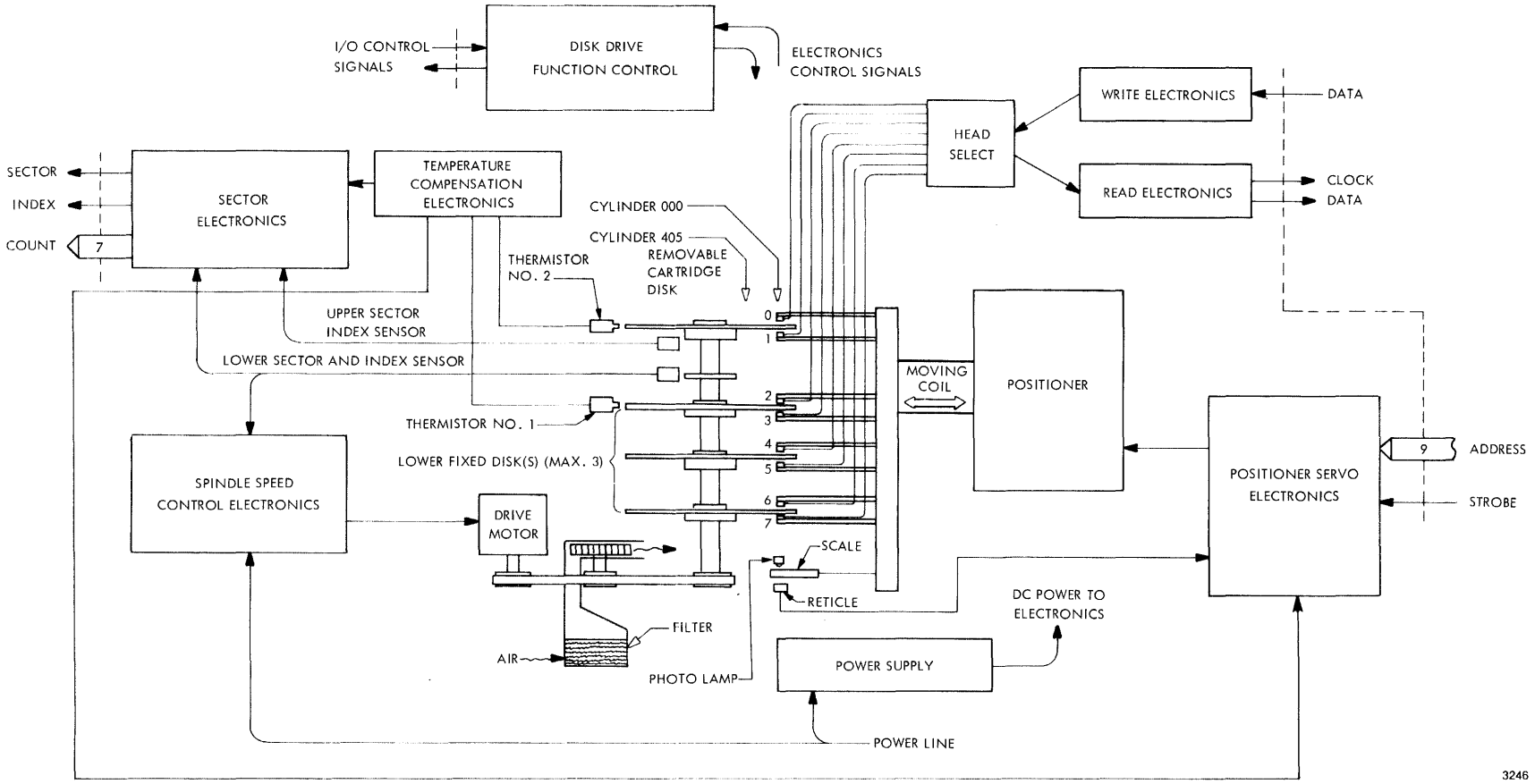


Figure 1-4. Functional Block Diagram

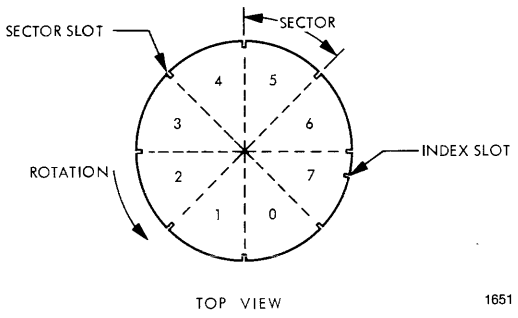


Figure 1-5. Mechanical Sectoring

The air system consists of an absolute filter preceded by a pre-filter, and a blower driven by the same motor that provides drive to the disk spindle. This air system provides a well-filtered flow of clean air in the disk area to remove contaminants. In addition, an exhaust fan at the rear of the drive removes heat generated by the adjacent PCBAs.

Power to the various electronic circuits is provided by an integral power supply. This power provides dc voltages at suitable levels derived from the line voltage.

All major components are mounted to the base assembly. An aluminum alloy casting is the basic component of the base assembly. Mounted onto the casting is the drive mechanism which consists of a precision spindle, an ac induction drive motor, a squirrel cage blower, and an idler system. Power to rotate the blower and spindle is transmitted from the drive motor by means of a flat belt. The idler system provides constant tension of the belt and compensates for stretch of the belt.

Mounted to the spindle assembly is a ring with equally spaced notches and one additional notch spaced midway between two of the other notches; this is referred to as the Phase Lock Ring and is used for sectoring and speed control.

In quad-disk models, the removable cartridge is driven by magnetic clutch which is located on top of the spindle assembly. Three fixed disks are also mounted to the spindle assembly but are not removable in the same manner as the cartridge. A precision-ground cone on the end of the spindle suitably locates the hub of the disk, which is mounted in the cartridge types used for quad-disk models. Rotary motion is imparted to all disks simultaneously.

The blower is in operation while the drive motor is running and the disks are spinning. Air flow from the blower travels through the disk area and purges the air of any contaminants in this area. Air is drawn in at the lower front part of the front bezel and passes through a high efficiency absolute filter located in the lower front portion of the base assembly.

Air is ducted to the squirrel cage blower and thence to the area below the fixed disk. Suitable vanes on the spindle provide additional pumping action to cause air to flow into the area of the upper platter. Air is exhausted at the rear of the disk drive. Additional cooling is provided by the fan at the rear of the drive which exhausts the air adjacent to the PCBAs thus preventing temperature buildup.

The base assembly provides mounting attachment points for the rack-mounting slides, switch brackets, front bezel, and the supporting structure for the PCBAs and dust cover.

The positioner, in conjunction with the positioner servo and control electronics, is used to position the read/write heads to one of a possible 406 cylinders. Each concentric track on the disk surface describes a circle which, when extended vertically through the disk, creates an imaginary cylinder. If, for example, four disks are stacked on the same spindle, the walls of the imaginary cylinder pass through both surfaces of each disk. Each disk, therefore, has twice as many tracks as cylinders because the tracks appear on both disk surfaces.

The *cylinder* concept was created mainly to minimize the complexity of the sector/track and address software. Figure 1-6 defines the relationship between disk, cylinder, and track as used throughout this document.

The positioner is a moving coil type of linear motor wherein the signal applied to the coil results in a magnetic field which reacts with the magnetic field of the permanent magnet. The force thus produced is used for controlling the position of the carriage.

The position of the positioner carriage is sensed by using the optical detent type of position transducer. Speed of the positioner carriage movement is controlled by a velocity signal which is derived electronically from the position signal.

NOTE

There is no actual mechanical detenting of the positioner carriage. The positioning at a given cylinder is achieved entirely by electronic techniques.

Dc power to the various electronic circuits is provided by the power supply which takes the line voltage input, transforms it to a suitable voltage level, then rectifies and filters the output of the transformer. The output is then provided to the power regulators on the Servo PCBA.

Also contained on the power supply assembly are the motor-start capacitors for the ac induction drive motor and a small Motor Control PCBA. The Motor Control PCBA contains ground isolation and power control circuitry for operating the drive motor. This PCBA is separate from other PCBAs in order to isolate the line voltage.

1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications for the disk drive are shown in Table 1-4.

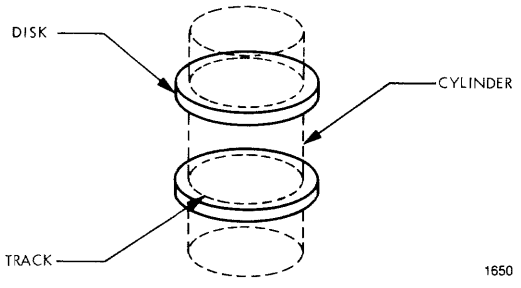


Figure 1-6. Disk, Cylinder, Track Relationship

Table 1-4
Mechanical and Electrical Specifications

Storage Capacity (Unformatted)	
Split-Quad Disk Models at 2200 bpi	203.0 megabits
Quad-Disk Models at 2200 bpi	203.0 megabits
Cylinders/Tracks	
Split-Quad Disk Models	406 cylinders/3248 tracks
Quad-Disk Models	406 cylinders/3248 tracks
Sectors	6,8,10,12,14,16,18,20,24,28,30,32,36,40,42,48,56,60,64
Bits per Inch/Tracks per Inch	2200 bpi/200 tpi
Data Transfer Rate	
2200 bpi, 1500 rpm	1.56250 megabits per second
2200 bpi, 2400 rpm	2.50000 megabits per second
Disk Speed	1500 or 2400 rpm (±1%)
Latency Time (Average)	
1500 rpm Models	20 milliseconds (±1%)
2400 rpm Models	12.5 milliseconds (±1%)
Head Positioner	Voice Coil Linear Motor with Optical Detent
Seek Time	
Adjacent Track	10 milliseconds maximum
Average (One-third Stroke)	40 milliseconds maximum
Maximum (Full Stroke)	70 milliseconds maximum
Start Time	120 seconds maximum
Stop Time	60 seconds maximum
Removable Media Type	IBM 5440 or 2315-type cartridge, or equivalent
Read/Write Heads	
Type	Ramp Loaded, Cartridge-Disk Heads (Radially Aligned) Ramp Loaded, Fixed-Disk Heads (Radially Offset)
Number	2, 4, 6, or 8 (One per Disk Surface)
Recording Mode	Double Frequency
Dimensions	
Height	222.3 mm (8.75 inches) maximum
Width	482.6 mm (19 inches)
Depth from Mounting Surface	660.4 mm (26 inches)
Front Projection from Mounting Surface	82.6 mm (3.25 inches)
Total Depth	743.0 mm (29.25 inches)
Mounting	Standard 482.6 mm (19-inch) EIA
Weight (excluding Slides and Cartridge)	
Top Loading Models	57.6 Kg (127 lbs) maximum (including Integral Power Supply)
Front Loading Models	55.8 Kg (123 lbs) maximum (including Integral Power Supply)
Operating Temperature	+10°C to 34°C (50°F to 95°F)
Non-Operating Temperature	−40°C to +65°C (−40°F to +144°F)
Operating Humidity	5% to 85% Non-Condensing
Storage Humidity	5% to 95% Non-Condensing for Temperatures ≤40°C (104°F) 5% to 80% Non-Condensing for Temperatures ≥65°C (149°F)
Operating Altitude	0 to 2286 m (0 to 7500 feet)
Non-Operating Altitude	0 to 6096 m (0 to 20,000 feet)
Power	
Volts ac	95, 100, 110, 115, 125, 190, 200, 215, 220, 225, 230, 235, 240, 250
Watts (Maximum on High Line)	1100 Peak (Start/Stop Cycles Only)
(Typical)	350 or less
Hertz	48 to 52 and 58 to 62
Electronics	All Silicon
Underwriters Laboratory	Designed to be approved
Canadian Standard	Designed to be certified

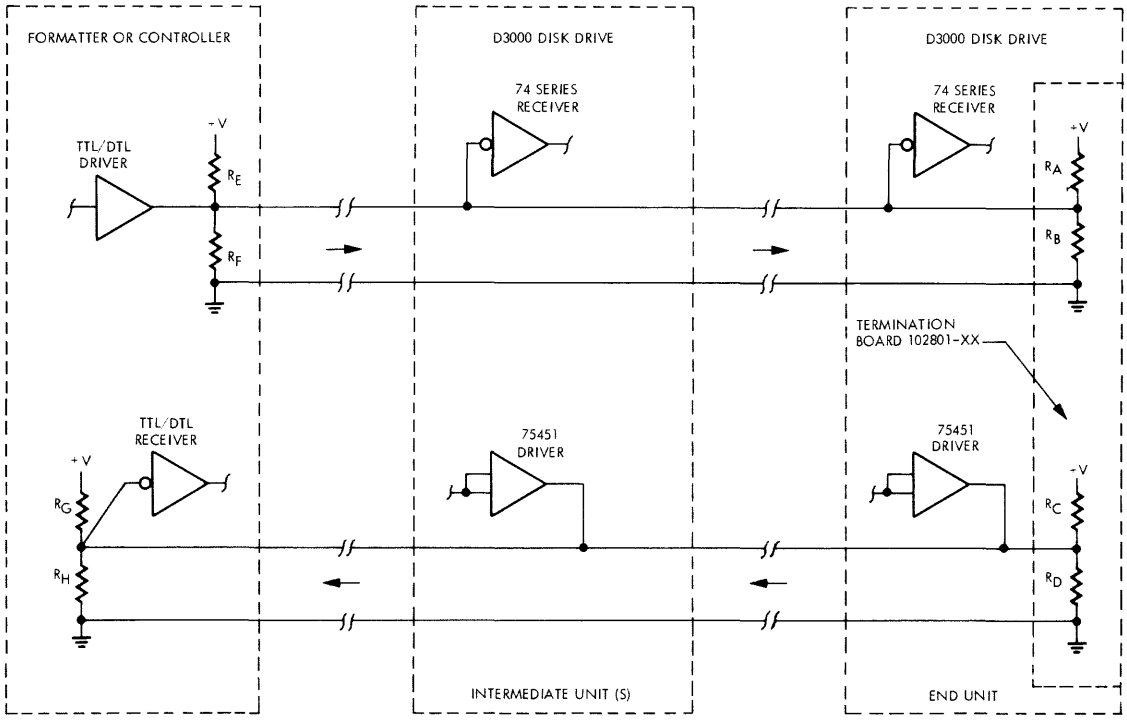
1.5.1 INTERFACE SPECIFICATIONS

Dc levels:

True = Low = +0.2v dc ±0.2v

False = High = +3.0v dc $^{+2.3v}_{-0.6v}$

The interface circuits are designed so that any disconnected wire results in a false signal. Figure 1-7 shows the configuration for which the drivers and receivers have been designed.



D3000 INSTALLATION CONFIGURATION	USE TERMINATION BOARD PART NO.	CORRESPONDING VALUES AT D3000 DISK DRIVE					TYPICAL VALUES AT CONTROLLER					NOTES AND COMMENTS
		R_A	R_B	R_C	R_D	+V	R_E	R_F	R_G	R_H	+V	
D3000 STANDARD MULTIPLE UNIT INSTALLATION VOLTAGE SUPPLIED BY DISK DRIVE (DAISY CHAIN)	102801-03	220	330	220	330	+5.0	220	330	220	330	+5.0	MAY ALSO BE USED FOR SINGLE UNIT INSTALLATION
D3000 STANDARD SINGLE UNIT INSTALLATION	102801-02	220	330	NONE	NONE	+5.0	NONE	NONE	220	330	+5.0	
COMPATIBLE WITH D5000 DAISY CHAIN TYPE INTERFACE	102801-04	120	NONE	120	NONE	+3.5	120	NONE	120	NONE	+3.5	
COMPATIBLE WITH D5000 SINGLE UNIT TYPE INTERFACE	102801-05	270	NONE	120	NONE	+3.5	160	NONE	120	NONE	+3.5	
D3000 STANDARD MULTIPLE UNIT INSTALLATION VOLTAGE SUPPLIED BY CONTROLLER (DAISY CHAIN)	102801-06	220	330	220	330	+5.0	220	330	220	330	+5.0	MAY BE USED FOR SINGLE UNIT INSTALLATION
SPECIAL DESIGN BY CUSTOMER	102801-01											ORDER DRAWINGS: 102800, 102801, 102835, 102836, 102841, 102770

Figure 1-7. Interface Configuration

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating and mounting the unit, as well as the procedure for electronically connecting and initially checking out the disk drive.

2.2 UNCRATING THE DISK DRIVE

The D3000 Disk Drive is shipped in a heavy duty container consisting of an inner and outer carton. Use of the dual carton minimizes the possibility of damage during shipment. To uncrate the disk drive:

(1) Place the shipping container in the position indicated by the arrows on the outer carton.

(2) Open the outer carton and remove the packing material.

(3) Open the inner carton and remove the disk drive.

(4) Lift the drive and its shipping frame and set it on a clean work surface. Ensure access to the top of the unit.

CAUTION

THE D3000 DISK DRIVE WEIGHS 64 KG (141 POUNDS) IN ITS SHIPPING CONFIGURATION. DO NOT ATTEMPT TO LIFT THE DRIVE WITHOUT SUFFICIENT PERSONNEL.

(5) Check the contents of the shipping container against the packing slip and investigate for possible damage. Notify the carrier if damage is noted.

CAUTION

TO AVOID DAMAGE TO EQUIPMENT, DO NOT ATTEMPT TO APPLY POWER TO THE DISK DRIVE UNTIL ALL POSITIONER AND MECHANISM SHIPPING RESTRAINTS HAVE BEEN REMOVED.

(6) Remove the polyethylene bag that surrounds the unit; remove the dust cover as follows.

- ☐ Top Load Models
  - (i) Remove the 4 screws around the top of the adapter bowl.
  - (ii) Remove the 5 screws along the side of the unit.
  - (iii) Lift the rear of the dust cover approximately 30 degrees, then carefully move the cover toward the rear of the unit until the front edge of the cover clears the bezel; remove the dust cover.
- ☐ Front Load Models
  - (i) Remove the 2 screws on top of the dust cover.
  - (ii) Remove the 5 screws along the sides of the unit.
  - (iii) Slide the dust cover toward the rear of the unit until the front edge clears the bezel.
  - (iv) Remove the dust cover.
  - (v) Remove the two tie-down straps used to secure the front door and cartridge receiver during shipment. Figure 2-1 shows the relationship of these restraints to the shipping frame and disk drive.

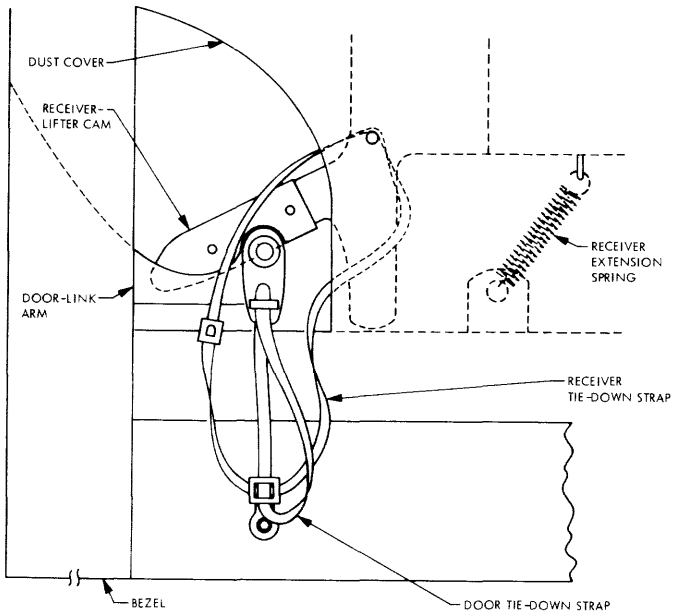


Figure 2-1. Cartridge Receiver and Front Door Shipping Restraint

(7) Locate and loosen the two retaining screws (shown in Figure 2-2) on top of the Logic PCBA; rotate the hinged card structure up and to the rear. The spring-loaded PCBA pivot-lock will automatically lock the Logic PCBA into the vertical position as shown in Figure 2-3.

NOTE

Illustrations used in this manual to depict parts and locations which are common to front and top loading versions will normally be of front loading models.

(8) Loosen the two retaining screws which secure the Servo PCBA to the Logic PCBA (see Figure 2-3).

(9) Swing the Servo PCBA into its extended position; engage the locking pin and the PCBA support bracket (see Figure 2-4).

(10) Loosen and remove the horizontal tie-down screw and rubber grommet that anchors the Balance Weight on the carriage assembly to the magnet assembly. Store the screw and rubber grommet in the tapped hole provided on the base assembly, adjacent to the position transducer assembly.

CAUTION

IF THE UNIT IS SHIPPED, THE TIE-DOWN SCREW AND RUBBER GROMMET MUST BE USED TO SECURE THE CARRIAGE ASSEMBLY. TIGHTEN THE TIE-DOWN SCREW FIRMLY BUT NOT TO THE POINT OF DISTORTING THE GROMMET. TIGHTENING THE SCREW BEYOND THIS POINT CAN CAUSE DAMAGE TO THE CARRIAGE BEARINGS.

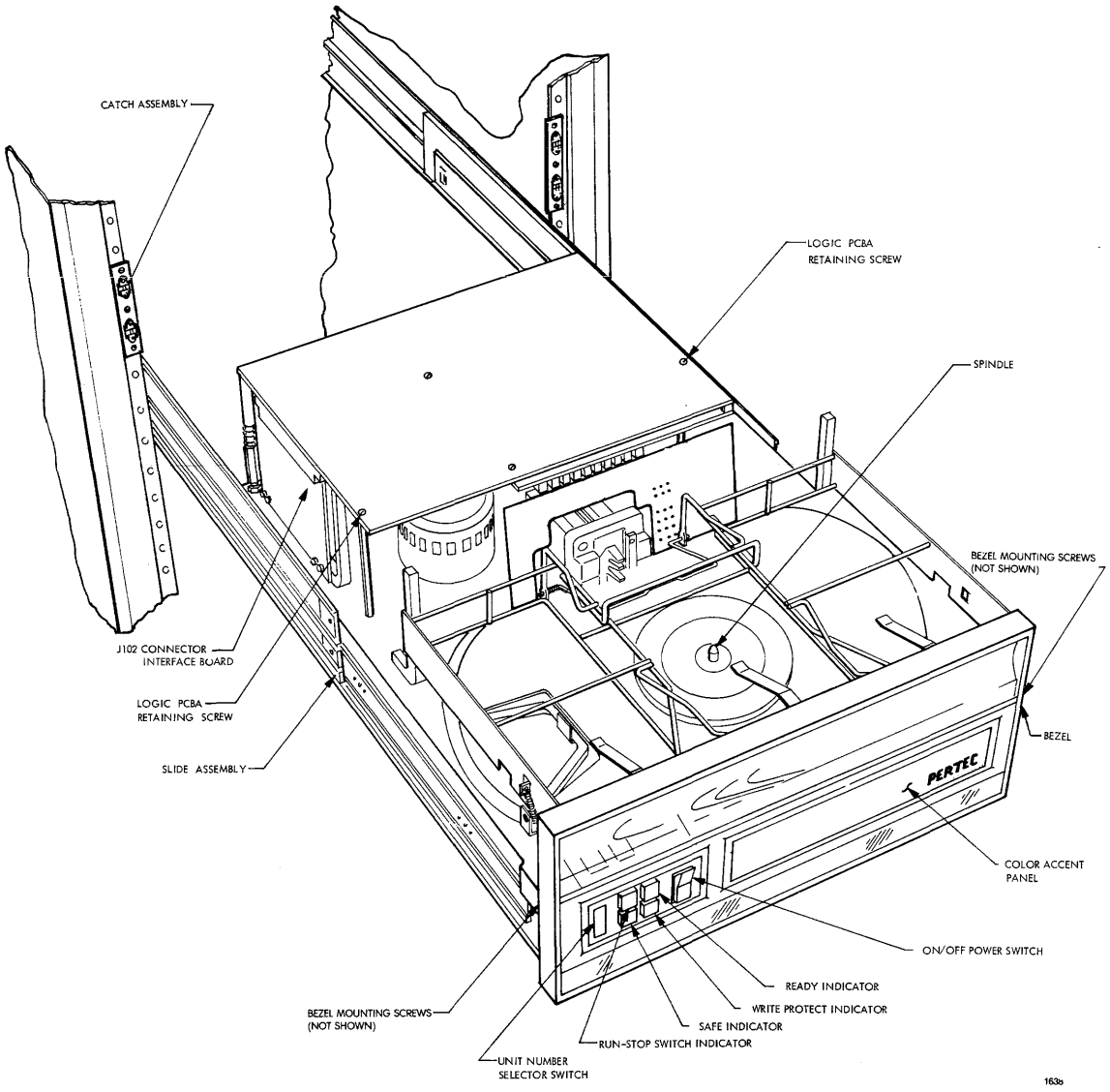


Figure 2-2. Rack Mounting the D3000 Disk Drive

(11) Check that the identification label on the rear of the unit bears the correct model number, line voltage, and line frequency. If the actual line voltage or frequency at the installation differs from that on the identification label, refer to Section IV of this manual.

CAUTION

OPERATOR MUST EXERCISE CAUTION WHEN EXTENDING OR LOWERING THE LOGIC AND SERVO PCBAS TO AVOID CRIMPING CABLING AND/OR DISENGAGING MOLEX CONNECTORS.

2.3 POWER CONNECTIONS

A fixed power cord is supplied for use in a polarized 115v or 220v outlet. For other power sockets, the supplied plug must be removed and the correct plug installed. Table 2-1 lists (in several languages) the color code scheme used to identify the supplied power cord.

2.4 INITIAL CHECKOUT PROCEDURE

A description of the controls and indicators used for operation of the D3000 Disk Drive is contained in Section III. To check the proper operation of the disk drive before placing it in a system, the following procedure should be performed.

(1) With the protective dust cover removed and the Servo PCBA in the raised position as shown in Figure 2-4, inspect the PCBAs, connectors, and cables. Verify that shipping damage has not occurred. Check the connectors and plug-in relay for proper installation.

(2) Verify that the positioner is in the fully retracted position.

(3) Verify that the cartridge area is free of dirt, contaminants, and shipping material.

(4) Verify that the ON/OFF switch is set to OFF.

CAUTION

CONNECTING THE DRIVE TO A LINE VOLTAGE OTHER THAN THAT SELECTED VIA THE TRANSFORMER TAPS CAN RESULT IN DAMAGE TO THE UNIT.

(5) Verify that connections to the power transformer are compatible with the local power source to which the disk drive is to be connected (see Paragraph 4.9); connect the power cord to the correct line voltage.

(6) Place the power ON/OFF switch to the ON position; the ON indicator and the SAFE indicator should illuminate within 2 seconds.

CAUTION

ON TOP LOAD MODELS, IF THE CARTRIDGE-LOCK ARM IS PIVOTED OUT OVER THE BOWL, DO NOT ATTEMPT TO ROTATE THE LOCK ARM TO THE STORED POSITION UNTIL POWER IS APPLIED AND THE ON/OFF SWITCH IS IN THE ON POSITION.

(7) Load the cartridge as described in Paragraph 3.4.1 or 3.4.3.

CAUTION

LOADING AND OPERATING WITH DIRTY, DAMAGED, OR DEFECTIVE CARTRIDGES WILL CAUSE DAMAGE TO THE DISK DRIVE.

(8) Depress and release the RUN/STOP switch/indicator; verify that during the Start sequence:

- The RUN/STOP indicator becomes illuminated immediately.
- The SAFE indicator is extinguished.
- The disk comes up to speed.
- The positioner loads the heads over the disk(s).
- The READY indicator becomes illuminated within 120 seconds after actuation of the RUN/STOP switch/indicator.

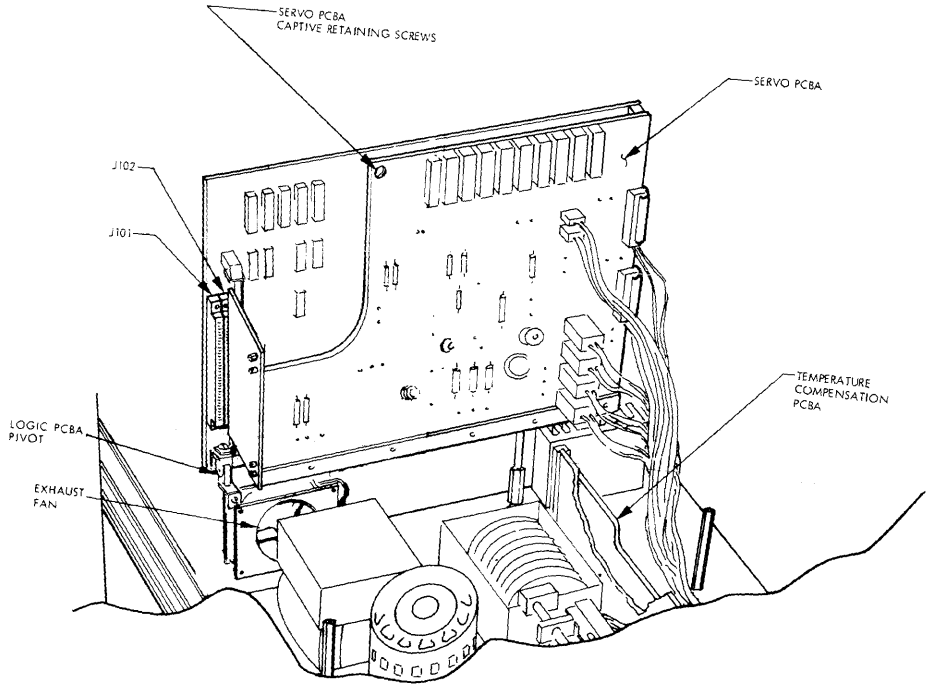


Figure 2-3. Component Identification, Logic and Servo PCBAs Extended

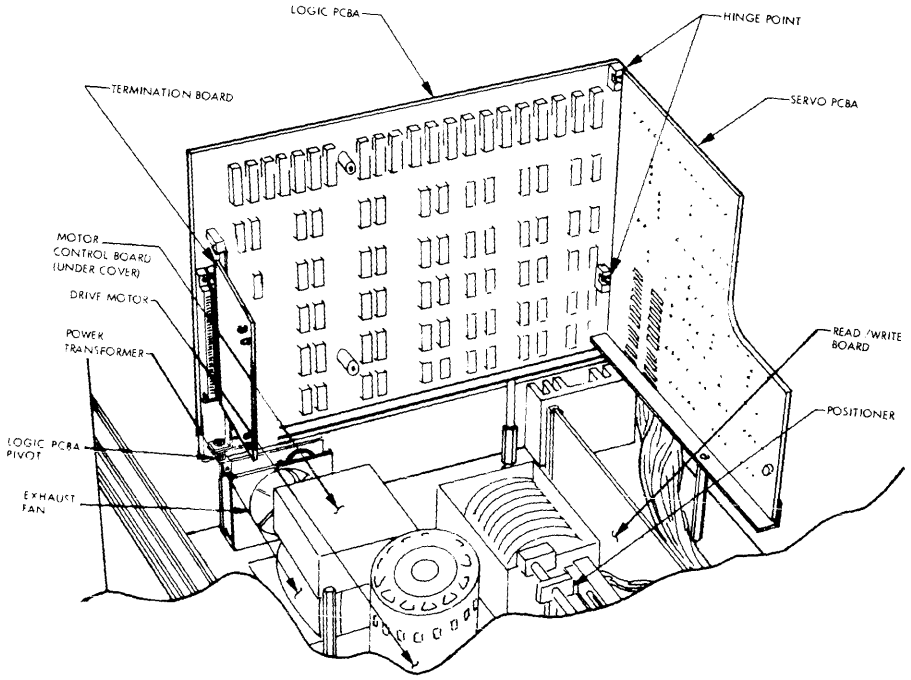


Figure 2-4. Component Identification

Table 2-1
Power Cord Color Code

Black or Brown AC 'Hot' (Live)	**Noir** Phase	**Nero** Vivo	**Schwarz** Heiss
White or Blue AC Return (Neutral)	**Blanc** Neutre	**Bianco** Neutro	**Weiss** Neutral
Green or **Green with Yellow Stripes** Chassis Ground (Earth)	**Vert** Chassis (Terre)	**Verde** Terra	**Grun** Grund

(9) Depress and release the RUN/STOP switch/indicator; verify that during the Stop sequence:
- The READY and RUN/STOP indicators are extinguished.
- The heads are slowly unloaded from over the disk(s).
- The disk(s) come to a stop.
- The SAFE indicator becomes illuminated within 60 seconds after RUN/STOP is actuated.

(10) Repeat Step (8) to return the disk drive to the Ready condition.

(11) Place the power ON/OFF switch to the OFF position; verify that:
- The positioner immediately retracts the heads from over the disk(s) at a high but controlled rate of speed (emergency unload).
- The cartridge access door is locked (front load models); the cartridge lock arm is locked (top load models).

(12) Before the disk has the opportunity to coast to a stop, place the power ON/OFF switch to the ON position; verify that the SAFE indicator does not become illuminated until after the disk(s) has coasted to a stop.

(13) Remove the cartridge as described in Paragraph 3.4.2 or 3.4.4.

(14) Place the power ON/OFF switch to the OFF position.

(15) Position the Servo PCBA in the closed position and secure it to the Logic PCBA with the two captive retaining screws (shown in Figure 2-3).

(16) Slide the spring-loaded sleeve of the Logic PCBA pivot lock downward to release the pivot lock (see Figure 2-3).

CAUTION

OPERATOR MUST EXERCISE CAUTION WHEN EXTENDING OR LOWERING THE LOGIC PCBA AND SERVO PCBA TO AVOID CRIMPING CABLING AND/OR DISENGAGING MOLEX CONNECTORS.

(17) Lower the Logic PCBA and secure it to the PCBA support brackets using the two retaining screws (shown in Figure 2-2).

2.5 INTERFACE CONNECTIONS

The D3000 interface is configured to provide flexibility in the design of new controllers and remain compatible with existing controllers designed for the D5000 Disk Drives. The D3000 will also operate in conjunction with the F3000 Disk Formatter.

The 3M flat cable used in the fabrication of the D3000 Input/Output (I/O) cables has the following specifications.

(1) Number of conductors: 36
(2) Conductor size: 24
(3) Impedance: 100 ohm

The maximum length of the conductor between the D3000 and the Controller/Formatter in a multiple disk drive installation is 6.1 m (20 feet). The maximum length of conductor between adjacent disk drives in a daisy-chain configuration is 3.0 m (10 feet).

D3000 Disk Drives are normally supplied with a mating input/output cable board and a termination board. These boards must be installed as shown in Figure 2-5. Interface signals are routed to and from the disk unit via the input/output cable board. Table 2-2 shows the input/output lines required. Details of the interface are contained in Section III.

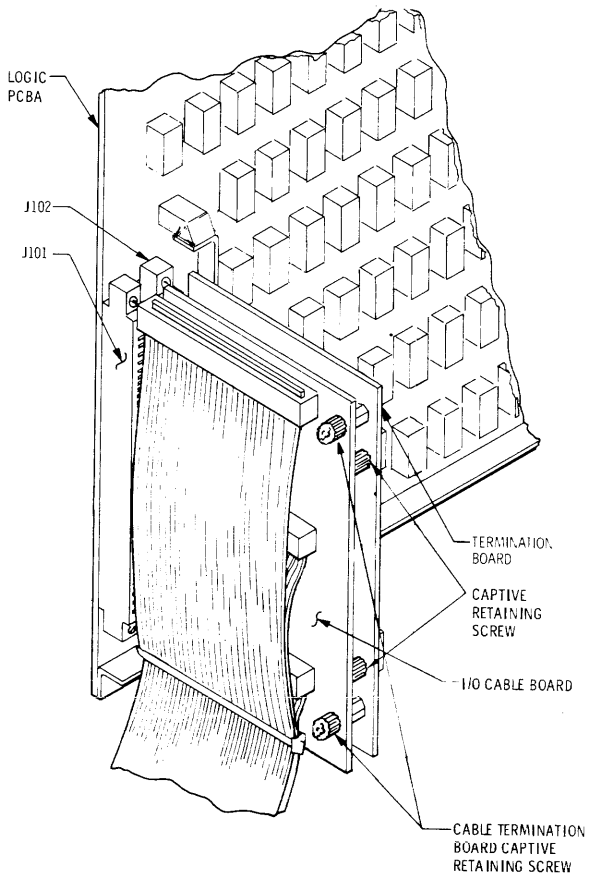


Figure 2-5. Interface Connector Board Installation

Table 2-2
Input/Output Interface Lines

Input Lines (26 Total)	Mnemonic	Pin	Gnd	Function	Para. Ref.
Unit Select No. 1	IUS1R	B42	B41	Disk Drive Unit Selection	3.16.1
Unit Select No. 2	IUS2R	A42	A41		
Unit Select No. 3	IUS3R	B43	B44		
Unit Select No. 4	IUS4R	A43	A44		
Platter Select 1	IPSXR	B27	B26	Storage Surface Selection	3.16.2
Platter Select Extension	IESLR	A30	A29		3.16.2
Head Select	IHSXR	A27	A26		3.16.3
Cylinder Address Strobe	ICASR	B33	B32	Head Positioning Control	3.16.4
Cylinder Demand Address 0	ICD0R	A39	A38		3.16.5
Cylinder Demand Address 1	ICD1R	B39	B38		
Cylinder Demand Address 2	ICD2R	A37	A38		
Cylinder Demand Address 3	ICD3R	B37	B38		
Cylinder Demand Address 4	ICD4R	A36	A35		
Cylinder Demand Address 5	ICD5R	B36	B35		
Cylinder Demand Address 6	ICD6R	A35	A35		
Cylinder Demand Address 7	ICD7R	B34	B35		
Cylinder Demand Address Extension	ICDER	A33	A32		
Restore Initial Cylinder	IRICR	A31	A32		3.16.6
Write Enable	IWEXR	B22	B23	Write Operation Control and Data Input	3.16.7
Erase Enable	IEEXR	A22	A23		3.16.8
Write Data Signal	IWDSR	A28	A29		3.16.9
Read Enable	IREXR	B24	B23	Read Control	3.16.11
Track Offset Plus	ITOPR	B25	B26	Margin Test Control	3.16.12
Track Offset Minus	ITOMR	A25	A26		
Activate Emergency Unload	IAEUR	B31	B32	Emergency Control	3.16.10
Start/Stop Disk Drive	ISSDR	B30	B29	Remote Start and/or Stop Control	3.16.13

Output Lines (27 Total)	Mnemonic	Pin	Gnd	Function	Para. Ref.
Ready	IRXXD	B1	B2	Unit Operational Status	3.17.1
Busy Seeking No. 1	IBS1D	B19	B20	Individual Unit Positioning Busy Status	3.17.2
Busy Seeking No. 2	IBS2D	A19	A20		
Busy Seeking No. 3	IBS3D	B21	B20		
Busy Seeking No. 4	IBS4D	A21	A20		
Sector Pulse	ISPXD	A4	A5	Sector Locating Status	3.17.3
Sector Count 0	ISC0D	A15	A14		3.17.4
Sector Count 1	ISC1D	B15	B14		
Sector Count 2	ISC2D	A13	A14		
Sector Count 3	ISC3D	B13	B14		
Sector Count 4	ISC4D	A12	A11		
Sector Count 5	ISC5D	B12	B11		
Sector Count 6	ISC6D	A10	A11		
Index Pulse	IIPXD	B4	B5		3.17.5
Read Clock	IRCXD	B16	B17	Read Operation Data Output	3.17.7
Read Data	IRDXD	A16	A17		3.17.8
Illegal Cylinder Address	IICAD	B3	B2	Situation Status	3.17.6
File Protected	IFPXD	A1	A2		3.17.9
Malfunction Detected	IMDXD	B6	B5		3.17.10
Dual Platter Drive	IDPDD	B7	B8	Disk Drive Model Type Status	3.17.11
Quad Platter Drive	IQPDD	B18	B17		3.17.12
Double Track Drive	IDTDD	A7	A8		3.17.13
Special Interface Signal	——	A3	A2	Status	3.17.14
Termination Voltage	——	A45	B45	Status	3.17.15
+ 5v dc	——	B48	A48	—	—
+ 5v dc	——	B49	A49	—	—
+ 5v dc	——	B50	A50	—	—

NOTE: The following are spare pins: A6, A9, A18, A24, A40, B9, B10, B28, B40

There are three types of cable available for use with the D3000 Disk Drives.

(1) Controller to Disk Drive cable for a non-specified controller. This cable is 3M flat cable with an input/output cable board on one end to mate with the D3000; the other end is free to accommodate connection to a controller input/output board. This cable is available from PCC PD in lengths of 1.5, 3.0, and 6.1 m (5, 10, and 20 feet); refer to the Spare Parts List, Table 7-8, for specific part numbers.

(2) I/O Link cable (daisy-chain). This cable is 3M flat cable with an input/output cable board on each end to join two D3000 drives. This cable is available from PCC PD in lengths of 1.5, 2.1, and 3.0 m (5, 7, and 10 feet); refer to the Spare Parts List, Table 7-8, for specific part numbers.

(3) F3000 Formatter cable. This cable is 3M flat cable with an input/output cable board on one end to mate with a D3000 drive and an input/output cable board on the other end to mate with an F3000 Formatter. This cable is available from PCC PD in lengths of 1.5, 3.0, and 6.1 m (5, 10, and 20 feet); refer to the Spare Parts List, Table 7-8 for specific part numbers.

2.6 RACK MOUNTING THE DISK DRIVE

The disk drive is entirely self-contained (including power supply). The unit is 203.2 mm (8.75 inches) high, requires 660.4 mm (26 inches) rack depth, and extends 82.6 mm (3.25 inches) from the front mounting surface. The unit is designed to be mounted in any equipment rack or desk having standard EIA mounting rails at the front and rear. Mounting for two slide configurations is described.

All models are supplied with heavy duty chassis slides, carefully selected to give the optimum in unit serviceability. When mounted in the rack, the chassis may be extended fully forward for servicing; where servicing from the front is not practical, the unit may be extended from the rear.

CAUTION

DUE TO THE WIDE RANGE OF SLIDE TRAVEL, A CABINET OF SUFFICIENT STATURE MUST BE USED TO REDUCE THE POSSIBILITY OF UPSETTING THE CABINET WHEN THE UNIT IS FULLY EXTENDED TO THE FRONT OR REAR. REFER TO DWG NO. 103587 (SECTION VII) FOR CG LOCATIONS AT THESE EXTREMES BEFORE INSTALLING THE UNIT.

2.6.1 SLIDES

Remove the slide set (Part No. 102731 or 103670) and the installation kit (Part No. 102723) from the shipping container. Slide set Part No. 102731 extends the disk drive 762 mm (30 inches) to the front and 635 mm (25 inches) to the rear of the cabinet; slide set Part No. 103670-01 extends the disk drive 489 mm (19.25 inches) to the front and 750 mm (29.5 inches) to the rear of the cabinet.

2.6.2 INSTALLATION OF SLIDE SET PART NO. 102731

Refer to Figure 2-2 and Drawing No. 103587 in conjunction with the following mounting procedure. The front and rear slide brackets and the slides are marked 'LH' and 'RH' for correct assembly.

CAUTION

TO EXTEND THE DISK CHASSIS FROM THE REAR OF THE CABINET, THE BEZEL MUST BE REMOVED; REFER TO PARAGRAPH 2.6.2, STEP (4).

(1) Assemble the front and rear right-hand brackets to the right-hand slide assembly; assemble the front and rear left-hand brackets to the left-hand slide assembly. The bracket screw heads must be installed on the track side of the slide; the nuts will therefore appear on the bracket side, or outside, of the slide assembly. Use lock washers under the nuts.

(2) Install the right and left slide assemblies to the front and rear EIA rails. Adjust the distance between the slide brackets to 451.6 mm (17.78 inches). Ensure that the right front and rear slide brackets, as well as the left slide brackets, are installed at the same height as on the front and rear rails. The screw heads must be on the outside of the EIA rails.

(3) Pull the smaller chassis slide member forward to expose the screw holes that will be used to attach the small slide member to the disk chassis.

(4) Remove the bezel assembly from the disk drive by removing the three screws on each side of the bezel and sliding the bezel assembly forward until free of the chassis (refer to Figure 2-2 for location of these screws).

(5) Remove the eight screws which attach the shipping frame to the disk chassis and lift the unit free of the frame.

(6) With the right and left chassis slides extended fully forward, slide the disk drive chassis between the inner members until the front slide mounting hole pattern lines up with the tapped holes in the chassis. Thread three 8-32 × ¼-inch button-head screws through the slide and into the chassis. Perform this on each side of the chassis.

(7) Slide the unit through the cabinet to the rear and thread two additional 8-32 × ¼-inch button-head screws through the slide and into the chassis on each side.

(8) Locate the chassis in the closed position in the cabinet. Adjust each slide bracket height by loosening the slide bracket screws to obtain the 5.97 mm (0.235-inch) dimensions as shown in Drawing No. 103587.

(9) Reinstall the bezel.

(10) Install the slide restraining blocks (Part No. 102776) at the rear of the cabinet using the hardware provided. Adjust the restraining blocks to prevent the intermediate slide member from working to the rear during normal operation.

(11) For top load models only, install the brim (Part No. 102691) using the hardware provided.

(12) Install the catch assemblies as shown in Figure 2-2 using the hardware provided. Adjust the catch spring on the EIA rail so the ball stud assembly installed on the bezel strikes the catch spring on the EIA rail squarely. Apply a small amount of lubricant (PCC PD Part No. 665-0004, or equivalent) to each ball stud.

2.6.3 INSTALLATION OF SLIDE SET PART NO. 103670

Figure 2-6 and Drawing No. 103587 show the relationship of the rail mounting brackets to a standard EIA cabinet and should be referred to in conjunction with the following procedure.

Prior to installation of the disk mounting slides, determine the exact location in the cabinet in which the drive is to be mounted.

NOTE

To ensure correct hole spacing positions for slide mounting bracket, catch assemblies, and top load brim assembly, location of the bottom surface of the bezel must lie between a pair of rail holes spaced ½-inch apart.

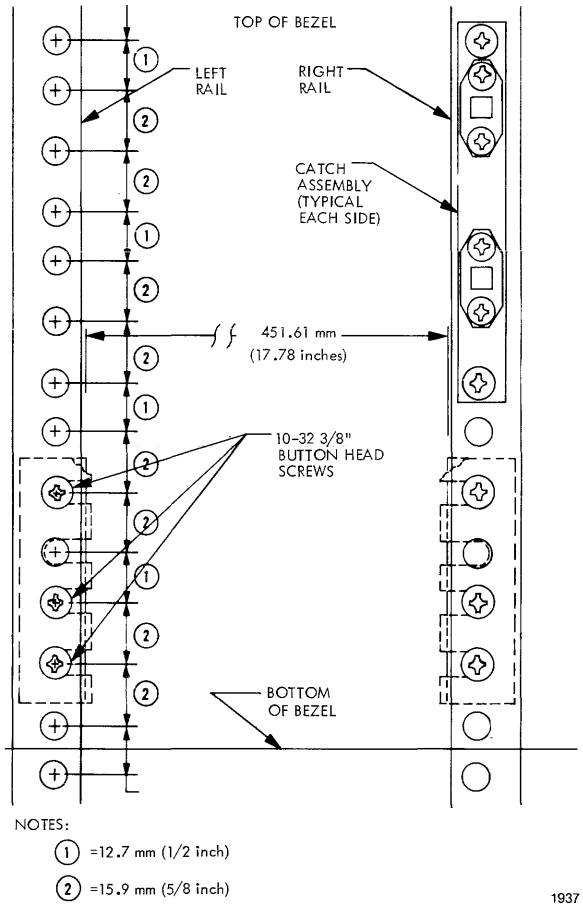


Figure 2-6. Mounting Bracket to EIA Cabinet; Hardware Orientation for use with P/N 103670

(1) Thread and tighten three 10-32 × 3/8-inch button-head Phillips screws for each pair of front and rear brackets into the EIA rails; spacing must be as shown in Figure 2-6.

(2) Place a star lockwasher and 10-32 nut on each of the three screws. The nuts should be started onto the screw only far enough to hold. The mounting bracket will be secured between the back of the EIA mounting surface and the lockwasher.

NOTE

If the cabinet rails have untapped mounting holes, the nut bars furnished in the hardware kit are to be used in place of the 10-32 nuts.

(3) Install the right and left brackets to the rails and tighten the 10-32 nuts sufficiently to hold them in place.

(4) Determine that the bracket surface adjacent to the rail is parallel to the rail and to the side of the cabinet.

(5) Establish that the measurement between the brackets is 45.14 mm (17.78 inches) as shown in Figure 2-7. Tighten the 10-32 nuts on the right and left brackets. If this measurement is not held, the bezel may not fit between the trim molding on the cabinet. Note that dimension 'A' must equal dimension 'B'.

NOTE

Steps (1) through (5) must be repeated when the rear brackets are installed.

(6) By inspection, determine which slide assembly and mounting holes will be used for the installation.

(7) Install the slide assemblies to the brackets using 8-32 × 3/8-inch Phillips screws; tighten hardware finger tight.

(8) Extend the small slide bar as far forward as possible to expose two Allen-head stop screws located in the body of the lower slide of the slide assembly.

(9) Loosen the Allen-head stop screws so that 4 or 5 threads are showing. Move each small slide bar to the extreme rear position (all the way out the rear of the cabinet) to ensure that they do not become disengaged from the main slide assembly.

(10) Remove the small slide bar from the main slide assembly by moving the small slides all the way out of the front of the cabinet.

NOTE

The small slide bar will be attached to the disk drive.

(11) Install restraining blocks to each of the rear rails with 10-32 × 3/8-inch Phillips button-head screws. Position each restraining block so that the slide member will be prevented from projecting beyond the rear of the cabinet.

(12) Install the small slides (removed in Step 10) to the right and left sides of the disk drive casting with 8-32 × 3/8-inch button-head Phillips screws.

CAUTION

ENSURE THAT THE DIMPLE ON EACH SMALL SLIDE MEMBER APPEARS BELOW THE CENTERLINE OF THE SLIDE BAR; FAILURE TO DO SO WILL ALLOW THE DISK DRIVE TO BE PULLED FROM THE SLIDE ASSEMBLY.

(13) Extend each cabinet mounted slide assembly fully forward until a mechanical stop is reached.

(14) Install the disk drive to the two main slide assemblies which project from the front of the cabinet by engaging the small slides on the disk drive with each of the extended slide assemblies.

(15) Slide the disk drive into the cabinet to the closed position, i.e., the point at which the bezel is seated against the cabinet rails.

(16) Carefully pull the disk drive forward about 6 inches until the first setscrew is exposed on the right and left slide assemblies.

(17) Tighten the left and right setscrews until they bottom out on their respective slide assemblies; at this point, back off each setscrew one full turn.

(18) Carefully pull the disk drive forward about 16 inches until the second setscrew is exposed on the right and left slide assemblies.

(19) Repeat Step (17).

(20) Carefully extend the disk drive forward about 30 inches, at which point the slides strike the second setscrews in each slide assembly.

(21) In the position indicated in Step (20), the PCBAs may be raised for servicing.

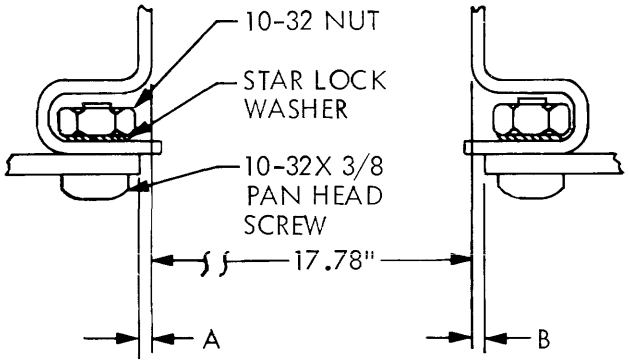


Figure 2-7. Inside Measurement Between Slide Brackets

SECTION III
OPERATION

3.1 INTRODUCTION

This section explains the manual operation of the disk drive and defines the interface functions with regard to timing, levels, and interrelationships.

3.2 CARTRIDGE HANDLING AND STORAGE

The magnetic coatings on the disk surface have the ability to retain recorded intelligence for an indefinite period. The recorded data does not tend to weaken or fade with age; however, the physical properties of the recording medium are susceptible to damage.

It is important that the disk cartridge be properly handled and stored so that the integrity of the recorded data is maintained. A damaged or contaminated cartridge can impair or prevent recovery of data and can result in damage to the disk drive.

CAUTION

DO NOT ATTEMPT TO INSTALL OR USE A CARTRIDGE WHICH DOES NOT HAVE A DISK-DRIVE COMPATIBLE BIT-DENSITY RATING OR IS SUSPECTED OF DAMAGE OR CONTAMINATION.

A disk drive that has been damaged or contaminated due to use of a defective cartridge should not be operated with other cartridges until the disk drive has been inspected and/or reconditioned by qualified service personnel. The rated density of each cartridge must be compatible with that of the drive being used.

The following methods will ensure maximum protection of disk cartridges.

(1) The head port door on front load cartridges should be kept closed when the cartridge is not inserted in a drive. This prevents the ingress of dirt and secures the disk internally.

(2) Top load cartridges should have the bottom cover in place at all times when the cartridge is not inserted in a drive. Do not allow the bottom cover to accumulate dirt or other debris.

(3) Cartridges can be stored either horizontally or vertically. Front load cartridges must always be positioned to avoid objects which could damage the hub or cause the air inlet door to be pushed open.

CAUTION

DO NOT PLACE CARTRIDGES IN A STACK CONTAINING MORE THAN FIVE CARTRIDGES.

(4) Avoid exposing the cartridge to any magnetizing force in excess of 50 oersted or loss of stored data may result.

NOTE

The 50 oersted level of magnetizing force is reached at a distance of approximately 3 inches from a typical source, e.g., motors, generators, transformers.

(5) Do not store the cartridge in direct sunlight; temperatures outside the range of 0.6°C to 60°C (33°F to 140°F) should be avoided for non-operational storage.

(6) Internal, as well as external, damage to a cartridge can result if dropped. If a cartridge is dropped, it should be inspected by a qualified service representative.

(7) Front load cartridges should be labeled only in the area of the label frame, which is molded as part of the handle; top load cartridges should be labeled only in the handle recess area. Placement of labels in any other areas may cause improper operation or contamination.

3.3 DISK DRIVE PREPARATION

The initial checkout procedure in Section II should be performed prior to placing the disk drive in a system environment.

Optimum data reliability can be obtained only when the protective dust cover is installed on the drive. Also, to ensure proper operation and data reliability, it is necessary that disk cartridges be temperature stabilized at the disk ambient temperature for 2 hours.

The following initial preparation must be performed before attempting to insert a cartridge into the drive.

(1) Ensure that the power cord is connected to the correct line voltage.

(2) Place the ON/OFF switch in the ON position and observe that the associated indicator becomes illuminated.

(3) Observe that the SAFE indicator becomes illuminated within 2 seconds of the ON indicator illumination.

3.4 CARTRIDGE LOADING AND UNLOADING

The following paragraphs describe the proper method to load and unload disk cartridges. Procedures for front load models are contained in Paragraphs 3.4.1 and 3.4.2; procedures for top load models are contained in Paragraphs 3.4.3 and 3.4.4.

3.4.1 LOADING A CARTRIDGE, FRONT LOAD MODELS

Refer to Figures 3-1 through 3-3 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Referring to Figure 3-1, grip the handle formed by the top of the front bezel and move the handle out and downward; this will open the drive door and cam the cartridge receiver into position to accept a cartridge.

CAUTION

DO NOT ATTEMPT TO INSTALL A CARTRIDGE WHICH DOES NOT HAVE A DISK-DRIVE COMPATIBLE BIT-DENSITY RATING OR IS SUSPECTED OF DAMAGE OR CONTAMINATION.

(3) Grip the cartridge by the molded handle and position the cartridge in the receiver opening as shown in Figure 3-2. Note that the raised portion of the cartridge top is aligned between the guide rails at the top of the receiver. Slant the cartridge to match the slope of the bottom of the receiver.

(4) Press the cartridge slowly but firmly most of the way into the receiver; relax the grip on the cartridge handle and press the cartridge fully into the receiver, seating it completely within the receiver as shown in Figure 3-3.

(5) Close the door on the front of the drive by moving the door handle (top of the front bezel) up and toward the drive. As the door is closed, the cartridge will be positioned onto the spindle.

CAUTION

IF THE CARTRIDGE IS NOT PROPERLY INSERTED IN RECEIVER, THE DOOR WILL NOT CLOSE. DO NOT

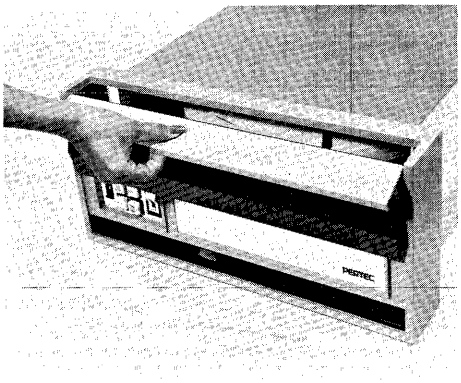


Figure 3-1. Cartridge Loading/Unloading, Front Load Models

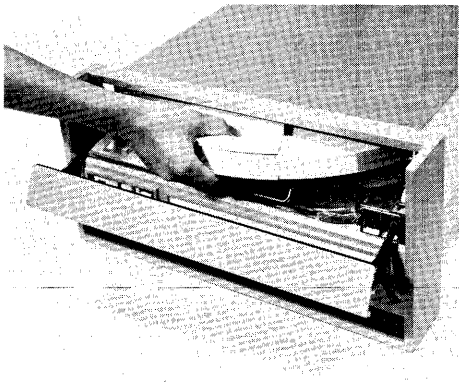


Figure 3-2. Cartridge Loading/Unloading, Front Load Models

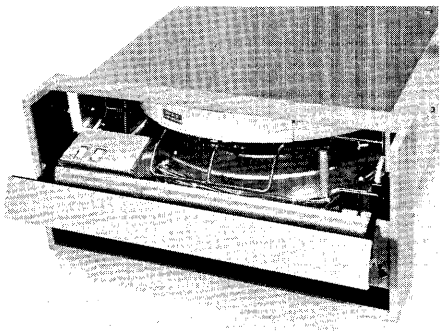


Figure 3-3. Cartridge Inserted, Front Load Models

ATTEMPT TO FORCE THE DOOR CLOSED AS DAMAGE TO THE CARTRIDGE AND THE DRIVE WILL RESULT; REPEAT STEPS (1) THROUGH (5).

DO NOT ATTEMPT TO START THE DRIVE UNTIL THE DOOR IS FULLY CLOSED.

3.4.2 UNLOADING A CARTRIDGE, FRONT LOAD MODELS

Refer to Figures 3-1 and 3-2 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Referring to Figure 3-1, grip the door handle formed by the top of the front bezel and move the handle out and downward, opening the door.

(3) Grip the cartridge by the molded handle and pull the cartridge slowly out of the receiver (Figure 3-2).

(4) Unless another cartridge is to be inserted immediately, close the door to exclude dirt and contamination from the interior of the drive.

3.4.3 LOADING A CARTRIDGE, TOP LOAD MODELS

Refer to Figures 3-4 through 3-9 in conjunction with the following procedure.

CAUTION

DO NOT ATTEMPT TO LOAD A CARTRIDGE UNLESS SAFE INDICATOR IS ILLUMINATED.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Grip the handle formed by the top of the front bezel and slowly pull the disk drive from the cabinet on its slides until the cartridge area is accessible.

(3) Ensure that the cartridge lock arm is positioned away from the disk area as shown in Figure 3-4.

NOTE

The cartridge lock arm must be rotated completely into its recess.

(4) With the cartridge positioned as shown in Figure 3-5, press the cartridge release/lock (with the thumb) all the way to the side. Holding the cartridge release/lock, grip and pull the cartridge handle smartly to the vertical position shown in Figure 3-6. The cartridge is now released from the cover.

(5) Referring to Figure 3-7, place the cartridge over the cartridge adapter bowl with the handle recess pointing downward (approximately 30 degrees) toward the rear of the drive. Slide the lowered edge of the cartridge under the fixed retainer arm; then lower the cartridge into the adapter, positioning it so that the keys on the wall of the adapter engage the key notches in the base of the cartridge.

NOTE

Correct positioning of the cartridge has been obtained if the cartridge rim is fully seated against the adapter bowl along the complete periphery of the rim. When the cartridge is correctly seated, it cannot be rotated or tilted.

CAUTION

DO NOT ATTEMPT TO FORCE-SEAT ANY CARTRIDGE; DAMAGE TO THE CARTRIDGE AND DRIVE WILL RESULT.

(6) Lower the cartridge handle into the handle recess and allow the release/lock to return (Figure 3-8). This will cause the cartridge hub to engage the spindle clutch.

(7) Invert the cartridge cover (removed in Step 4) and place it over the cartridge, aligning the cover edge over the ridge along the cartridge rim.

(8) Position the cartridge lock arm over the cartridge cover (allowing the arm to cam upward) until the arm comes to rest against the stop provided by the side of the recesses in the adapter bowl (Figure 3-9).

CAUTION

IF EITHER THE CARTRIDGE OR COVER HAS NOT BEEN PROPERLY POSITIONED, IT WILL NOT BE POSSIBLE TO ROTATE THE ARM INTO THE CORRECT POSITION; THIS WILL PREVENT THE DRIVE FROM STARTING. DO NOT ATTEMPT TO FORCE THE ARM. ROTATE THE ARM BACK INTO THE RECESS AND CORRECTLY POSITION THE CARTRIDGE COVER.

(9) Push the disk drive into the cabinet until the catches engage.

3.4.4 UNLOADING A CARTRIDGE, TOP LOAD MODELS

Refer to Figures 3-10 and 3-11 in conjunction with the following procedure.

CAUTION

DO NOT ATTEMPT TO REMOVE A CARTRIDGE UNLESS THE SAFE INDICATOR IS ILLUMINATED.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Grip the handle formed by the top of the front bezel and slowly pull the drive from the cabinet on its slides until the cartridge area is accessible.

(3) Rotate the cartridge lock arm away from its position over the cartridge cover to the recess in the bowl as shown in Figure 3-4.

(4) Lift the cartridge cover out of the drive (Figure 3-8) and invert it.

(5) Press the cartridge release/lock (with the thumb) all the way to the side. Holding the cartridge release/lock as shown in Figure 3-10, grip and pull the cartridge handle smartly to the vertical position. The cartridge is now disengaged from the clutch.

(6) Carefully lift the cartridge out of the adapter bowl and place it into the cartridge cover as shown in Figure 3-11.

(7) Press the cartridge handle into the cartridge cover recess and release; this causes the cartridge hub to engage the cover, thus securing the disk.

3.5 SELECTING WRITE PROTECTION

When the disk drive is equipped with WRITE PROTECT switches, the operator should select the appropriate switch setting at the time the cartridge is inserted. Table 3-1 shows the various WRITE PROTECT switch combinations necessary to write protect specific disks in the dual-disk, quad-disk, and split quad-disk models.

On front load models, the switches are mounted inside the door, behind the operator switch panel; the drive must be in a Safe condition as indicated by the SAFE indicator in order to open the door and gain access to the WRITE PROTECT switches. On top load models, the switches are mounted at the left rear of the cartridge adapter and are accessible through the top of the dust cover only when the unit is pulled forward out of the cabinet.

To select write protection for a particular disk(s), refer to Table 3-1 and set the applicable switch(s) to the ON position. To enable writing for a particular disk(s), set the applicable switch(s) to the OFF position.

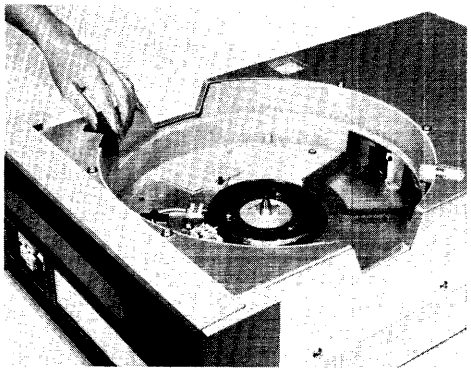


Figure 3-4. Cartridge Loading, Top Load Models (Lock Arm Away from Disk Area)

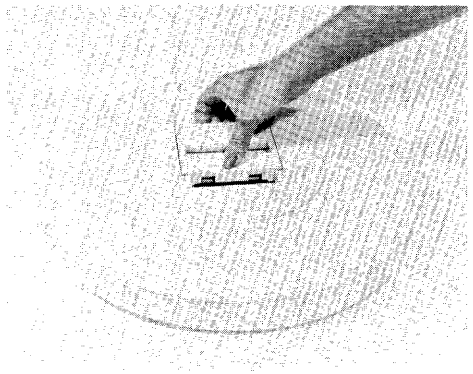


Figure 3-5. Cartridge Loading, Top Load Models (Release/Lock Down)

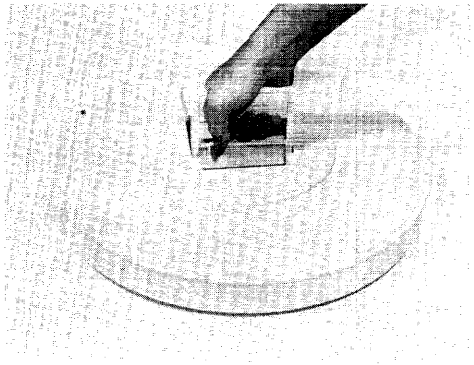


Figure 3-6. Cartridge Loading, Top Load Models (Release/Lock Up)

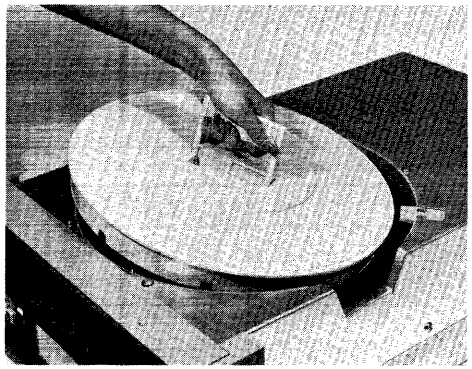


Figure 3-7. Cartridge Loading, Top Load Models (Cartridge Positioned over Adapter Bowl)

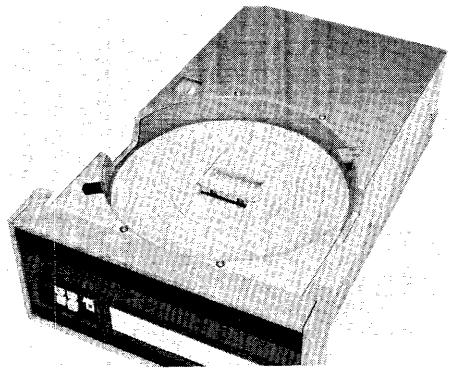


Figure 3-8. Cartridge Loading, Top Load Models (Cartridge Loaded, Release/Lock Down)

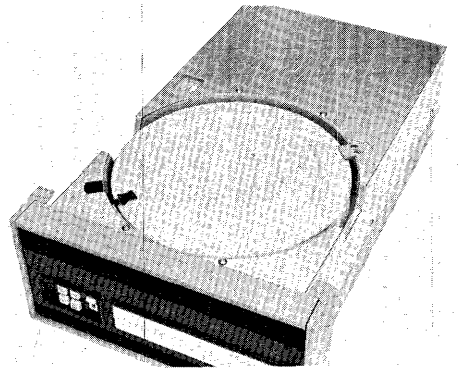


Figure 3-9. Cartridge Loading, Top Load Models (Lock Arm Over Cartridge Cover)

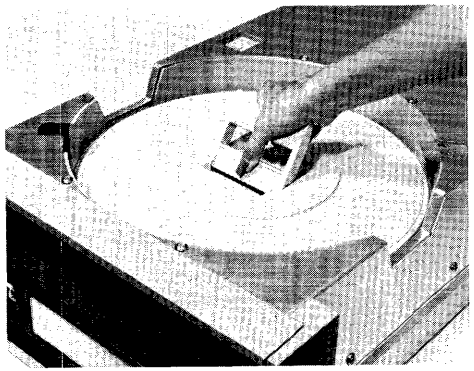


Figure 3-10. Cartridge Unloading, Top Load Models

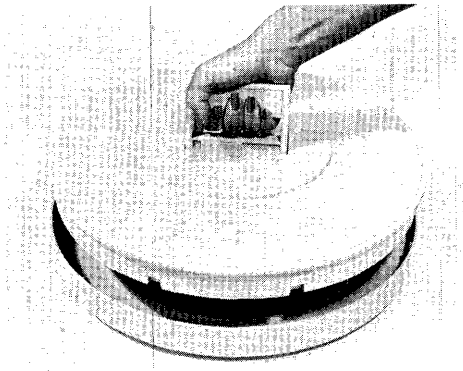


Figure 3-11. Cartridge Unloading, Top Load Models

Table 3-1
WRITE PROTECT Switch Combinations

Dual-Disk Models

Drive Type	Write-Protect Switches Upper	Write-Protect Switches Lower	PROT/PROT Indicator	Write-Protected Surface* 0	1	2	3	4	5	6	7
Dual	ON	OFF	Lit	Yes	Yes	No	No	—	—	—	—
Dual	OFF	ON	Lit	No	No	Yes	Yes	—	—	—	—
Dual	ON	ON	Lit Lit	Yes	Yes	Yes	Yes	—	—	—	—
Dual	OFF	OFF	—	No	No	No	No	—	—	—	—
Quad-Disk Models											
Quad	ON	OFF	Lit	Yes	Yes	No	No	No	No	No	No
Quad	OFF	ON	Lit	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Quad	ON	ON	Lit Lit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Quad	OFF	OFF	—	No	No	No	No	No	No	No	No

*See disk and disk-surface profile, and identification drawing.

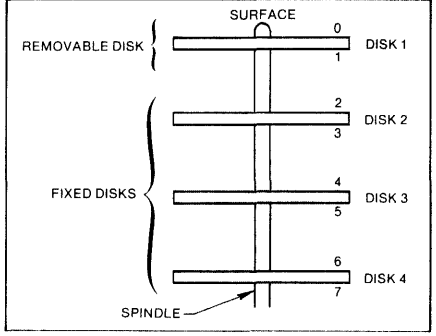
Split Quad-Disk Models

Write Protect Switches Upper	Write Protect Switches Lower	PROT/PROT Indicator	Unit No. Select Switch	Write-Protected Surface** Split-Quad (Dual) 0	1	2	3	Split-Quad (Dual) 4	5	6	7
ON	OFF	Lit	1	Yes	Yes	No	No	No	No	No	No
OFF	ON	Lit	1	No	No	Yes	Yes	Yes	Yes	Yes	Yes
ON	ON	Lit Lit	1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ON	OFF	Lit	2	—	—	—	—	No	No	No	No
OFF	ON	Lit	2	—	—	—	—	Yes	Yes	Yes	Yes
ON	ON	Lit Lit	2	—	—	—	—	Yes	Yes	Yes	Yes
				Write-Protected Disk Surfaces in the Quad-Disk Unit Daisy Chained to the First Unit.							
ON	OFF	Lit	3	Yes	Yes	No	No	No	No	No	No
OFF	ON	Lit	3	No	No	Yes	Yes	Yes	Yes	Yes	Yes
ON	ON	Lit Lit	3	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ON	OFF	Lit	4	—	—	—	—	No	No	No	No
OFF	ON	Lit	4	—	—	—	—	Yes	Yes	Yes	Yes
ON	ON	Lit Lit	4	—	—	—	—	Yes	Yes	Yes	Yes

*In split-quad models, Unit Select Switch numbers 1 and 2 or 3 and 4 are wired so that another unit can be daisy chained.

**See disk and disk-surface profile and identification drawing.

Disk and Disk Surface Profile and Identification



When a WRITE PROTECT switch is set to the ON position, the particular disk(s) is protected from write operations regardless of any write commands which may be received. When a WRITE PROTECT switch is set to the OFF position, write operations may be executed unless the write protect status is set by the controller through the Write Protect input line on the interface.

3.6 STARTING THE DISK DRIVE

Upon completion of the relevant cartridge load procedure, the drive may be started as follows.

(1) Depress and release RUN/STOP switch/indicator on the operator control panel.

NOTE

Illumination of RUN/STOP indicates there are no inhibiting conditions and the drive is rotating the disk(s).

(2) Observe that the READY indicator becomes illuminated within 120 seconds after actuating the RUN/STOP switch/indicator.

NOTE

Illumination of READY indicates the drive is ready to accept interface commands.

3.7 STOPPING THE DISK DRIVE

To stop the disk drive while RUN/STOP is illuminated, perform the following procedure.

(1) Depress and release the RUN/STOP switch/indicator.

(2) Observe that the SAFE indicator becomes illuminated within 60 seconds, indicating the disk(s) has come to a stop and the cartridge may be removed or changed.

3.8 DESIGNATING UNIT NUMBER

When the disk drive is equipped with a Unit Number Selector Switch, the setting of this switch determines which interface UNIT SELECT line the drive will respond to, i.e., the switch position specifies the device (unit) address.

The operator should set the switch to the appropriate position as specified by the system and software operating procedures for the particular installation.

The switch is set by moving the thumbwheel until the desired number appears in the window adjacent to the thumbwheel. Although there are eight positions on the switch (0 through 7), only positions 1 through 4 are used. This corresponds to the maximum number of D3000 drives which can be daisy chained in a single system.

A drive may be designated a particular unit number, subject to the restriction that different units on the common I/O bus must not have the same number assigned. Since the switches in different units are not interlocked, if two (or more) drives are accidently assigned the same unit number and that number is then selected by the controller, undefined operation may occur.

CAUTION

LOSS OF DATA MAY OCCUR IF THE UNIT NUMBER SELECTOR SWITCH IS REPOSITIONED DURING A WRITE OPERATION.

3.9 CE ALIGNMENT

Prior to placing the disk drive into operation, the CE alignment procedure in Section VI must be performed. Because misalignment of only 200 μinches is significant and the amount of shock a unit may encounter during shipping cannot be controlled, the CE alignment is mandatory on all models.

3.10 PERIODIC MAINTENANCE

Periodic maintenance requirements of the disk drive are detailed in Section VI of this manual. Periodic cleaning of the heads and disks, and filter changing, should be performed according to the prescribed schedules and procedures.

3.11 INTERLOCK PROTECTION

The operator should not attempt to force or override the various protection interlocks provided by the drive. These interlocks are designed to prevent damage to data contained in the disk cartridges, and to the drive equipment. Front load models are interlocked by a switch that senses when a cartridge is correctly inserted into the receiver. When a cartridge is not inserted in the receiver, or is incorrectly inserted, the switch will not be actuated and this condition is sensed by the logic, which prevents the drive from responding to RUN/STOP operator commands and START/STOP DISK DRIVE interface commands.

If the door is not properly closed on front load models, either as a result of the cartridge being incorrectly inserted or because of operator error, the switch will not be actuated; this results from the fact that as the receiver lowers a properly inserted cartridge down onto the spindle clutch, the cartridge body actuates the switch lever. Additionally, the door is locked whenever the drive is not in a Safe condition (the SAFE indicator is not illuminated).

Top load models are interlocked by a switch that senses the position of the cartridge lock arm. This switch will be actuated only when the lock arm is fully rotated toward the spindle and when the correct height is sensed by the lock arm. This condition will exist when a cartridge has been correctly seated on the aligning keys and the cartridge bottom cover has been correctly positioned over the top of the cartridge. When a cartridge is inserted incorrectly, or a cartridge is inserted without a cover, or only a cover is inserted, or when a cartridge having a non-compatible bit-density rating is inserted, the correct height will not be sensed by the switch. Therefore, the drive will be unable to respond to RUN/STOP operator commands or START/STOP DISK DRIVE interface commands.

To prevent removal of a cartridge during unsafe conditions, the cartridge lock arm will be locked whenever the drive is not in a Safe condition.

In addition to the electro-mechanical interlock protection, additional interlocking is provided via certain logic within the drive. If the operator should actuate the RUN/STOP switch/indicator, or if the interface should command a Stop sequence as a result of a change of state on the START/STOP DISK DRIVE line during the time that a Write and/or Erase operation is in progress, the heads will not be unloaded immediately from the storage surfaces, even though the drive prepares to execute a Stop sequence. Only when the controller has completed the current Write and/or Erase operation will the heads be unloaded from the storage surface. This prevents the loss of data in the event that the operator attempts to stop the drive during the time that a write data transfer is in progress.

An additional interlock prevents changing the Write Protect status if a Write and/or Erase operation is in progress. Write protect status cannot be changed electrically regardless of the positions of the WRITE PROTECT switches. Only after completion of the current Write and/or Erase operation will the write protect status change to agree with the particular switch setting.

This is primarily applicable to top load models, although the same logic is present in all machines. The purpose of this arrangement is to prevent loss of data in the event an operator should change the condition of the WRITE PROTECT swiches during the time the controller is in a write data transfer.

3.12 SAFE CONDITION

The Safe condition for both front and top load models is indicated by illumination of the SAFE indicator and is defined by:

(1) Power correctly applied.

(2) Disk not rotating.

(3) Heads retracted.

(4) Emergency or fault conditions not being detected by the logic.

(5) Disk drive not executing a brake cycle or a stop sequence.

Additionally, it should be noted that although the drive is in a Safe condition, it is not necessarily enabled to respond to start commands. The conditions which inhibit starting the drive are:

(1) The cartridge is not properly inserted.

(2) Power is not applied.

(3) An internal emergency or fault condition exists and is being detected.

(4) The ACTIVATE EMERGENCY UNLOAD line is being asserted.

3.13 EMERGENCY AND FAULT DETECTION

When power to a disk drive is lost when the disk is spinning, it is impossible for the drive to maintain disk speed at a value which assures that the heads will continue to fly above the surface of the disk.

In order to protect the data and the cartridge, as well as the drive, it is necessary to remove the heads from the surface of the disk as fast as possible when a power fault is detected. This process is referred to as Emergency Unload. Additionally, there are other conditions which are undesirable, either from the standpoint of potential hazard to data or to the drive.

It is also important to be able to communicate emergency conditions to the drive via the ACTIVATE EMERGENCY UNLOAD interface line and cause the drive to enter an Emergency Unload mode. This is appropriate in situations when a fault or the failure of power to the computer and/or controller could result in a situation where the controller can no longer maintain control of the interface lines. All of these conditions are sensed by the drive logic and may cause the drive to perform an emergency unload.

Notwithstanding conditions communicated via the ACTIVATE EMERGENCY UNLOAD interface line, the conditions which can cause an emergency unload are summarized as follows.

(1) Loss of ac or dc power.

(2) Disk speed does not remain within tolerance or is at an incorrect speed at the time it is tested.

(3) Positioner error is detected.

(4) Write circuit faults that could affect the stored data are detected.*

*If emergency unload is due to a WRITE CHECK, the unit will not return to a Safe condition until the RUN/STOP switch is depressed or the Power switch is cycled to OFF and then to ON again.

3.14 MANUAL CONTROLS

The operational controls and indicators are located on the front panel of the disk drive; additionally, one or two rocker-type switches may be located inside the drive which provide protection from inadvertent write operations. The following paragraphs describe the functions of these controls.

3.14.1 ON/OFF

The ON/OFF power control is a rocker-type switch/indicator which provides the operator a means of energizing and de-energizing the power to the drive. The indicator is illuminated when power is ON and the internal +5v power is operational.

3.14.2 RUN/STOP

The RUN/STOP control is a momentary action switch/indicator which provides a means of selecting the operational status of the drive. The alternate action arrangement is provided by the drive logic. The control will be illuminated when actuated and the drive has been properly conditioned to allow the disk to be brought to operating speed.

When the illuminated switch/indicator is depressed again, a Stop sequence will be entered and the disk will decelerate to a stop, after which the SAFE indicator will become illuminated. The cartridge may be unloaded at this time.

If a cartridge has been incorrectly inserted or an emergency condition exists, the operation of the RUN/STOP control is inhibited. Under this condition, the control will not become illuminated and the Run status will not be achieved.

3.14.3 READY

This is an indicator which is illuminated when the drive achieves a Ready condition. The Ready condition is defined in Paragraph 3.17.1.

3.14.4 SAFE

This is an indicator which is illuminated when it is possible to safely insert or remove the disk cartridge. When the SAFE indicator is extinguished, protective cartridge locks prevent removal of the cartridge.

CAUTION

DO NOT ATTEMPT TO FORCE REMOVAL OF A DISK CARTRIDGE WHEN THE SAFE INDICATOR IS EXTINGUISHED. FAILURE TO OBSERVE UNSAFE CONDITION CAN RESULT IN DAMAGE TO THE EQUIPMENT.

3.14.5 PROT (PROTECT) INDICATORS

Two indicators, mounted in a common housing, are provided to indicate the data protection status of the disk(s). This status information can be from the WRITE PROTECT switches (Paragraph 3.14.7), or from a hard-wired configuration.

When the upper PROT indicator is illuminated, the upper (removable) disk is protected from a write operation; protection of the lower (fixed) disk(s) is indicated by illumination of the lower PROT indicator.

The indicators are extinguished when the respective switch (or hard-wired configuration) is set to permit write operations. Table 3-1 shows the condition of the PROT indicators in relation to the WRITE PROTECT switches and the disk surfaces that are write protected.*

*To reset the write protect condition, the RUN/STOP switch must be depressed or the Power switch cycled from ON to OFF and then back to ON.

3.14.6 UNIT NUMBER SELECTOR SWITCH

A 4-position thumbwheel switch may be included on the front panel of the drive to provide a means for selecting one of several peripheral units on a common I/O bus.

Any drive may be assigned (designated) a particular unit number (unit address) subject to the restriction that different units on the bus may not have the same number. Since the switches in different units are not interlocked, if two (or more) drives are accidentally assigned the same unit number and that number is then selected by the controller, undefined operation may occur. Refer to Paragraph 3.8 for additional information on designating a unit number.

When the split quad-disk option is exercised, the unit can be configured to act like two separate dual-disk drives. This is accomplished by jumper plugs on the Logic PCBA which alter the thumbwheel Unit Selector Switch circuitry so that the appropriate pair of disks can be chosen on the front panel.

When the thumbwheel switch is not included, the drive will respond to UNIT SELECT NO. 1 line or other SELECT lines as indicated by customer order.

3.14.7 WRITE PROTECT SWITCHES

Two rocker switches are included in the D3000 Series Disk Drive. These switches selectively protect the disks from inadvertent write operations.

In quad-disk models, the disk(s) protected from inadvertent write operations depends upon the ON/OFF combination of both the upper and lower WRITE PROTECT switches as determined in Table 3-1. The upper WRITE PROTECT switch, in the ON position, write protects the upper (removable) disk. The lower WRITE PROTECT switch, in the ON position, write protects all fixed disks. To write protect the fixed disks selectively, the lower WRITE PROTECT switch must be in the OFF position and the WRITE PROTECT INPUT line must be pulsed by the controller via the interface.

On front load models, the switches are mounted to the rear of the operator control panel. Access to the switches can be obtained only after the door is opened. On top load models, the switches are mounted at the left rear of the cartridge adapter and are accessible only when the unit is pulled forward out of the cabinet.

When a WRITE PROTECT switch is set to the ON position, the particular disk is protected from write operations regardless of any write commands which may be received. When a WRITE PROTECT switch is set to the OFF position, write operations may then be executed unless the write protect status is set by the controller through the WRITE PROTECT INPUT line on the interface.

The PROT indicators (Paragraph 3.14.5) indicate the status of the WRITE PROTECT switches.

3.15 D3000 INTERFACING

The D3000 interface is described in two sections: Controller (or Formatter) -to-Disk Drive, and Disk Drive-to-Controller (or Formatter). The interface is arranged such that as many as four different disk drives may be operated on the interface by a common controller. This is accomplished by providing a group of (disk drive) input lines and a group of output lines which become a common I/O bus. This bus is time-shared by the various drives that may be connected with the bus, i.e., a daisy-chain arrangement.

3.16 INTERFACE INPUTS (CONTROLLER-TO-DISK DRIVE)

All signal names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the low (true) condition considered to be 0v, and the high (false) condition considered to be + 3v.

3.16.1 UNIT SELECT LINES (IUS1R—IUS4R)

A low level on one of the four UNIT SELECT lines will connect one predetermined disk drive to the common I/O bus.

The low level on one of these lines enables all input/output lines except the START/STOP DISK DRIVE line which is enabled at all times.

When the Unit Number Selector switch is included, the units are identified to switch positions and select lines on a one-to-one basis, i.e., switch position 1, UNIT SELECT NO. 1 line, etc.

After a unit has been selected and the I/O bus has been allowed 2 μsec to stabilize, the selected drive will recognize inputs and provide stable outputs.

3.16.2 PLATTER SELECT (IPSXR) AND PLATTER SELECT EXTENSION (IESLR)

The IPSXR line determines which disk is selected. When the level on this line is low, the top (removable) disk is selected. When the level is high, the bottom (fixed) disk is selected.

The IESLR line, in conjunction with the logic levels on the Platter Select (IPSXR) and Head Select (IHSXR) lines, determine which disk is selected. Table 3-2 shows the line combinations necessary to select each disk.

Optionally, the thumbwheel Unit Select Switch on the disk drive control panel can be wired so that a quad-disk model can be made to appear as two dual-disk models. Similarly, two daisy-chained quad-disk models can be operated as four dual-disk models. Table 3-3 shows the Unit Select Switch positions and logic level combinations of the Platter Select, Head Select and Unit Select signals for the *Split Quad* option.

3.16.3 HEAD SELECT (IHSXR)

This level determines which head will be used on the selected disk as determined by the logic level combinations of IPSXR and IESLR shown in Table 3-2.

In split-quad disk models, a low condition on this line selects the top storage surface of the selected disk. When high, the line selects the bottom storage surface of the selected disk.

In quad-disk models, a low condition on this line selects head 0 and the top storage surface of the disk. When high, head 1 and the bottom storage surface are selected, as shown in Table 3-2. Heads for the remaining fixed disk surfaces are also selected as shown in Table 3-2.

3.16.4 CYLINDER ADDRESS STROBE

When the unit is selected and ready, this pulse causes the RESTORE INITIAL CYLINDER and CYLINDER DEMAND ADDRESS lines to be sampled. This will initiate a restore operation or a cylinder seek operation depending on the state of the RESTORE INITIAL CYLINDER line.

Table 3-2
Platter Selection

IPSXR Platter Select Line 1 Logic Level	IESLR Platter Select Extension Line 2 Logic Level	IHSXR Head Select Line Logic Level	Split-Quad Disk			Quad Disk		
			Disk	Storage Surface	Selected Head	Disk	Storage Surface	Selected Head
Low	High	Low	top (removable)	top	0	top (removable)	top	0
Low	High	High	top (removable)	bottom	1	top (removable)	bottom	1
High	High	Low	fixed bottom	top	2	fixed No. 1	top	2
High	High	High	fixed bottom	bottom	3	fixed No. 1	bottom	3
Low	Low	Low				fixed No. 2	top	4
Low	Low	High				fixed No. 2	bottom	5
High	Low	Low				fixed No. 3	top	6
High	Low	High				fixed No. 3	bottom	7

Table 3-3
Split Option Unit Select Switch/Signal Combinations

Interface Levels							Unit Select Switch on 1st Quad Unit	Unit Select Switch on 2nd Quad Unit	Selected Head
IPSXR	IESLR	IHSXR	IUS1R	IUS2R	IUS3R	IUS4R			
Low	X	Low	Low	High	Low	High	1	3	0
Low	X	High	Low	High	Low	High			1
High	X	Low	Low	High	Low	High			2
High	X	High	Low	High	Low	High			3
Low	X	Low	High	Low	High	Low	2	4	4
Low	X	High	High	Low	High	Low			5
High	X	Low	High	Low	High	Low			6
High	X	High	High	Low	High	Low			7

NOTE:
X = High or Low

For a restore operation, the CYLINDER DEMAND ADDRESS lines are ignored and the positioner will initialize at cylinder 000 (decimal).

For a seek operation, if a legal address is presented on the CYLINDER DEMAND ADDRESS lines, the positioner seeks the cylinder address specified by the states on these lines. If an illegal address is presented, then the positioner will not move and the illegal condition will be reported on the ILLEGAL CYLINDER ADDRESS line. The CYLINDER ADDRESS STROBE pulse must remain at the low logic level at least 0.5 μsec.

The action is initiated by the trailing edge (low-to-high transition) of the pulse. While there is no specific maximum time limit restriction on the pulse duration, it is usually desirable that the duration be not greater than 2 μsec.

The RESTORE INITIAL CYLINDER line must be in a stable state at least 0.5 μsec prior to the leading edge (high-to-low transition) of the pulse. It must remain in that state during the strobe and for at least 0.5 μsec after the trailing edge.

The CYLINDER DEMAND ADDRESS lines must be in a stable state at least 0.5 μsec prior to the trailing edge of the strobe. They must remain in that state during the trailing edge and for at least 0.5 μsec after the trailing edge of the strobe.

The BUSY SEEKING line will go low within 1.0 μsec after the leading edge of the strobe. If a strobe is issued to the disk drive when the positioner is executing a previous command (and the BUSY SEEKING line is low), the results will be as follows.

(1) The new operation will not be commenced.

(2) The operation currently in progress will continue to completion.

(3) An indication of illegal address will be given on the ILLEGAL CYLINDER ADDRESS line.

The CYLINDER ADDRESS STROBE should never be issued when the unit is selected and the BUSY SEEKING line is active.

3.16.5 CYLINDER DEMAND ADDRESS LINES (ICD0R—ICDER)

These lines specify the cylinder address for accessing a specific cylinder. The address is represented by the binary value with a low logic level corresponding to a binary one.

The most significant bit for 406 cylinder models is CYLINDER DEMAND ADDRESS EXTENSION, bit 256; the least significant bit for all models is CYLINDER DEMAND ADDRESS, bit 0. The decimal cylinder number may be expressed as the sum of the true bit weights as expressed by the bit number, e.g., CYLINDER DEMAND ADDRESS 6 has a bit weight of 64. The range of legal addresses for 406 cylinder models is from 000 through 405 (decimal).

3.16.6 RESTORE INITIAL CYLINDER (IRICR)

The state of this line when the CYLINDER ADDRESS STROBE is issued determines the type of positioning operation that will be performed.

Logic Level	Type of Operation Specified
Low	Restore position to initial cylinder (Cylinder 000)
High	Seek to cylinder specified by address

This line is used primarily in conjunction with bootstrap-loaded programs to obtain an effective address without having to actually specify a specific address. Another use is to re-initialize the positioner as a diagnostic check if a header disagreement has occurred.

3.16.7 WRITE ENABLE (IWEXR)

A low level on this line when the unit is selected and ready causes the write electronics to be conditioned for writing data (the read electronics are disabled). This signal simultaneously turns on write current in the selected head if the write protect condition does not exist and the positioner is not moving.

Data are written under control of the WRITE DATA SIGNAL line. Certain applications may require that all write data pulses be correctly recorded. Therefore, it is recommended that changes of state on the WRITE ENABLE line be accomplished when no data pulses are being transmitted on the WRITE DATA SIGNAL line. When the WRITE ENABLE line is at a high logic level, all write electronics are disabled.

3.16.8 ERASE ENABLE (IEEXR)

This is a level which, when low and the unit is selected and ready and a write protect condition does not exist and the positioner is not moving, allows erase current to flow in the selected erase head.

Erase must be enabled during any write operation. The erase current is disabled when the ERASE ENABLE line is at a high logic level.

The ERASE ENABLE line must be placed in the low state within 1 μsec after the WRITE ENABLE line is placed in the low state. When the WRITE ENABLE line is placed in the high state (any low-to-high change of state), the erase current must remain enabled for a period of time thereafter. The minimum time is defined as the minimum erase gap time (unless the Write Enable and Erase Enable lines are tied together).

NOTE

The erase current may remain enabled for a period of time greater than the minimum erase gap time.

3.16.9 WRITE DATA SIGNAL (IWDSR)

The bit-serial write data pulses on this line control the switching of the write current in the head. The write electronics must be conditioned for writing. For each high-to-low transition on the WRITE DATA SIGNAL line, a flux change will be produced at the write head gap. This will cause a flux change to be stored on the selected disk surface.

The double frequency encoding technique is used in which data and clock form the combined WRITE DATA SIGNAL. The repetition rate of the high-to-low transitions when writing all zeros is equal to the nominal data rate $\pm$ 0.25 percent. The repetition rate of the high-to-low transitions when writing all ones is equal to twice the $\pm$ 0.25 percent nominal data rate. The nominal data rate is listed in Table 1-1. It is recommended that the WRITE DATA SIGNAL be disabled at the controller when performing a Read operation to ensure optimum read-back performance.

3.16.10 ACTIVATE EMERGENCY UNLOAD (IAEUR)

This is a level or pulse which, when low for a period of at least 1.0 μsec, causes the drive to enter an Emergency Unload sequence. The write and erase currents (if any) will be disabled and the heads will be retracted and unloaded from the storage surfaces. The drive will revert to a not-ready condition within 5.0 μsec after recognition of the command, although unloading of the heads will not be completed this quickly.

As it is not necessary for a drive to be ready or selected in order to recognize the command, the command may be issued at any time. All drives on the common I/O bus will unload when the command is issued. When this command is a continuous low level, the drive is prevented from loading the heads.

The primary use of this line is the protection of the stored data in the event of power failure or other faults in the controller or computer. During such fault conditions, it may be impossible to maintain correct control of the interface for more than a few microseconds after the fault occurs or is detected.

Additionally, this line may be used to prevent the loading of the heads (and hence protection of stored data) before the software has properly initialized and gained correct control.

Residual data errors can be expected in a given track if ACTIVATE EMERGENCY UNLOAD is commanded while a write operation is in progress.

3.16.11 READ ENABLE (IREXR)

This is a level which, when low and the unit is selected and ready, enables the read electronics (READ DATA and READ CLOCK). After READ ENABLE is placed at the low logic level, the read electronics must detect one clock transition before any clock and data pulses may be transmitted, i.e., the first clock transition of preamble or gap will not be transmitted, but all others will be transmitted assuming the required conditions are met. This arrangement prevents pulses of less than normal duration from being transmitted.

When the READ ENABLE line is high, the read electronics outputs are immediately disabled and, if any data or clock pulses are in progress, these pulses will be shaved.

NOTE

It is recommended that the controller be designed such that the low-to-high transition of READ ENABLE is timed or caused by a clock pulse transition.

3.16.12 TRACK OFFSET (ITOPR AND ITOMR)

The TRACK OFFSET PLUS line and the TRACK OFFSET MINUS line provide a means of margin testing. When one of these lines is low and the unit is selected and ready, the heads are slightly offset from the normal track center. The direction of the offset is determined by the active line. An active direction is defined as being toward the disk center; a minus direction is defined as being away from the disk center. Table 3-4 defines the operational condition of the drive when the track offset function is used.

When either of the TRACK OFFSET lines is placed at a low logic level, the positioner requires 10 msec to seek the new position and to settle. A busy signal on the READY TO SEEK, READ OR WRITE line will not be given for TRACK OFFSET settling. The settling time for any TRACK OFFSET is in addition to seek time as indicated by the READY TO SEEK, READ OR WRITE line.

In general, the use of the TRACK OFFSET lines during a write operation is not recommended. Unless there is some means to guarantee that the entire track will later be erased (with the same offset control), then errors may be induced. TRACK OFFSET is non-functional during the first 20 minutes (approximately) of operation, starting with READY.

Prior to a read operation, the TRACK OFFSET lines should be conditioned for the type of operation desired. Assume a track of data has been previously recorded under normal conditions; the margin for recovery can be tested by reading and checking the data first with TRACK OFFSET PLUS, and then with TRACK OFFSET MINUS. If adequate margins exist, then all data will be correctly read.

When only one of the TRACK OFFSET lines is low during a Seek operation, the settling time for a Track Offset operation is in addition to the seek time as indicated on a BUSY SEEKING interface line. The settling time for a Track Offset operation cannot be overlapped with seek time.

Table 3-4
Track Offset Logic Levels

Track Offset Plus Line Logic Level	Track Offset Minus Line Logic Level	Operation Condition of Disk Drive
High	High	Normal operation with heads centered over track.
Low	High	Operation with heads offset in the plus direction.
High	Low	Operation with heads offset in the minus direction.
Low	Low	Operation with heads centered over track under control of offset lines and reduced read amplifier gain.

3.16.13 START/STOP DISK DRIVE (ISSDR)

This is a level which, when low and the following conditions and restrictions are met, allows the controller to start and stop the drive remotely. The function performed, and the resulting actions, depend on the condition of the drive at the time this line goes low. When the START/STOP DISK DRIVE line is held at a high logic level, or is not connected, the line has no effect on the operation of the drive.

Conditions and restrictions effecting this line are:

(1) This line is enabled at all times (unless the gated option is selected) regardless of the state of the UNIT SELECT lines. Therefore, all drives on the common I/O line may respond to this line.

(2) A low level on this line will cause the drive to commence a Start sequence if the drive is not already in a Run condition, or if the RUN/STOP switch/indicator is not depressed and none of the following inhibiting conditions exist.

- The disk cartridge is improperly inserted.
- Power is not applied.
- An internal emergency condition exists.

When used for commanding a Start operation, a pulse of not less than 260 μsec, or level change may be used.

(3) A low level on this line will cause the drive to enter a Stop sequence if the drive is in a Run condition and the RUN/STOP switch/indicator is not depressed. The sequence will be completed if the WRITE ENABLE and ERASE ENABLE interface signals are high.

(4) Since the START/STOP DISK DRIVE line performs the same function as the RUN/STOP switch/indicator, priority is by first actuation. If the START/STOP DISK DRIVE line is actuated continuously, the RUN/STOP switch/indicator is locked out during this period; conversely, if the RUN/STOP switch/indicator is depressed and held, the START/STOP DISK DRIVE line is locked out during this period.

3.17 INTERFACE OUTPUTS (DISK DRIVE-TO-CONTROLLER)

All signal names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface, with the low condition considered to be 0v and the high condition considered to be + 3v.

3.17.1 READY (IRXXD)

This is a level which, when low, indicates that the drive is in a Ready condition. If the unit is not in a Ready condition and is selected, the READY line will be at a high logic level. The

applicable indication on the READY line will become valid within 2 msec after a unit is selected. The indication will remain until either the unit status changes (the drive becomes Ready or loses Ready condition) or until it is de-selected.

The Ready condition is defined as that condition which exists when the following requirements are met.

(1) All power is applied and correct.

(2) A cartridge is correctly inserted.

(3) The disk is rotating at the correct speed.

(4) The heads are loaded.

(5) No equipment faults are detected.

(6) The logic is prepared to recognize commands.

3.17.2 BUSY SEEKING (IBS1D—IBS4D)

This group of four lines provide signals (on separate lines) indicating that the drive is busy seeking a new cylinder position. These lines do not require that the drive be selected in order to enable these signals) therefore, the current status is always indicated.

When the Unit Number Selector Switch is set to a given number, the corresponding BUSY SEEKING line number will be indicated.

When a BUSY SEEKING line is low, it indicates that the drive is executing or processing the previous operation commanded by CYLINDER ADDRESS STROBE. The appropriate line will go low within 1.0 μsec of the leading edge of any strobe that is recognized.

If the operation commanded does not result in positioner motion (illegal address or address same as current position) the line will go high within 2 μsec of the trailing edge of the strobe.

If the operation commanded results in a normal cylinder seek operation, the line will remain low for the duration of the cylinder seek time (defined as the time from the trailing edge of the strobe to the trailing edge of BUSY SEEKING). At the end of the Seek operation, the line will go high.

If the operation commanded results in a Restore operation, the line will remain true for a maximum of 3 seconds (specified time is from the trailing edge of the strobe to the trailing edge of BUSY SEEKING). At the end of the Restore operation, the line will go high.

The readiness of the drive to perform a read/write operation is inferred by a high level on the BUSY SEEKING line; however, the unit must also be selected and ready to execute a read/write operation.

3.17.3 SECTOR PULSE (ISPXD)

This line provides a signal which may be used for sectoring a disk. The signal consists of pulses at regular intervals during each revolution of the disk. These pulses, in essence, divide the disk (surface) into 'N' equal segments, where 'N' is the number of pulses.

For drive models that accept the 5440-type cartridge, the SECTOR PULSE line provides electronically generated pulses of a predetermined number derived from machined notches, or slots, located on the disk cartridge hub. This is known as mechanical sectoring. The number is specified at the time of order. This may be readily changed in the field by plugging in a different programming-array plug. This plug configures the drive to electronically generate a specific number of sector pulses. The number of electronically generated sector pulses for the fixed disk is also determined by a plug-in array.

For drives that accept the 2315-type cartridge, the SECTOR PULSE line provides pulses derived from the machined slots located on the sector ring on the cartridge. One pulse for each sector slot will be issued (this applies only to the removable disk). In some applications, it may be desirable to utilize electronically generated sector pulses in lieu of the mechanical sectoring by the 2315-type cartridge sector ring. This can be configured by plugging in the appropriate programming-array plug. The sector pulses for the removable disk will then be similar to the arrangement described previously for the 5440-type cartridge. The number of sector pulses for the fixed disk is also determined by a plug-in array.

In all cases, the pulses on the SECTOR PULSE line correspond only to the respective disk as selected by the PLATTER SELECT and PLATTER SELECT EXTENSION lines. This is accomplished by a multiplexer internal to the drive. The number of sector pulses that may be accommodated by the electronically generated sectoring are listed in Table 1-4.

The duration of any sector pulse is 8 ± 2 μsec. The SECTOR PULSE line is low during the pulse; at all other times the line is high. If a unit is selected at the moment a sector pulse is in progress, that pulse duration will be shortened, i.e., the pulse will be shaved an indeterminate amount. This will have the effect of introducing a time uncertainty (instantaneous jitter) for the shaved pulse.

If a *cold* cartridge is inserted into a *warm* drive and the unit reaches a Ready condition, for 20 minutes thereafter, each time the cartridge is selected or deselected, the sector pulse will be blanked for 10 msec. This allows for sufficient time for transient temperature compensation of the positioner servo.

3.17.4 SECTOR COUNT LINES (ISC0—ISC6D)

These seven lines specify the sector address presented in binary format. This address indicates the particular segment of the disk surface currently under the read/write heads. The signals on these lines are, in essence, the status of a binary counter. In all cases, the address presented corresponds only to the respective disk as selected by the PLATTER SELECT and PLATTER SELECT EXTENSION lines. This is accomplished through the use of separate counters multiplexed internal to the drive.

The sector address is represented by the binary value with a low level corresponding to a binary one. The most significant bit is number 64; the least significant bit is number 1. The decimal sector number may be expressed as the sum of the *true* bit weights as expressed by the bit number, e.g., SECTOR COUNT 4 has the bit weight of 16.

The signals on the SECTOR COUNT lines will change state 2.4 ± 2.6 μsec prior to the leading edge of the SECTOR PULSE pulse (assuming non-shaved pulses).

The SECTOR PULSE pulse immediately following an INDEX PULSE defines the beginning of SECTOR COUNT 0, and at the time of this SECTOR PULSE, the SECTOR COUNT lines present a zero value. Thereafter, the value will be incremented until the maximum count is achieved. The maximum count that will occur is (N – 1) where 'N' is the number of Sector Pulses. This is determined by the particular configuration as described under SECTOR PULSE (Paragraph 3.17.3).

3.17.5 INDEX PULSE (IIPXD)

This is a pulse which occurs once per disk revolution and is used to define the sector reference (sector zero). The pulse will always occur during the sector just prior to Sector Count Bit 1, i.e., during sector N – 1, where 'N' is the maximum number of sectors.

The duration of the index pulse is 10.4 ± 3.0 μsec. The INDEX PULSE line will be at the low logic level for the duration of the pulse. At all other times, the line will be high. If a unit is selected at the moment that an index pulse is in progress, that pulse duration will be shortened, i.e., the pulse will be shaved an indeterminate amount.

In all cases, the pulse on the INDEX PULSE line corresponds only to the respective disk as selected by the PLATTER SELECT and PLATTER SELECT EXTENSION lines. This is accomplished by a multiplexer internal to the drive. The INDEX PULSE will be unconditionally discontinued for 10 msec when there is a change in disk selection between cartridge and fixed disk(s) during the 20 minutes of operation following a Start sequence.

3.17.6 ILLEGAL CYLINDER ADDRESS (IICAD)

This is a level which, when low, indicates that an illegal cylinder address was detected during the last CYLINDER ADDRESS STROBE.

The line will go low within 1.0 μ sec after the trailing edge of the strobe only when an illegal condition is detected. The line will go high within 1.0 μsec of the leading edge of the strobe if the line is not already high at the time of the strobe. These actions will take place only if the strobe is recognized. The unit must be selected and ready in order to recognize the strobe.

An illegal condition will be indicated for either or both of the following.

(1) The cylinder address specified at the time of the strobe exceeds the range of legal addresses for that particular model of drive.

(2) A strobe is issued to the drive while it is busy seeking.

The following actions will clear (or prevent) an illegal address indication.

(1) An address within the legal range is present with the strobe.

(2) A Restore Initial Cylinder operation is commanded.

(3) The drive becomes not-ready as the result of an operator-initiated Unload or Emergency Unload operation.

3.17.7 READ CLOCK (IRCXD)

This is a pulse which goes low at the beginning of a new bit cell during a read operation. The leading edge of this pulse defines the beginning of a new (next) bit cell. The line will be at the low logic level during the time of the pulse.

During a portion of each bit-cell time, the READ CLOCK line will be placed high and remain in this state until the next bit-cell time is to be defined by a pulse leading edge. This line is utilized to establish a timing reference for interpreting pulses on the READ DATA line.

3.17.8 READ DATA (IRDXD)

The signals on this line define the content of the data read during a Read operation. The signal consists of a pulse for each *logic one* bit read from the disk. The line will be low during the time of the pulse and high for each *logic-zero* bit read from the disk; the pulsewidth is the same as Read Clock pulsewidth.

The timing of pulses on this line is relative to the READ CLOCK line. The relative timing is such that a *logic one* bit is interpreted if the READ DATA line is low at any time when the READ CLOCK line is high between consecutive pulses on the READ CLOCK line.

3.17.9 FILE PROTECTED (IFPXD)

The level on this line indicates the selected platter is protected from a Write operation. When the FILE PROTECTED line is low, it indicates that the drive will not perform a Write or Erase operation regardless of a command on the WRITE ENABLE or ERASE ENABLE lines; when the FILE PROTECTED line is high, it indicates that the selected platter is not protected and data may be written.

Write protection for the removable cartridge or fixed disk(s) may be selected by the operator from the interface. Changes of state on this line, as applicable, will occur within 1.0 msec of a platter select change (assuming the unit is selected). It is recommended that the controller test the state of this line prior to attempting a Write operation.

3.17.10 MALFUNCTION DETECTED (IMDXD)

This is a pulse which, when low, indicates detection of one of the following malfunctions.

(1) Loss of ac or dc power.
(2) Disk speed does not remain within tolerance.
(3) Positioner error is detected.
(4) Write current faults that could affect stored data.

Any of the above items necessitates unloading the heads, and the drive will commence an emergency unload sequence coincident with the trailing edge of the malfunction pulse; duration of the pulse is between 0.2 and 2.0 msec.

Any drive on the I/O bus can pulse this line regardless of whether or not it is selected. The line will not be pulsed if the malfunction is detected before the drive achieves a Ready condition. The drive will become not-ready within 5.0 msec after the leading edge of the pulse on the MALFUNCTION DETECTED line. Software diagnostics can determine which drive has detected a malfunction by selecting one drive at a time, determining its ready status, and comparing the results with the previous status.

The time between pulses in a group may become arbitrarily small, as all drives on the I/O bus could pulse the MALFUNCTION DETECTED line asynchronously and independently. In the case of power failures, etc., the pulses may overlap or occur simultaneously.

NOTE

It is recommended that the leading edge of a malfunction pulse be used to initiate diagnostic action and that once the condition has been flagged, additional pulses can be disregarded until after the flag is cleared. The flag need not be cleared before diagnostic action is commenced.

3.17.11 DUAL PLATTER DRIVE (IDPDD)

A low logic level on this line indicates that the drive is a split quad-disk drive. A valid level will exist on the line whenever the particular drive is selected, regardless of whether the particular drive is ready or not.

Logic Level	Type of Disk Drive Indicated	Number of Platters
Low	Split Quad	(2 fixed) + (2 fixed and 1 removable)

This line may be used by the controller or formatter to determine, in advance, the legal number of storage surfaces available in a specific drive. This allows utilization of different model drives on a common Input/Output bus. The DUAL PLATTER DRIVE Line, if not used, may be left open on the interface.

3.17.12 QUAD PLATTER DRIVE (IQPDD)

The logic level on this line indicates whether or not the drive is a quad-disk drive. A valid level exists on the line whenever the particular drive is selected, regardless of whether the drive is ready or not.

Logic Level	Type of Disk Drive Indicated	Number of Platters
Low	Quad disk; one removable, three fixed	4

This line may be used by the controller or formatter to determine in advance the range of legal addresses that a specific drive can accommodate. This allows utilization of different model drives on a common I/O bus.

3.17.13 DOUBLE TRACK DRIVE (IDTDD)

The logic level on this line indicates the number of usable cylinders that the drive is capable of accessing. A valid level exists on the line whenever the particular drive is selected, regardless of whether the drive is ready or not.

Logic Level	Number of Cylinders	Corresponding Tracks per Inch
Low	406	200

This line may be used by the controller or formatter to determine in advance the range of legal addresses that a specific drive can accommodate. This allows utilization of different model drives on a common I/O bus.

3.17.14 SPECIAL INTERFACE SIGNAL

The function of this line is selected by customer option. It is conditioned by anyone of the UNIT SELECT lines and, when low, may represent any of the following conditions.

(1) SAFE — The SPECIAL INTERFACE SIGNAL will be at a high logic level whenever the requirements for Safe condition are met.

(2) RUN — Whenever this signal is at a high logic level, the drive is in a Start sequence, or in a Ready condition.

The SPECIAL INTERFACE SIGNAL may also be maintained at a permanent high logic level if none of the above signals are required.

3.17.15 TERMINATION VOLTAGE

This is power supply voltage output which may be used by the controller when the single-resistor-type interface line termination is used. The maximum current to be drawn is 800 milliamps.

The voltage must be 3.5v dc $^{+\ 0.6v\ dc}_{-\ 1.0v\ dc}$ or 4.3v dc $^{+\ 0.7v\ dc}_{-\ 1.0v\ dc}$ or 5.0v dc $\pm$ 0.25v dc optionally.

Decoupling capacitors must be used at the controller. These capacitors should be connected between the Termination Voltage and digital ground. It is recommended that at least three 1.0 mfd low-inductance capacitors be connected in parallel. These should be located in close proximity to the termination resistors. A minimum of two conductors should be utilized in the cable to transmit the voltage.

Termination voltage may optionally be supplied by the controller. In this case, the voltage is fed through each drive in a daisy chain so that it is available to the drives that follow. Additionally, drive-supplied termination voltage of 3.5v, 4.3v, or 5.0v may be connected to the Termination Voltage line through diodes to provide backup voltage in the event of controller termination voltage failure.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the D3000 Disk Drive theory of operation. The disk drive consists of the mechanical and electrical components necessary to record and read digital data recorded on a magnetic disk. The drive consists of the following major groups.

(1) Main chassis group
(2) Positioner assembly
(3) Power supply assembly
(4) Read/Write PCBA
(5) Servo PCBA
(6) Logic PCBA
(7) Temperature Compensation PCBA

4.2 ORGANIZATION OF THE DISK DRIVE

Figure 4-1 is a block diagram illustrating the overall organization of the disk drive. This organization can be subdivided into the mechanical and electrical/electronics group. The mechanical group can be further divided into the main chassis group and the positioner assembly group.

4.2.1 MAIN CHASSIS GROUP

The main chassis group consists of the following components and assemblies.

(1) Base casting
(2) Air system filter and blower
(3) Spindle assembly
(4) Drive motor
(5) Drive train components
(6) Cartridge adapter (top load models)
(7) Receiver assembly (front load models)
(8) Lower disks cover (top load models)
(9) Lower disks cover (front load models)
(10) Bezel assembly
(11) Dust cover
(12) Control switch and indicator group

The main mechanical element of the drive is the base casting. It is a machined aluminum alloy casting which is the supporting structure for all of the components in the drive. When rack mounting the drive, the rack mounting slides are mounted directly to the sides of the base casting. This provides a means of sliding the unit in and out of rack installations.

The absolute filter and high efficiency blower are components of the air system and are mounted in the base casting. Duct work, either integral with the base casting or formed by suitable cover plates, provides the means for channeling the filtered air into the area of the disks and heads. Operational characteristics of the *flying head* type of magnetic head employed in the drive require that the air bearing formed between the head and the disk

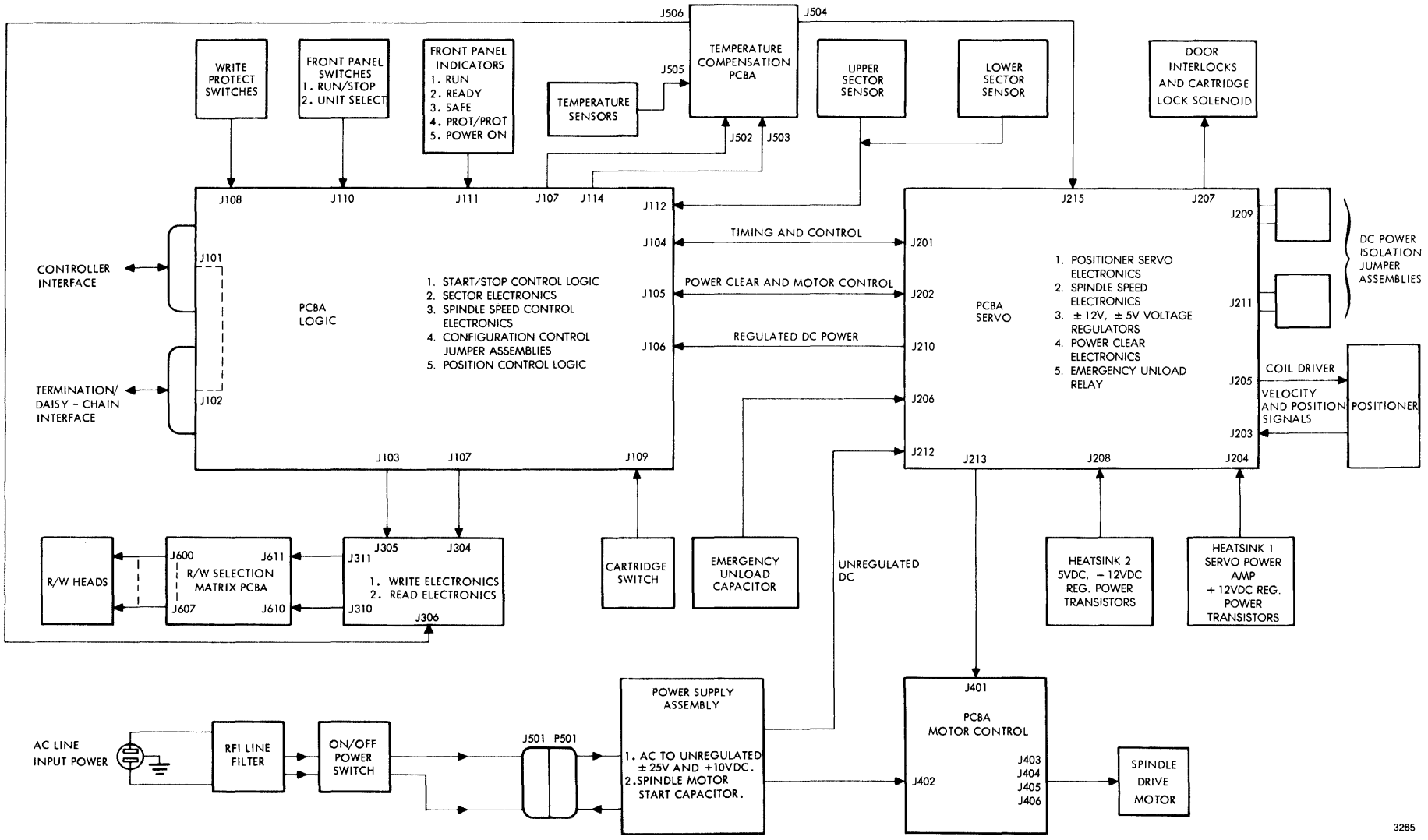


Figure 4-1. D3000 Disk Drive Organization

surface be relatively free of particle contamination. Therefore, the filtered air flow provided by the air system causes a continual flow of clean air to purge this area of the disks and ensure correct operation of this air bearing. The air cushion that causes the heads to fly above the surface of the disk is dependent only upon the surface velocity of the disk and not upon the air flow through the filter. A fan at the rear of the drive exhausts the heat generated by the heatsinks and cools the surfaces of the adjacent PCBAs.

The spindle assembly mounts into the base casting and provides the central axis of rotation for the disks. This spindle is a precision machined assembly utilizing ball bearings which are pre-loaded to provide a runout of less than several hundred microinches. The assembly contains the phase lock ring which is used for sectoring the lower fixed disks and for the spindle speed control. It also provides a mounting location for the lower fixed disks in both quad-disk and split-quad disk drives. A permanent magnet clutch, used to engage the hub of the removable cartridge, is mounted on top of the spindle hub. A precision ground cone is on top of the spindle hub which accurately centers the cartridge hub. The hub of the spindle assembly acts as an air pump to pump the filtered air into the cartridge area.

The drive motor is mounted on a mounting plate which, in turn, is mounted to the base casting. The drive motor provides the power to rotate the disks at the prescribed speed and drive the blower in the air system. This motor is a multiple winding, permanent split phase induction motor which is used to drive the spindle and blower through a belt drive system. The drive train components consist of the pulleys at the spindle, blower shaft, motor, and tension idler. The necessity for a belt tension adjustment is avoided by spring-loading the tension idler to maintain a constant belt tension.

The design of the D3000 drive provides maximum commonality of mechanical components between top and front load models. The major difference between top and front load machines is in that area which receives or adapts the cartridge to the drive.

In top load models, the cartridge, which is plastic injection molded, mounts to the top of the base casting. Mounted on this adapter is the cartridge lock mechanism with an arm that pivots out over the top of the cartridge dust cover. The position of this arm is sensed with a snap-action switch. The arm can be locked or unlocked by a solenoid arrangement fitted to the adapter.

In front load models, a receiver assembly is fitted to the top of the base casting and is pivoted from supports attached to the base casting. This arrangement provides a mechanism for properly locating the cartridge in the drive. It is also the mechanism for disengaging the cartridge hub from the magnetic clutch on the spindle. A link arm which is integral with the bezel assembly provides the camming action to disengage the cartridge hub from the magnetic clutch.

Also, on front load models, a lower disk cover supports the magnetic transducer and photoelectric sensor pickups and provides a covering for the lower disks. The analogous component in top load models is the disk cover which is an aluminum alloy separator mounted in the cartridge adapter just above the lower disks. The bezel assembly provides the decorative trim at the front of the drive and a suitable cover for the air system intake. In addition, for front load models, the mounting arrangement for the door and the link arms provide the camming action for the receiver.

A dust cover of formed metal is used to cover the drive and protect it from contamination. This cover is held in place by machine screws on both top and front load models. The cover directs the air flow through the interior of the drive.

The ON/OFF power switch, RUN/STOP switch, and the indicators are mounted to the base casting by the use of a bracket located directly behind the bezel. On top load models, the bezel may be removed without disturbing the operator switches or the wiring since there is no mechanical connection between the bezel and the switch bracket.

4.2.2 POSITIONER ASSEMBLY

The positioner assembly is a separate modular unit that is mounted on the base casting. Also mounted on the base casting are the positioner magnetic structure, and the shaft for supporting the carriage. The carriage is supported on a bearing structure riding on this shaft. The read/write heads are mounted in the carriage.

Also attached to the carriage is the positioner coil. This arrangement of magnet and coil provides a linear motor actuator for positioning the read/write heads. This type of arrangement is also referred to as a voice coil positioner. Carriage velocity is determined by the velocity signal which is derived electrically from the positioner signal. The position of the carriage is detected and sensed using a photoelectric position transducer which is attached to the positioner baseplate by a mounting strip.

All models have two temperature sensing elements. These thermistors are part of the temperature compensation circuitry. One senses surface temperature of the removable disk as it spins, the other senses the temperature of the topmost fixed disk area.

4.2.3 POWER SUPPLY ASSEMBLY

The power supply assembly is a major subassembly contained on a steel plate which mounts to the underside of the base casting and includes the power transformer, rectifiers, and filter capacitors. The Motor Control PCBA is mounted on top of the power transformer which protrudes from a well in the base casting. This PCBA is protected by a removable hard plastic cover.

4.2.4 READ/WRITE, READ/WRITE SELECTION MATRIX, SERVO, AND LOGIC PCBAS

The partitioning of the electronics system is primarily functional. The four major PCBAs constitute the major partitioning of the D3000 electronics. These are the Read/Write, Read/Write Selection Matrix, Servo, and Logic PCBAs. In addition to the functional descriptions contained in this section, detailed descriptions of these PCBAs are contained in Section V.

The electrical and electronic components comprising the main chassis group, the positioner assembly, and the power supply chassis are interconnected with the PCBAs through use of interconnecting cable assemblies. The Read/Write PCBA is located adjacent to the positioner assembly and is constrained by card guides. One of the card guides mounts to the Read/Write Selection Matrix PCBA which is 90 degrees to the Read/Write PCBA. The Read/Write Selection Matrix PCBA also straddles the moving head and carriage assembly. The head cables connect directly to this board. The Logic PCBA is mounted on pivoting supports which are mounted directly to the base casting. Hinged on the face of the Logic PCBA is the Servo PCBA; these PCBAs are interconnected by interboard flat cables.

4.2.5 TEMPERATURE COMPENSATION PCBA

The temperature compensation assembly is comprised of a Temperature Compensation PCBA and two thermistor assemblies which sense ambient temperatures of the removable and fixed disk(s). This PCBA mounts beside the Read/Write PCBA into card guides located on the power supply chassis.

4.3 FUNCTIONAL SUBSYSTEMS

The major functional groups of the drive are illustrated in Figure 1-4; these major groups, functionally discussed in the following paragraphs, are:

(1) Positioner and Positioner Electronics
(2) Read/Write Electronics
(3) Read/Write Selection Matrix
(4) Disk Drive Function Control
(5) Spindle Speed Control
(6) Position Control Logic
(7) Sector Electronics
(8) Motor Control
(9) Power Supply
(10) Temperature Compensation

4.4 POSITIONER AND POSITIONER ELECTRONICS

An essential function in a moving head disk drive is the positioning of the read/write head at the correct cylinder. This is accomplished in the D3000 Disk Drive by the Positioner Servo Electronics and the Positioner Assembly.

4.4.1 POSITIONER ASSEMBLY

The Positioner Coil and Moving Mass (linear motor) and Position Transducer are the two major functional entities which comprise the Positioner Assembly. Figure 4-2* shows the relationship of these subsystems to the Positioner Servo Analog Circuits and the Positioner Control Logic.

The linear motor consists of a stationary permanent magnet and a positioner coil attached to the moving-mass, i.e., the carriage and magnetic head assembly. A description of the physical arrangement of the Positioner is contained in Paragraph 4.2.2.

Functionally, the magnet structure and the ways that the carriage rides on are the stationary portion of the linear motor. The moving structure consists of the carriage, the positioner coil, the heads mounted into the carriage, the bearings which support the carriage on the ways, and the Position Transducer. The force that is necessary to move the moving-mass portion of the positioner is a function of the inter-reaction of the magnetic fields produced by the permanent magnet structure and the magnetic field resulting from the current in the positioner coil. This force may be used for accelerating or decelerating the moving-mass, or as a restoring force for holding the moving-mass in a given position. To a first approximation, the force developed is proportional to the current in the positioner coil.

The speed of the positioner carriage movement is controlled by a velocity signal which is derived electrically from the position signal.

The Position Transducer is a photoelectric sensor that develops four electrical signals, each serving a specific function for use in controlling the positioner. An incandescent lamp, mounted in the position transducer body, supplies illumination to a group of photodiodes located opposite the lamp. The transducer body is mounted stationary to the positioner baseplate by the use of a mounting strip.

*Foldout drawing, see end of this section.

Attached to the carriage is a precision scale which is part of the moving-mass. This scale is interposed between the lamp and the photodiodes and consists of opaque and transparent areas in specific patterns. Interposed between the scale and the photodiodes is a precision reticle which is also made up of opaque and transparent areas in specific patterns. The combination of the reticule patterns and the scale patterns are used to control the amount of illumination reaching the photodiode group.

Two of the signals developed by the Position Transducer as a function of carriage position are level change type of signals. One signal, Heads Retracted, changes state when the carriage is approximately ¼-inch from the fully retracted position and is used to indicate the gross carriage position, specifically, the retracted position of the heads. The other signal, Position Transducer Index, is used to define the legal range of the carriage position. This signal is a multi-change-of-state signal. One of the transitions of this signal is used in the initialization process during a head loading operation.

The other two signals derived from the Position Transducer are referred to as X + 0 and X + 90. These signals are linear signals that are cyclic as a function of cylinder position, and bi-polar in terms of polarity. They are displaced in electrical phase by approximately 90 degrees.

All of the signals from the Position Transducer are current signals proportional in amplitude to the illumination of the specific photodiode associated with that signal. The X + 0 and X + 90 signals are actually derived from photodiode pairs rather than a single photodiode.

4.4.2 POSITIONER ELECTRONICS

The Positioner Electronics consists of two major groups: the Position Control Logic and the Positioner Servo Analog Circuitry. The relationship of these subsystems to the Linear Motor and Position Transducer is shown in Figure 4-2. The entire arrangement comprises a servo mechanism which controls the mechanical position of the carriage and the position of the heads.

The servo mechanism may be operated in one of two modes, a Position Mode where the position of the carriage is controlled, or the Velocity Mode where the velocity of the carriage is controlled. The servo is switched between the Position Mode and Velocity Mode, or vice versa, by means of transistor switches which are controlled by the Position Control Logic. The Position Control Logic determines the specific mode of operation on the basis of commands input to it from the interface and the status of the signals derived from the Position Transducer.

Additionally, as shown in Figure 4-2, the Linear Motor can be disconnected from the servo and operated by the Emergency Unload Driver on the Temperature Compensation PCBA and powered by the Emergency Unload Capacitor in a manner which controls the retracting velocity of the positioner. This emergency unload system provides a means of independently supplying power to the Linear Motor during emergency situations. This network is independent of the servo electronics for purposes of retraction of the heads from the storage surface during emergencies. The Emergency Unload Relay acts as a double-pole, double-throw switch, to connect the Positioner Coil to either the output of the Power Amplifier and the Current Sensor, or to the Emergency Unload system. Additionally, a dynamic brake is provided on the Servo PCBA to further control the motion of the positioner during emergencies. The brake is activated for several milliseconds after the emergency has been detected and until the Emergency Unload Relay drops out.

The Emergency Unload Relay Driver receives its commands from the Logic PCBA via the Emergency Unload Enable (LEUEG) line. When the Emergency Unload Relay is energized, the positioner coil is connected to the servo; specifically, it is connected to the output of the Power Amplifier and to the Current Sensor. The Power Amplifier, in conjunction with this Current Sensor, forms a voltage-to-current converter providing a current in the positioner coil that is proportional to the applied input voltage to the Power Amplifier. As previously mentioned, the available force for moving the carriage is proportional to the positioner coil current to a first approximation, and the Power Amplifier, being a voltage-to-current converter, provides a current that is proportional to its input voltage.

Therefore, the output of the Summing Amplifier, which is the input to the Power Amplifier, determines the force applied to the carriage where the force is approximately proportional to the output voltage of the Summing Amplifier.

The Summing Amplifier input is the major summing junction of the servo. Applied to this Summing Amplifier are the servo commands and the feedback which nulls these commands. Therefore, the servo loop functions to reduce the voltage at the Summing Amplifier input by providing an output voltage which results in a feedback signal which nulls the command signal. Additionally, the resultant of two temperature compensation signals are applied to this summing junction.

One of the input commands to the Summing Amplifier is the velocity reference. The velocity reference command is a request for a specific velocity when the loop is operating in the fast velocity mode. This velocity reference is derived from the Velocity Reference Circuit. The polarity of this reference is determined by the network following the Forward Direction signal (LFDX1) applied to J201, pin 21 (page 2, zone C6). This network consists of U42, U40, Q11, and Q10 on the Servo PCBA (Schematic No. 108130).

The Velocity Reference Circuit is a digital-to-analog converter which has a single polarity output. The address difference input is a digital signal that is the binary representation of the difference between the demand address from the interface and the current address defining the current positioner position. The output of the Velocity Reference Circuit is an analog voltage representative of the address difference. Therefore, the specific velocity requested is a function of the distance to be traveled in achieving the demand address.

The address difference is specified on the Address Difference lines in binary form where NLAD0G is the least significant bit and NLADEG is the most significant bit. The decimal address difference number may be expressed as the sum of the active bit weights, each address difference being assigned a specific bit weight. The bit weights are ascending powers of two, where bit number 0 is decimal bit weight number 1; bit number 1 is decimal bit weight number 2; bit number 2 is decimal bit weight number 4, etc., to the extension bit number where the bit weight is 256. The address difference as specified on the Address Difference lines determines the magnitude of the velocity reference generated by the Velocity Reference Circuit.

Referring to the Servo PCBA, Schematic No. 108130, it can be seen that the Velocity Reference Circuit portion of the velocity function decoder/encoder consists of U40, U39, and U44. The remainder of the Velocity Reference Circuit is the digital-to-analog conversion arrangement consisting of a resistor network, a current-to-voltage converter, and diode switches. The purpose of this arrangement is to take the digital signal encoded by the velocity function decoder/encoder and convert it into a current of a specific value which is then applied to the current-to-voltage converter. The summing junction of U30 (zone G3 on the Servo PCBA) functions as a current-to-voltage converter producing a voltage level which is determined by the address difference value. The resistor network is R40, and R47 through R53. The diode switches are CR5 through CR18. The current-to-voltage converter consists of U30 in conjunction with Q9.

Referring to Figure 4-2, the output magnitude of the Velocity Reference Circuit is the velocity reference which is utilized during seeks. This reference is determined by the address difference value. The polarity of the velocity reference which determines the direction of the velocity is controlled by a polarity select network controlled by the Forward Direction (LFDX1) line from the Position Control Logic. The Transistor Switch, which switches the velocity reference to the Summing Amplifier, is controlled by the Velocity Reference Enable (NLVREG) line from the Position Control Logic. When the positioner is executing a high-speed seek and is not operating as a position servo, NLVREG will be active, thereby switching to the velocity reference from the Velocity Reference Circuit.

Other commands which may be applied to the input of the Summing Amplifier are for controlling the positioner in the Slow Velocity mode, i.e., during loading and unloading of the heads. The Slow Velocity mode is also used when executing a Restore operation. The Slow Velocity mode is determined by two logic signals, Forward Slow Mode (NLFSM1) and Reverse Slow Mode (NLRSM1).

The two slow mode control signals, NLFSM1 and NLRSM1, are developed by the Position Control Logic and control transistor switches in the Mode Control Circuits which establish the Slow Mode velocity reference.

Additionally, command signals Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) from the Position Control Logic can be used to determine position mode offset through the use of position reference voltages derived in the Mode Control Circuits. The track offset function is employed in the position mode for diagnostic purposes. The two logic signals, NLTOPG and NLTOMG, operate transistor switches in the Mode Control Circuits to generate a position mode reference, thereby offsetting the heads from the nominal track centerline.

Referring to the Servo PCBA, Schematic 108130, it can be seen that NLTOPG, in conjunction with R101 and R102, determines the magnitude of the Track Offset Plus position reference. Likewise, NLTOMG, in conjunction with R107 and R108, determines the Track Offset Minus position reference.

In addition to the commands controlled by logic signals that may be input to the main summing junction, an offset correction may be introduced by the Servo Offset Adjust, R146 (zone G7) on the Servo PCBA. There is also an external input test point provided to enable the introduction of external test signals into the summing amplifier. TP11 and R143 on the Servo PCBA perform this function.

Two separate and distinct feedback paths to the main summing junction are provided. One of these feedback loops is closed at all times when the servo is energized. This path, as shown in Figure 4-2, is from the Position Transducer, through the Velocity Synthesizer, to the Summing Amplifier input. This feedback is switched on by a transistor switch which is disabled by the Position Mode signal (LPMXG), and is used to null velocity commands.

The other feedback path is used only in the Position mode. This path takes the X + 0 signal from the Position Transducer, conditions it to a voltage signal in the Position Transducer Amplifiers, and then switches it to the Summing Amplifier input. The transistor switch on the Servo PCBA performs the switching function and is controlled by LPMXG from the Position Control Logic. Another transistor switch feeds a derivative of the Position Mode signal into the Summing Amplifier in order to provide damping for the servo loop.

As previously discussed, four signals are provided to the Position Control Logic which are derived from Position Transducer signals. These four signals are the X + 0, X + 90, Heads

Retracted, and Position Transducer Index. They are converted from current signals into voltage signals by current-to-voltage converters that are contained in the Position Transducer Amplifiers. These current-to-voltage converters are U38, U37, U34, and U33 located on the Servo PCBA.

Since the output of the Position Transducer Amplifiers are an analog voltage and therefore unsuitable for direct application to logic, they are converted into digital signals by analog-to-digital converters. These converters are, in essence, a special type of Schmitt trigger and are comprised of U19 and U20 on the Servo PCBA. The signals which are fed back to the Position Control Logic are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Heads Retracted (SHRXG), and Position Transducer Index (SPTIG). These signals are utilized by the Position Control Logic to determine the operation of the positioner servo in conjunction with commands from other parts of the logic and the I/O interface.

Additionally, failure of the lamp in the Position Transducer is detected by the Lamp Failure Detector. A signal derived from this detector is fed back to the Position Control Logic for determining when an emergency condition exists. This signal is Position Transducer Failure (SPTFG).

4.5 READ/WRITE OPERATIONS

The double frequency recording method is used in reading and writing data in the D3000 Disk Drive. Read/Write operations are accomplished by a read/write head. During a Write operation, a bit is recorded on the disk whenever the coils of the read/write head are switched by the Write Driver circuits. During a Read operation, a clock or data bit is sensed on the disk whenever the flux direction induced by the coil winding is reversed as a result of a change in polarity of the flux pattern presently passing under the head gap.

4.5.1 DOUBLE FREQUENCY RECORDING

A basic clock frequency signal is encoded in the data pulses to produce a single composite signal at the read/write head. The composite signal represents either a logic zero bit condition or a logic one bit condition for each bit-cell time defined by the clock.

The double frequency method, shown in Figure 4-3, makes use of a clock frequency to establish the basic bit-cell timing cycle. The insertion of a data pulse between clock pulses in a bit-cell period produces a composite Read/Write signal which uses only clock pulses for a logic zero bit indication, and data pulses for a logic one bit indication. A zero bit-cell (clock pulses only) produces a single change in direction of the flux pattern. A one bit-cell (data pulse located between two clock pulses) produces a double change in direction of the flux pattern. In either case, the clock signal causes a change in direction of magnetism from plus to minus or minus to plus polarity, thus causing the storage of a bit. Because both clock and data information are synchronized on a composite signal, double frequency recording is sometimes referred to as *self-clocking*.

In double-frequency recording, a clock bit is always inserted at the beginning of each bit-cell time to establish the basic recording frequency. A data bit is inserted between clock bits (at twice the frequency) so that the data bit results in two flux reversals within a single bit-cell time. If the data bit is not present, a single flux reversal occurs in a bit-cell time.

The recording head is a split-ring core containing coil windings so that a magnetic field with a given flux direction prevails at the core gap while the coil is energized. When current flows through the coil, the flux induced in the core establishes a fringe flux at the gap. As a magnetic recording surface passes by the gap, the fringe flux magnetizes the surface of the disk.

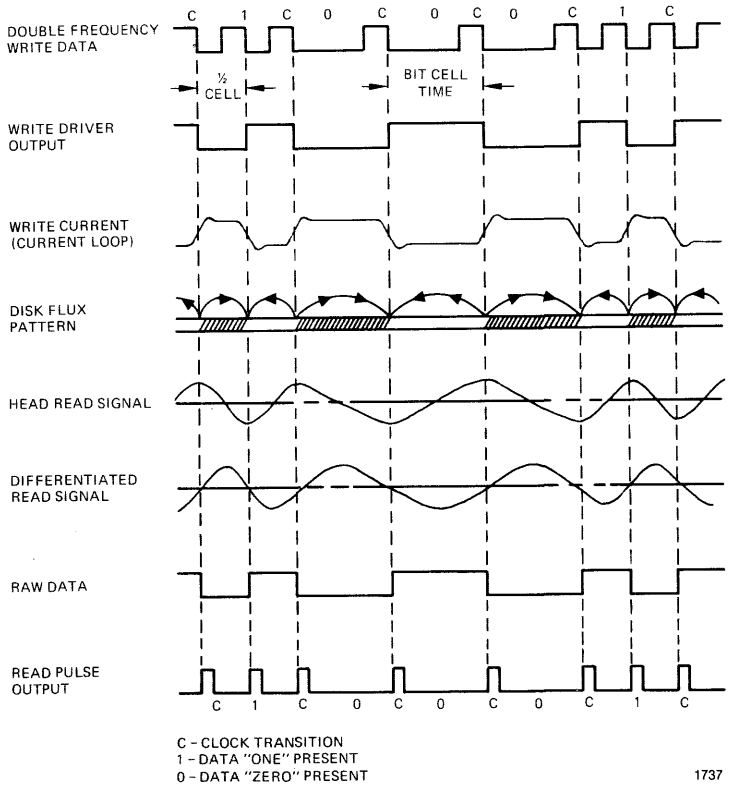


Figure 4-3. Double Frequency Recording Flux and Pulse Relationship

During a Write operation, a bit is recorded when the flux direction in the core is reversed by switching between coils of the read/write head. The fringe flux is reversed at the gap and, hence, the portion of the flux flowing through the recording medium is reversed. If the flux reversal is considered instantaneous in comparison to the motion of the recording surface, and the gap is observed at the moment of reversal, it can be seen that the portion of the surface that just passed the gap is magnetized in one horizontal direction while the portion directly under the gap is magnetized in the opposite direction. Between these two areas, the flux must reverse 180 degrees; this recorded flux reversal represents a bit.

During a Read operation, the gap first passes over an area that is magnetized in one horizontal direction, and a constant flux is induced into the core and the coil. The coil provides no instantaneous output voltage for this condition. However, when the recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux induced into the core and coil must go through a 180-degree reversal. This reversal means that the coil sees a change in flux which results in a voltage output pulse.

4.6 READ/WRITE ELECTRONICS

The Read/Write Electronics are contained on two printed circuit board assemblies, the Read/Write PCBA and the Read/Write Selection Matrix PCBA, which operate in consort with each other. Figure 4-4* is a functional block diagram of the D3000 read/write system and should be referred to for the following discussion.

*Foldout drawing, see end of this section.

4.6.1 HEAD SELECT

Head selection in the D3000 is accomplished by signals from the using system via the Platter Select (IPSXR), Platter Select Extension (IESLR), and Head Select (IHSXR) I/O interface lines. The signals on these lines are required to select one of eight read/write heads. Table 3-1 shows the head select decoding used in the D3000 disk drive.

4.6.2 WRITE ELECTRONICS

Information to be recorded is supplied to the drive via the Write Data Signal (IWDSR) I/O interface line. The writing process is under complete control of the logic functions and control circuitry (Paragraph 4.7). Verification of system readiness, a software function, is required prior to initiation of a write operation. The conditions that must be satisfied before a write operation can be performed are:

(1) The unit must be in the Ready condition and Selected. This implies that only one head is selected.

(2) The head must be positioned over a legal track address.

(3) The WRITE PROTECT switch(es) for the platter(s) selected is switched to the OFF position and the Power Clear signal is at a high level.

(4) The Write Mode and Read Switch input lines must be low.

The drive is conditioned to perform a write operation when the Write Enable (IWEXR) line is low. At this time the Write drivers are receptive to Write Data pulses. When the Write Enable line is active and system readiness is satisfied, current flows through the write coil, recording new data and causing all previous data to be overwritten, i.e., obliterated.

The read/write coil is a split center-tapped winding. During a write operation, current flows in alternate halves of the read/write coil. Switching of write current in each half leg causes magnetic flux reversals on the disk surface. It is important to note that when the drive is in the Write mode, the erase coil is also energized. The read/write gap is located in front of the erase gap. The magnetized portion of the track is approximately 0.102 mm (0.004 inch) wide on the surface of the disk, but the erase gap, which straddles the read/write gap, erases part of the write flux pattern, leaving a recorded-data band that is approximately 0.091 mm (0.0036 inch) wide. This provides a signal guard band between adjacent tracks.

4.6.2.1 Write Driver

The Write Driver circuitry, shown in Figure 4-4, switches the write current to alternate halves of the read/write head winding. The rate at which the write current is switched is determined by the Write Double Frequency (NLWDFT) signal from the Logic PCBA. NLWDFT toggles a flip-flop whose outputs drive two write current control switching transistors into alternately conducting states. The write current drivers are enabled by a low logic level input on the Write Mode (NLWDFT) line at the Read/Write PCBA.

4.6.2.2 Erase Driver

The Erase Driver circuit is a transistor switch current source that is energized by the Erase Current Enable (NLECEG) signal input to the Read/Write PCBA. A low logic level at the NLECEG input enables the erase current to flow into the read/write head erase windings.

4.6.2.3 Write Current Control

The write current control causes the current level in the read/write coils to change as a function of the positioner cylinder address. For cylinder addresses of 0 through 255, the current level is set at approximately 68 ma; at cylinder address 256 and above, the current level is reduced to approximately 58 ma. This current level change is required because of the increased bit density at the innermost tracks on the disk surface. The lower write current levels reduce the flux pattern fringe effects on neighboring bits.

4.6.2.4 Write Emergency Monitor

This circuitry continuously monitors the legality of conditions within the read/write system. If conditions are improper, the write emergency monitor outputs an active high logic level to the emergency unload circuitry on the Logic PCBA. This causes the drive to execute an emergency unload operation. Conditions that would cause a read/write emergency unload are:

(1) More than one head is selected at one time.

(2) The current monitor circuitry indicates the presence of a current in either the write or erase circuits when such current is not enabled by NLWMXG and/or NLECEG.

4.6.2.5 Current Monitor

The current monitor circuitry continuously checks the current level in the Write Driver and Erase Driver circuits and outputs a low logic level to the write emergency circuitry during a write/erase operation. When both the Write Mode and Erase Current Enable lines are at a high logic level, the write emergency circuitry assumes that a read operation is in progress and looks for a high logic level from the current monitor. Should the output of the current monitor be at a low logic level at this time, the write emergency monitor will sense an illegal condition and cause the system to perform an emergency unload.

In addition to the current monitoring function, the current monitor circuitry can disable the flow of write or erase currents to the read/write heads. The Power Clear signal (SPCSA) generated on the Servo PCBA indicates the status of the regulated dc voltages and controls a transistor switch in series with the common write/erase current path. In case of a power failure, SPCSA goes to a low level, causing the transistor switch to open the write/erase current line. This action prevents the writing of erroneous information on the disk surface during a power failure emergency unload condition.

4.6.3 READ ELECTRONICS

A Read Enable (IREXR) signal from the system I/O interface conditions the Read/Write circuitry to perform a read operation. Certain readiness checks must be performed by the drive Function Control Logic circuitry before information can be transferred from the surface of the disk to the system I/O interface. The selected drive must be in the Ready condition; this implies that the following conditions exist:

(1) The heads are positioned over a legal track address.

(2) Only one head is selected.

(3) The Write Enable and Erase Current Enable lines are both high and the current monitor senses no write or erase current flow.

(4) The Write Mode and Read Switch inputs must be high.

The Read Electronics are activated when both the Write Mode and Erase Current Enable inputs to the Read/Write PCBA are at a high level. This condition is locally ANDed resulting in the Read/Write head windings being connected to the read preamplifier. The amplified read data are filtered, peak detected, digitized, and decoded before being suitable for transmission to the using system interface. When the Read Enable Control (NLRECG) signal to the Read/Write PCBA goes low, the Read Data (IRDXR) and Read Clocks (IRCXD) are gated onto the system I/O interface lines. A detailed discussion of the Read Electronics portion of Figure 4-4 is contained in the following paragraphs.

4.6.3.1 Head Switch Circuitry

The Head Switch circuitry (Read Switch input line low) disconnects the Read preamplifier signal inputs from the read/write heads during a write/erase operation. This is done to prevent the large voltage signals that are applied to the head's read/write windings during a write operation from entering the low level inputs of the read preamplifier. Thus, the

Head Switch circuitry prevents the amplifier from being driven into saturation during a write operation.

4.6.3.2 Read Preamplifier

The Read Preamplifier is a single integrated circuit consisting of a wide band, linear differential amplifier stage. Read signals from the read/write heads are typically quasi-sinusoidal with typical amplitudes of approximately 1 mv to 5 mv. The nominal voltage gain of this amplifier is 150; the read signal output has an amplitude of approximately 200 mv peak-to-peak. The amplifier gain is determined by a resistor of appropriate size across the gain-adjust terminals.

4.6.3.3 Filter

The amplifier read signal is ac-coupled to an L-C filter stage which removes the undesirable high-frequency noise signals superimposed on the read signal. The special quality of the filter is its ability to pass the read signal with only small attenuation and negligible phase non-linearity.

4.6.3.4 Differentiator and Peak Detector

The filtered read signal is amplified and phase shifted 90 degrees by the differentiator stage. This stage has a nominal voltage gain of approximately 7.3 under normal operating conditions; thus, the read signal output is normally 350 to 650 mv peak-to-peak. The operation of the peak detector is illustrated in Figure 4-5.

4.6.3.5 Squarer and Frequency Doubler

The filtered read signal drives a squaring circuit which converts the sinusoidal read signal into digital data by switching its output voltage level at each zero crossover of the read data signal.

The output voltage signal from the squaring circuit is 1.2v peak-to-peak amplitude that swings about a + 0.6v reference. Prior to decoding, the read data are converted into a pulse train at a frequency that is twice the read data rate. The action of the edge detector is shown in Figure 4-6. The pulsewidth of the signal is controlled by component values within the edge detector circuitry.

4.6.3.6 Data Decoder Circuitry

The Data Decoder circuitry is essentially a data/clock separator. It is comprised of two one-shot multivibrators, a decoding window generator, and a window polarizing circuit. The Read Pulse Narrow (RPN) signal has a nominal data rate frequency when read data are all zeros, and is twice this frequency when read data are all ones. It is this characteristic that enables the Data Decoder circuitry to separate read data from the clocks.

The first RPN pulse is treated as a clock pulse. Its leading edge clocks the ones window one shots to look for a data bit. At the end of the one-shot timing, the ones gate is reset and the next RPN pulse is another clock pulse. If an RPN pulse is present between the clock pulses, it is treated as a data bit or a one bit and presented to the Read Data interface line. The ones data output repetition rate will therefore be at the read clock rate. The timing diagram shown in Figure 4-7 details these timing relationships. Two pulse former one-shots determine the output pulsewidth.

4.6.3.7 Read Data Control

The Read Data Control gates the Read Clocks and Read Data onto the system I/O interface lines, via line drivers on the Logic PCBA, in response to the Read Enable Control (NLRECG) signal. When NLRECG is initiated, the Read Clock and Read Data gate control is clocked to the enable state. This prevents pulse *shaving* of the Read Data and Read Clock signals.

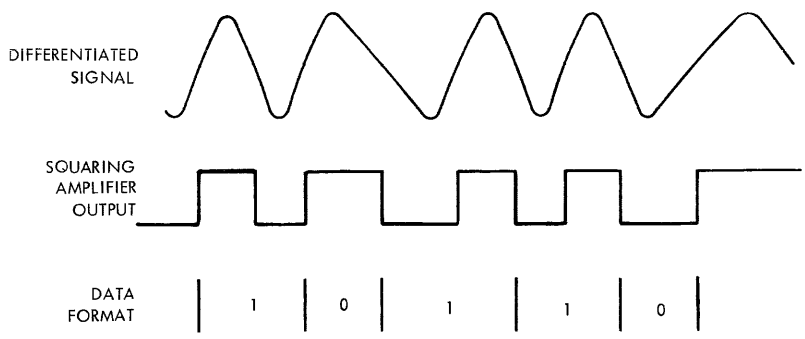


Figure 4-5. Peak Detector and Squarer Waveform

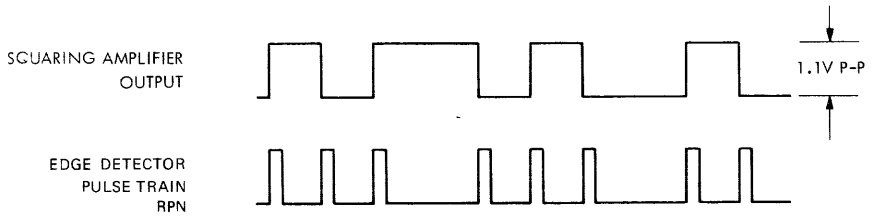


Figure 4-6. Edge Detector Timing Relationship

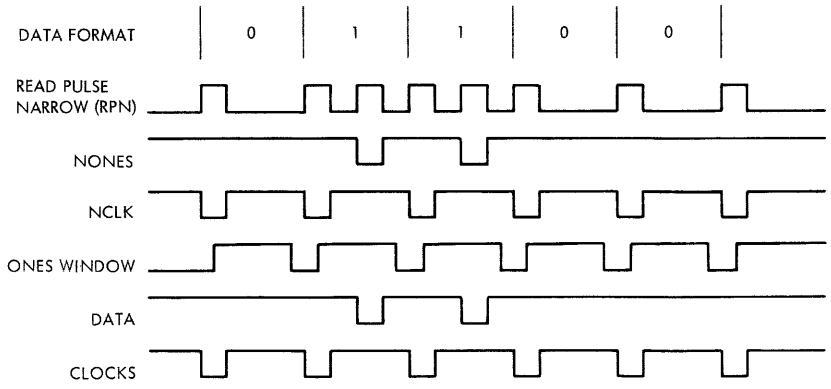


Figure 4-7. Data Decode Timing Relationships

4.7 LOGIC FUNCTIONS AND CONTROL

There are five major areas in the D3000 Series Disk Drives which require logic for control of functions and timing, these are: Disk Drive Function Control, Read/Write Electronics, Spindle Speed Control Electronics, Position Control Electronics, and Sector Electronics. They are functionally shown in Figure 1-4. Since the majority of logic in the D3000 is packaged on the Logic PCBA, the following is primarily a functional description of the Logic PCBA. Only those areas on other circuit boards having logic functions of interest are included.

NOTE

To fully understand the logic functions described, the reader should acquaint himself with the discussion of the circuits contained in Section V. He should also become familiar with the schematics contained in Section VII.

4.7.1 LOGIC ARRANGEMENT

The Logic PCBA is depicted on sheets 3 through 13 of Schematic No. 108160. These sheets have been divided on the basis of function and, therefore, a specific sheet is a complete (or nearly complete) schematic representation of a specific function. The following discussion identifies these functions by schematic sheet number.

4.7.1.1 Logic Schematic, Sheets 3, 4, and 5

Sheet three of the Logic schematic contains the Start/Stop Control which is used in the control and timing process of executing the start cycle of the drive and for executing the stop cycle of the drive. Also shown on this sheet is the main clock generation circuitry which consists of the crystal oscillator, clock countdown, and clock gating circuitry. This arrangement provides the reference for all timing functions on the Logic PCBA.

A subdivision of the Start/Stop Control is also included. This circuitry is used for the detection of run/stop commands, emergency and fault mode control, interlocking control, start cycle sequencing, stop cycle sequencing, and condition indication.

4.7.1.2 Logic Schematic, Sheets 6, 7, and 8

Sheet three of the Logic schematic contains a number of minor functions; these are the select enable controls, the read outputs, the status outputs, the termination voltage power supply, and the spindle speed control digital logic.

A subdivision of the select enable function is the head and platter select control, track offset enable control, write/erase enable control, unit select decoding, busy signal encoding, write protection control, and the status and indication circuitry.

4.7.1.3 Logic Schematic, Sheets 9 and 10

The functions shown on sheet four of the Logic schematic deal entirely with position control; these are the track address register, the illegal address comparator, the current address counter, the count clock detector register, subtractor and complementor, and carry control.

4.7.1.4 Logic Schematic, Sheets 11, 12, and 13

The functions shown on these sheets of the Logic schematic consist entirely of sector electronics. These functions consist of the upper sensor detector, the upper time demultiplexer, the lower sensor detector, lower time demultiplexer, sector phase lock loop, upper sector countdown, lower sector countdown, sector multiplexer, index multiplexer, sector pulse formers, index pulse formers, upper sector number counter, lower sector number counter, sector count multiplexer, and the multiplexer control.

4.7.2 DISK DRIVE FUNCTION CONTROL

The Disk Drive Function Control Logic is one of the major subdivisions of the drive which require logic for the control of functions performed. Figure 1-4 is a functional block diagram of the D3000 Disk Drive and should be referred to in conjunction with the following paragraphs.

The major block identified as Disk Drive Function Control in Figure 1-4 can be subdivided into two parts: a major block consisting of the Start/Stop Control, and a minor block containing minor control functions, e.g., head select control and unit select decoding. The following paragraphs contain a functional discussion of these blocks.

4.7.2.1 Start/Stop Control

Essentially, the Start/Stop Control is a digital sequential machine mechanized with integrated circuit logic. This logic takes the external commands, combines them with internal conditions plus suitable timing, and generates output signals for control and indication purposes. Figure 4-8 is a block diagram of the digital sequential machine used to mechanize the Start/Stop Control.

Referring to Figure 4-8, the three essential blocks are State Storage, Combinational Logic, and Delay Generator. The State Storage block stores the machine states. This is mechanized with flip-flops and a counter. The present states are combined in the Combinational Logic with external commands which allows the generation of output signals for indication and control by the output signal combinational logic. All of the combinational logic is mechanized with gates. It should be noted that external commands can modify directly the stored states. This is in addition to the capability of external commands in combination with the present states to provide output signals and modification of the stored states.

Included in the block diagram is a Delay Generator which is mechanized with counters and a flip-flop. The generator provides specific delays under control of certain of the Combinational Logic output signals. The Time Reference to the Delay Generator is obtained from a crystal oscillator and clock countdown circuits.

Figure 4-9* is a functional block diagram of the Start/Stop Control. All of the logic depicted in this figure is contained on sheet two of the Logic PCBA schematic. The time reference for this arrangement is provided by a crystal oscillator whose output signal is frequency divided by the Clock Countdown circuitry. This circuitry consists of a series chain of counters that generate clock signals that are used by the Start/Stop Control logic. These clock frequencies are also used in other portions of the drive logic.

Within the Start/Stop Control, gating of the clock signals is accomplished by allowing clock pulses to be fed to the flip-flops only at specific times, thereby permitting these flip-flops to change state only when a clock pulse is present. The delay generation portion of the Start/Stop Control is handled by a Delay Counter which is operated from a clock signal generated by the Clock Countdown circuitry.

In addition to the state storage, there are three major functions performed by the Start/Stop Control; these are interlocking control, emergency unload logic, and condition indication.

Referring to Figure 4-9, commands used to start or stop the drive may be received either from the RUN/STOP operator control or from the Start/Stop Disk Drive I/O interface line (ISSDR). These commands are detected by the Run/Stop command and Detection circuitry and cause the Start/Stop Control to execute a start or a stop, as appropriate.

*Foldout drawing, see end of this section.

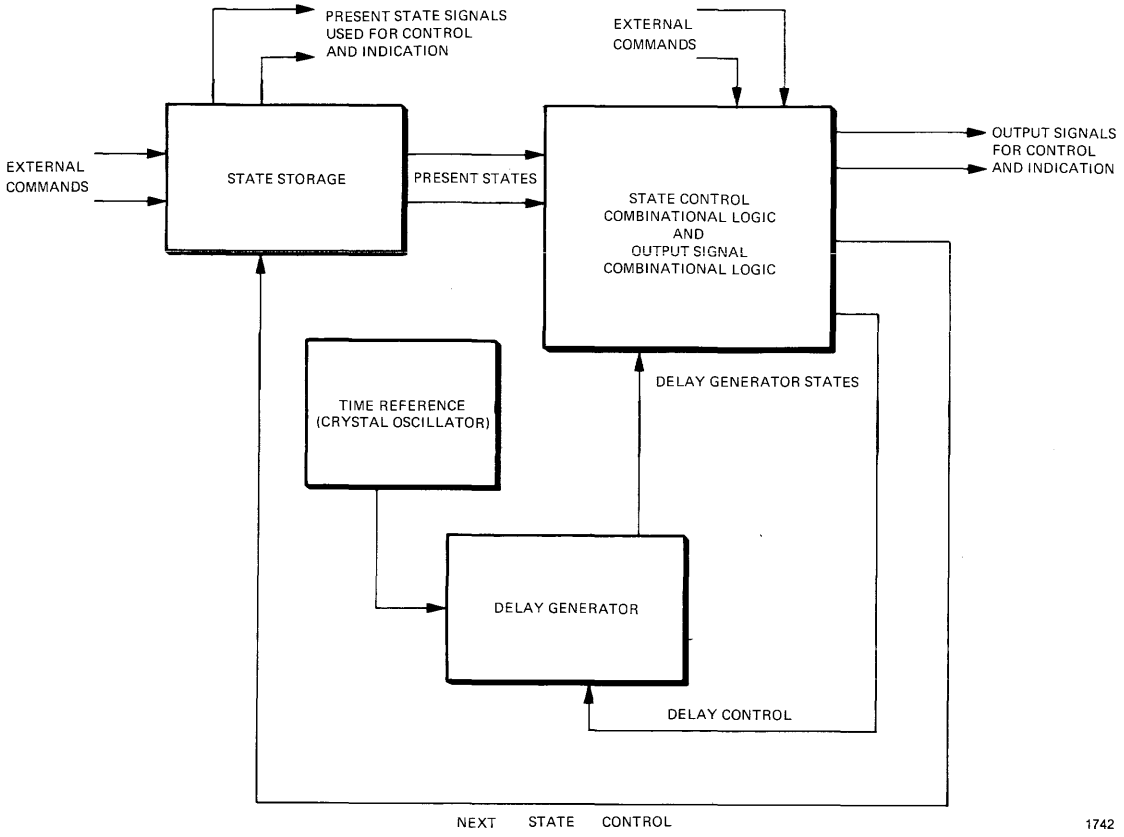


Figure 4-8. Digital Sequential Machine Block Diagram

Interlocking is obtained by using a number of signals which are available within the drive. These signals, used in conjunction with each other, allow interlocking of various mechanical functions, e.g., locking the door on front load machines, and locking the cartridges in top load machines when the disk is rotating. The Lower Detector Pulse (LLDPG) input to the Interlock Control portion of the logic is used to establish that the disk is rotating. The Not Write Or Erase signal (NLWOEG) is generated by some of the minor control logic within the Disk Drive Function Control block and is used to prevent retracting the heads during a normal unload when either a Write or an Erase command from the I/O interface is occurring.

Correct insertion of the cartridge is detected by one switch in top load machines, and by one switch in front load machines. This interlock prevents starting the drive when the cartridge is not inserted.

The Power Clear Signal (SPCSA) from the Servo PCBA signals when an unacceptable power supply condition is sensed. The SPCSA is provided to the Start/Stop Control logic as well as to the Read/Write PCBA. Also supplied from the Servo PCBA is the Heads Retracted signal (SHRXG) which is used by the Interlock Control to ensure that the disk does not stop rotating unless the heads are retracted.

The purpose of the Emergency Unload Logic is to begin an emergency unload operation when commanded externally, or when this logic detects certain fault situations which require emergency unloading of the heads from the storage surface. One of these fault conditions is the Position Transducer Failure (SPTFG) condition. This condition is

detected on the Servo PCBA and is provided to the Emergency Unload Logic should a failure occur in the position transducer. Another signal, the Write Emergency Condition (RWECG) is generated on the Read/Write PCBA if a write emergency condition is detected.

All other emergency unload conditions are detected by logic circuitry on the Logic PCBA. Three of these emergency conditions are detected within the Start/Stop Control arrangement by the Emergency Unload logic. The signals utilized are: Not Position Mode (NLPMXG), and Speed Out of Tolerance (LSOTF). The NLPMXG logic state is tested by the Emergency Unload logic to determine if the heads have properly loaded during a start sequence. LSOTF is tested during the start sequence to determine if the disks have reached the proper speed prior to loading the heads.

Elsewhere within the logic, three signals are generated upon detection of a specific fault condition and are provided to the Emergency Unload logic. These signals are Not Position Limit Error (NLPLEG), Not Disk Speed Error (NLDSEG), and Not Seek Time Error (NLSTEG). The NLPLEG signal commands emergency unload when the positioner exceeds its legal range of travel. The NLDSEG signal commands an emergency unload when a disk speed error is detected after the system achieves the Ready condition. The NLSTEG signal commands an emergency unload when the time for a seek exceeds the allowable maximum.

The major function control output signals from the Start/Stop Control are:

(1) Start Drive Motor (NLSDMG), a pulse used for initializing the spindle speed control logic.

(2) Purge Cycle (LPCFF), a flip-flop output state used for controlling the disk speed during the purge cycle.

(3) Load Heads (LLHFF), a flip-flop output state used for controlling the position control logic and loading and unloading the heads.

(4) Emergency Unload (LEUFF), a flip-flop output state used to indicate that an emergency unload condition has started or presently exists.

(5) Load or Purge Not (NLLPNG), the output of combinational logic within the Start/Stop Control, decodes the states of two of the major state storage flip-flops, Purge Cycle and Load Heads. NLLPNG is used for initializing the position limit monitor contained within the Position Control Logic.

(6) Brake Cycle Enable (NLBCEG), the control signal which determines when the braking current is applied to the drive motor.

(7) Lock Cartridge Mechanism (LLCMG) controls the solenoid drivers on the Servo PCBA and is the signal which determines when the cartridge mechanism is locked or unlocked.

(8) Emergency Unload Enable (LEUEG) controls the emergency unload relay driver on the Servo PCBA; this relay driver, in turn, actuates the emergency unload relay as commanded by the Emergency Unload Enable signal.

The output signals from the Start/Stop Control circuitry described in Steps (1) through (5) are used on the Logic PCBA for specific control functions. The signals described in Steps (6) through (8) are fed directly to the Servo PCBA.

Three signals for driving the operator control panel lamps are generated by the Condition Indication portion of the Start/Stop Control logic. These signals are Safe Lamp Drive (NLSLDT), Run Lamp Drive (NLRXDT), and the Ready Lamp Drive (NLRLDT). The SAFE lamp is used to indicate when it is safe for the operator to remove or insert a cartridge into the drive; the RUN lamp is used to indicate when a machine is executing a start sequence, or the disk is running. Illumination of the READY lamp indicates that the drive has achieved the Ready condition.

Other signals generated by the Condition Indication logic are: Ready (LRXXG), Selected And Ready (LSARG), and Delayed Ready Condition (LDRCG). The Ready signal is the output of combinational logic and is the combination of several flip-flop states within the Start/Stop Control. The Selected And Ready signal is the Ready signal combined with the Selected signal from the Unit Select logic. The Delayed Ready condition is the Ready signal passed through a delay network. LRXXG, LSARG, and LDRCG signals are used in other parts of the Function Control logic as well as enabling certain portions of the Position Control logic and the Sector Electronics logic.

When the Interrupt Option is included in the drive, the File Ready, Ready to Seek/Read or Write, and Seek Incomplete are not conditioned by the Select line. Therefore, the states of these lines are presented to the interface at all times.

4.7.2.2 Minor Control Functions

The minor functions discussed in the following paragraphs are contained within the Disk Drive Function Control logic block shown in Figure 1-4. Due to the nature of these minor control functions, no attempt is made to relate them to a simplified block diagram. The circuitry which performs these logic functions is contained on sheet three of the Logic PCBA schematic.

The Select and Control logic consists of a holding register and associated control gates for processing the Platter and Head Select lines, the Track Offset Plus, and Track Offset Minus lines. Also included is the Write Double Frequency Data Retransmitter which acts as a line receiver and a line driver between the I/O interface and the Read/Write PCBA. The Unit Select logic, the Busy Output logic, and the Ready driver are also included as minor elements in the Disk Drive Function Control logic. Likewise, the Read/Write Control logic and the Write Protect logic, including the Write Protect Lamp Drivers, are part of the Disk Drive Function logic. Additional minor functions are performed by the Read Signal Drivers, the Malfunction Signal Driver, the Illegal Address Status Driver, the Dual Platter Status Driver, and the Quad Platter Status Driver. These functions are described in terms of function and purpose, as follows.

Three I/O interface control lines are provided for selecting a specific storage surface. These lines are Head Select (IHSXR), Platter Select (IPSXR), and Platter Select Extension (IPSER). Two other I/O interface control lines, Track Offset Plus (ITOPR) and Track Offset Minus (ITOMR) provide for selecting specific track offsets for diagnostic purposes. These five lines are processed by the holding register and distributed to the Read/Write PCBA. The ITOPR and ITOMR lines are also distributed to the Servo PCBA.

The Holding Register stores the status of these lines under certain conditions which are determined by the Selected And Ready and the Not Ready conditions. The Write Double Frequency Data Retransmitter acts as a line receiver for the I/O interface line Write Data Signal (IWDSR) and retransmits the signal to the Read/Write PCBA as the Write Double Frequency signal. This acts as a buffer and maintains timing of the Write Double Frequency signal.

Another minor function provided by the Disk Drive Function Control logic is contained in the Unit Select logic. This logic combines the setting of the Unit Number Selector switch on the operator panel with the specific Unit Select Number signal from the I/O interface. Decoding is performed and the Select signal is generated only when the Unit Select line from the I/O interface corresponds to the number designated for the specific drive by the Unit Number Selector switch.

Also contained within the Disk Drive Function Control logic is the Busy Output logic. This logic combines the busy signal from the Position Control logic with the Ready signal and encodes on a Busy Seeking line according to the setting of the Unit Number Selector switch.

A number of line driver functions are performed by various signal drivers. These drive internal logic signals onto the I/O interface lines as outputs of the drive. These are:

(1) The Ready Driver for driving the Selected And Ready signal onto the Ready line at the interface.

(2) The Read Signal Drivers for transmitting the outputs of the Read/Write PCBA onto the Read Data and Read Clock I/O interface lines.

(3) The Attention line drivers are logical combinations of output lines that inform the controller when the disk becomes Ready, completes a seek, fails to complete a seek, or accepts an illegal track address.

(4) A Double Track Status interface line for indicating, at the interface, that the drive is a 200-tpi model.

(5) The Illegal Address Status driver for transmitting the Illegal Address signal to the Illegal Cylinder Address interface line.

(6) Dual Platter Status signal driver for indicating on the Dual Platter Drive interface line that the drive contains two disks.

(7) Quad Platter Status signal driver for indicating on the Quad-Platter Drive interface line that the drive contains four disks.

Another minor function control performed is the processing of the Write Enable (IWEXR) and Erase Enable (IEEXR) signals from the I/O interface. These signals are gated by Selected And Ready, Position Mode, and File Protect Mode, then transmitted to the Read/Write PCBA for controlling those functions. In addition, the Not Write or Erase signal is generated for application to the Start/Stop Control Logic. Also performed within the Read/Write control logic is the gating of Read Enable with Selected And Ready. This signal is then transmitted to the Read/Write PCBA.

The Write Protect logic combines the state of the specific WRITE PROTECT switch on the operator panel with the state of the Platter Select (IPSXR) and Platter Select Extension (IESLR) lines such that the respective protect switch and the IPSXR and IESLR lines are decoded to set or reset the File Protect Mode latch. The state of the File Protect Mode latch determines whether a particular disk is permitted write and erase operations, depending upon whether it is designated as a protected disk by the respective WRITE PROTECT switch on the operator panel.

The state of the File Protect Mode latch is gated with Selected And Ready and is transmitted to the I/O interface by the File Protected Status Driver which transmits the file protect condition of the drive to the controller on the File Protected (IFPXD) I/O line. The state of the WRITE PROTECT switches is indicated by the operator panel PROT (Protect) lamps regardless of which disk is selected. In dual-disk models, the lamp indication depends entirely on the state of the respective switch; in quad-disk models, the lamp drive signals are generated by the protect lamp drivers according to the switch states.

4.7.3 SPINDLE SPEED CONTROL

The rotational speed of the spindle is controlled to within ± 1 percent of the nominal value. This tight control is maintained so that spindle speed is not affected by line frequency variations and to avoid disk speed variations due to tolerances of the drive train components. The time reference for the spindle speed control is derived from the Crystal Oscillator and Clock Countdown logic that is shown in Figure 4-9 as part of the Start/Stop Control logic.

The actual speed of the spindle is derived by sensing notches in the phase lock ring with a magnetic transducer. In addition to the speed sensing function, Phase Lock Ring and the Magnetic Transducer are used in conjunction with the Sector Electronics (Paragraph 4.7.5). The Phase Lock Ring is a flat circular plate with notches in the periphery. It is

mounted integral with the spindle and therefore the rotational speed of the Phase Lock Ring is the same as that of the spindle. The Spindle Speed Control is a true servo loop in that power is controlled to the drive motor which, in turn, rotates the spindle; the actual speed of the spindle is sensed and compared with a time reference and the result of the comparison is used to correct the amount of power applied to the drive motor. In this manner, the loop corrects the existing speed of the spindle to the correct speed within the ability of its resolution and response capability. It is important to note that although the loop is a true closed loop servo, it is not a linear servo system. The reason is that the result of the time/speed comparison is a single binary digit and therefore can have only two possible states, a zero or a one, i.e., the speed is either too fast or too slow. For this reason, the actual speed regulation takes place in a limit cycle type of operation where the actual spindle speed varies between an upper and a lower boundary as determined by the response time of the loop and the resolution of the error detector. However, certain of the loop characteristics are like a linear servo in that power to the drive motor is varied for control by changing the time of occurrence of the application of power within a given power line cycle in a manner which is usually referred to as phase angle control. In other words, the actual phase angle during the power line cycle where power is applied to the main winding of the drive motor is the result of the integral of the binary speed error. This determination is made from the comparison of the actual speed sensed by the Magnetic Transducer to the time reference derived from the Crystal Oscillator.

Refer to Figure 4-10*, a functional block diagram of the Spindle Speed Control logic, for the following discussion. Operation of the spindle speed control can best be understood by starting at the Spindle and going around the loop. The Magnetic Transducer senses the notches in the Phase Lock Ring and produces a signal which is then processed by the Sector Electronics logic (refer to Paragraph 4.7.5).

The results of the action taken by the Sector Electronics logic is the output of a flip-flop called the Phase Lock Flip-Flop (LPLFF). This flip-flop functions as a frequency divider on the basic frequency derived from the Phase Lock Ring and converts the pulse as processed by the sector electronics into a square wave. The Phase Lock Flip-Flop signal is fed into the Speed Sequence Control as shown in the block diagram.

Clock signals derived from the Crystal Oscillator and Clock Countdown (LC02F, LC03F, LC04F) are fed to the Speed Control Programming logic, then to the Speed Control Counter. The time between the occurrences of low to high transitions of the Phase Lock Flip-Flop signal is detected by the Speed Sequence Control logic. Detection of this transition causes the Speed Sequence Control to generate two pulses which are synchronous with the clock signal specified by the Speed Control Programming logic. These pulses determine the sequence of the time comparison.

The desired value of disk speed is programmed by the Disk Speed Count Programming array. The program value fed to the Speed Control Counter is determined by the array and the state of the Purge Cycle Flip-Flop (LPCFF), thereby providing a nominal speed for normal operation and an over-speed value for use during the purge cycle. The programmed value of the disk speed count is fed to the Speed Control Counter logic and the selected clock signal from the Speed Control Programming logic is then counted by the Speed Control Counter. The results of the count are stored in the Speed Value Flip-Flops and, when appropriate, transferred to the Speed Status Flip-Flops as determined by the Speed Sequence Control logic. The actual comparison of the spindle speed to the reference signal occurs on the basis of the count totalized in the Speed Control Counter logic during the time interval defined between the transitions of the Phase Lock Flip-Flop.

*Foldout drawing, see end of this section.

There are two outputs derived from the Speed Status Flip-Flops; the Increase Motor Speed (NLIMS1) signal and the Speed Out Of Tolerance (LSOTF) signal. The Speed Out of Tolerance signal indicates when the disk speed is detected as being out of tolerance by the Speed Value Flip-Flops. This information is tested during the start sequence and is also combined in a Gate with the Ready signal (LRXXG) to produce Disk Speed Error (NLSDEG). The Increase Motor Speed signal is fed to the Servo PCBA and is the basic binary error signal derived from the comparison of the time reference to the actual speed. The Start Drive Motor pulse (NLSDMG) is used for initializing the speed status flip-flops during a start sequence and the Drive Motor Enable (LDMEG) line is used for initializing the Speed Sequence Control and the Speed Status Flip-Flops.

It can be seen that the purpose of the circuitry on the Logic PCBA is to convert the analog signal obtained from the Magnetic Transducer into a suitable digital square wave, then compare the time of occurrence of the positive transitions of that square wave with a time reference obtained from a Crystal Oscillator. The result of that comparison is two signals, one indicating the instantaneous speed error signal and, if appropriate, to provide a signal which would indicate a gross malfunction of the speed control. The Increase Motor Speed (NLIMS1) obtained from the Speed Status Flip-Flops is fed to the Servo PCBA.

A portion of the Spindle Speed Control circuitry is located on the Servo PCBA. Basically, there are two functions performed by this circuitry; the generation of a signal to the Motor Control PCBA which is synchronized to the line frequency and causes the trigger to occur at a specific time during the power line cycle.

Generation of a signal which is synchronized to the line frequency is necessary because the basic power line is the power applied to the drive motor by the Motor Control PCBA. This line synchronization is accomplished by a Zero Crossing type of synchronizing network in which a pulse is developed by the Line Synchronizer when the line voltage passes through the zero volt condition.

The trigger to the Motor Control PCBA must be supplied at a specific time during the power line cycle. The time of occurrence of this trigger must be proportional to the integral of the binary error signal. This is done to provide a proportional power control to the drive motor main winding that is the time average of the binary error signal NLIMS1.

Phase angle control is obtained by the use of a Ramp Generator which is synchronized to the line voltage by the line synchronizer. The output of the integrator is compared with the voltage developed by the Ramp Generator in a Voltage Comparator. The results of this comparison are used to generate a trigger signal which is fed to the Motor Control PCBA.

The Motor Control PCBA is, in essence, a bi-directional power switch isolated from the normal machine ground. The switch is turned on by the trigger signal from the Servo PCBA and then turns itself off as the line current passes through zero. Also contained on the Motor Control PCBA is the necessary interconnection wiring for configuring the drive motor for two basic types of power line operation, 110v and 220v (refer to Paragraph 4.8).

The trigger signal obtained from the Servo PCBA is applied to Current Amplifier Transistor Switches via an Opto-Isolator device. The Current Amplifier Transistor Switches apply gate current to the Triac Switch which selects the power line onto the main winding of the drive motor. During normal speed control, when power is to be applied to the drive motor, the specific time for switching in the power is determined by the voltage comparator on the Servo PCBA. The Triac Switch allows current to pass through the drive motor winding for that portion of the line cycle. Since the power line voltage has both a positive and a negative excursion in a given cycle, power may be applied twice during a cycle. The phase angle of that power application can be determined and controlled by the comparison of the Ramp Generator with the integrated increase motor speed signal.

The control circuitry contained on the Servo PCBA is enabled by the Not Drive Motor Enable (NLDMEG) signal. Thus, when it is desired to have no power applied to the drive motor (e.g., when the machine is stopped), the circuitry is correspondingly commanded by the state on the drive motor enable line. When it is desired to stop the disk from rotating, it is necessary to develop a braking torque to slow the disk down to the stop condition in a reasonable amount of time. This is necessary because the rotating assemblies have a considerable inertia and the time for the spindle to coast down to a stop without an additional braking force would be excessive. In order to develop this braking torque, the drive motor is operated in a special mode during that portion of the stop cycle. This is referred to as a brake cycle and is defined by the Brake Cycle Enable (NLBCEG) signal derived from the Start/Stop Control logic on the Logic PCBA. When the Brake Cycle Enable signal is asserted, the Servo PCBA circuitry is caused to operate in a slightly different mode wherein full power is applied to the drive motor main winding but only for one-half of a line cycle. This develops a magnetic field in the drive motor which results in a braking torque rather than in a running or starting torque. It is this torque which is used to slow the spindle to a stop.

4.7.4 POSITION CONTROL LOGIC

Figure 4-11* is a functional block diagram of the Position Control logic and should be referred to in conjunction with the following discussion.

The major function of the Position Control logic is to accept address commands from the I/O interface and cause the positioner to move to the address demanded by the interface. This involves generating suitable signals to control the mode of operation of the positioner servo and to control the velocity that is used by the positioner servo. Additionally, certain signals are generated which are supplied to the interface for indicating the Position Control logic status. Error checking of the Position Control logic functions are also accomplished by this logic.

The major inputs from the I/O interface are the Track Address (ITA0R—ITAER) lines, the Address Strobe (ISTRR), and the Restore (IRTRR) lines. Inputs to the Position Control logic from the Servo PCBA are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Position Transducer Index (SPTIG), and Heads Retracted (SHRXG). The signals from the Servo PCBA are derived from the position transducer. Additionally, the Load Head signal (LLHFF) is provided as an input to the Position Control logic from the Start/Stop logic and is used in the Mode Control logic.

Major output signals from the Position Control logic to the Servo PCBA are the Address Difference (NLADNG), Forward Direction (LFDX1), Velocity Reference Enable (NLVREG), Position Mode (LPMXG), Forward Slow Mode (NLFSM1), and Reverse Slow Mode (NLRSM1). The major output signals which determine interface outputs are the Illegal Address (NLIAXG) and the Busy (NLBSXG) signals. The auxiliary output supplied to the Read/Write PCBA from the Position Control logic is Demand Address Most Significant (LDAMG). An auxiliary output consisting of the three most significant bits from the current address counter are supplied to the Temperature Compensation PCBA.

A Track Address from the I/O interface specifies the address that is required by the controller. If the address is accepted by the Position Control logic, it is stored in the Demand Address Register. Loading of this register is under control of the Load Address and Illegal Address Control logic. The validity of a demand address on the I/O interface lines is tested by the Valid Address Decoders.

*Foldout drawing, see end of this section.

The inspection and test of the address is made only when accompanied by a Strobe (ISTRR) from the I/O interface. In addition, the state of Restore (IRTRR) line is examined at the time of a Strobe and the state of that line determines if the address is to be accepted or ignored, and if a restore operation is to be performed. When the Restore line is asserted at the time of a Strobe, the Track Address lines are ignored and the Position Control logic commences a Restore operation. A Restore operation initializes the Position Control logic and returns the positioner to cylinder 000. If a Restore is not asserted at the time of a Strobe, then the Track Address lines are examined to determine if they contain a valid address. If a valid address is present, this address is accepted by the Position Control logic. If the address is an illegal address, i.e., it lies outside the range of the valid addresses, then this is signalled by the Illegal Address (NLIAXG) line.

During a Strobe, and any time during a Seek operation, the Position Control logic and the positioner status are indicated on the Busy Time Signal (NLBTFF) line. Illegal Address and Busy Time signal are outputs of the Load Address and Illegal Address Control and the Busy logic.

Information describing the current position of the positioner is stored in the Current Address Counter which is an up/down type of counter. The direction of the count and the amount of the count are determined by the Count Control logic on the basis of the Position Reference Clock (SPRCG) and Position Quadrature Clock (SPQCG) signals from the Servo PCBA. These are the digital position transducer signals derived from the outputs of the position transducer.

The positioning system in the D3000 Disk Drive functions on the basis that the physical position of the positioner is known to the Position Control logic at all times. This is because the logic has kept track of all moves made by the positioner since initialization, i.e., current position information is initialized at the time the heads are loaded. In other words, the system knows where it is because it was told where it started from and it kept track of every move thereafter. Furthermore, it knows how far it has to go to achieve the demand address because it knows where its current location is. The particular mode of operation of the Position Control logic is determined by the Mode Control portion of the logic in conjunction with the Operation Control logic. The various inputs and outputs of this portion of the Position Control logic can be seen in the block diagram, Figure 4-11.

There are four modes of operation of the Position Control logic. One mode is the Position Mode which causes the positioner servo to operate as a position-type servo and hold a particular cylinder position.

During a Seek operation it is necessary to operate the positioner servo as a velocity-type servo. This, of course, is a negation of the Position Mode line. In addition to the velocity reference enabled by the Velocity Reference Enable (NLVREG) line, the direction of the velocity is specified by the Forward Direction (LFDX1) line, and the particular velocity reference level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Feedback Pulse Generator on the Servo PCBA by the Address Difference lines. It is important to note that the difference between the current address and the demand address is obtained by performing a ones-complement arithmetic subtraction on the binary values contained in Current Address Counter and the Demand Address Register. This subtraction process is performed by the Subtractor and Complementor logic. Since the arithmetic is ones-complement arithmetic, an end-around carry is used. This carry is under control of the Carry Control logic and the algebraic sign of the velocity desired is determined on the basis of the binary value of the carry. The actual subtraction is mechanized using an integrated circuit binary full-adder. When the heads are being loaded, it is necessary to force the carry to a particular state; this is accomplished by the Carry Control logic on the basis of the states of certain bits in the Current Address Counter.

The other two modes of operation of the Position Control logic are the Forward Slow Mode and the Reverse Slow Mode. The two slow modes are a slow velocity type of operation. The Forward Slow Mode is used during loading of the heads and the latter portion of a Restore operation. The Reverse Slow Mode is used for unloading the heads and performing the first portion of a Restore operation. When operating in the Slow Velocity Mode, the velocity reference developed from the Address Difference lines is not used and therefore Velocity Reference Enable (NLVREG) is not activated.

The Error Check logic performs two types of checks concerned with operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This check is done by the Seek Time Error (NLSTEG) check circuitry and is a gross type of check to determine simply that the positioner has not become stalled due to a fault. Although each seek is checked by this circuit, it does not verify that the time for the specific distance moved was compatible with the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The other error check performed is to determine that the positioner has not traveled outside of the legal range of travel. This is performed by the position limit monitor circuitry which generates a Position Limit Error (NLPLEG) signal if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded onto the disk.

4.7.5 SECTOR ELECTRONICS

Figure 4-12* is a functional block diagram of the Sector Electronics logic and should be referred to in conjunction with the following discussion.

The major function of the Sector Electronics logic is to provide Sector pulses at the I/O interface which electrically subdivide the disk storage surface into a number of sectors for the purpose of addressing data stored on the disk. Additionally, the specific number of the sector passing under the Read/Write heads is transmitted to the I/O interface on the Sector Count lines. These lines specify the sector count presented in a binary format. The count indicates the particular segment of the disk surface currently under the Read/Write heads.

In addition to the Sector Pulse and Sector Count, the Index Pulse is provided as an output of the Sector Electronics. This line provides a signal which is a pulse occurring once per revolution of the disk and may be utilized to define the sector reference, i.e., sector zero.

Referring to Figure 4-12, it can be seen that inputs to the Sector Electronics logic are a signal from the Upper Sector/Index Sensor, a signal from the Lower Phase/Index Sensor, Clock signals obtained from the clock countdown portion of the Start/Stop Control logic and the Drive Motor Enable (LDMEG) signal also from the Start/Stop Control logic.

In quad-disk drives, the removable cartridge may be sectored either electronically or mechanically while the lower (fixed) disk(s) is sectored electronically.

Electronic sectoring can be one of two configurations since the removable cartridge may be one of two configurations, i.e., an index notch only, or with sector slots and an index slot. The associated types of electronic sectoring are provided from an index-only type of cartridge and from a sector-plus-index-slot type of cartridge.

The normal top-loading cartridge has one slot in the armature plate which is referred to as the index notch. This is the standard top-loading cartridge arrangement. Some specially modified top-loading cartridges have additional notches for mechanical sectoring purposes.

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*Foldout drawing, see end of this section.

The normal front-loading cartridge has sector slots for the purpose of sectoring and a single index slot in the sector ring for purposes of mechanical sectoring. Special front-load cartridges may be designed with only an index slot.

Referring to Figure 4-12, the Upper Sector/Index Sensor is a photoelectric type of sensor for front load models and a magnetic transducer for top load models. The Lower Phase/ Index Sensor is a magnetic transducer on all D3000 models. This magnetic transducer senses the notches in the Phase Lock Ring mounted on the spindle. The Phase Lock Ring is used for electronic sectoring and for spindle speed control. The slots or notches in the removable cartridge are sensed by the appropriate sensor type and signal is fed to the Upper Sensor Detector which converts the analog signal from the sensor to a digital pulse train. The pulse train, however, contains either all the pulses for the sector slots or notches and a pulse for the index slot or notch, or in the case of index-only cartridge, just a single pulse for the index notch.

In the event that pulses for the sector slots or notches and the index slot or notch are present, these will be separated by the Upper Time Demultiplexer. The pulse representing the index will be output on one line from the Upper Time Demultiplexer and the sector pulses will be output on another line. Therefore, the Upper Time Demultiplexer functions to separate the index pulse from the sector pulse. It is important to note that these pulses are representative of sensing of the slot and are not the signals fed to the interface. The specific gate time required by the Upper Time Demultiplexer is programmed by a jumper and the basic time reference used is obtained from a clock signal generated in the Clock Countdown portion of the Start/Stop Control logic.

In the case when an index-only cartridge is being used, a single pulse per revolution is applied to the input of the Upper Time Demultiplexer. The output of the Upper Time Demultiplexer will be a single pulse on the same line that was used for outputting the demultiplexed sector information in the previously mentioned case.

The Lower Sensor Detector is a circuit similar to the Upper Sensor Detector except that it has a variable threshold. The circuit converts the analog signal from the Phase Lock Ring magnetic transducer to a digital signal which is applied to the Lower Time Demultiplexer. The purpose of the Threshold Control is to provide a means for changing the sensitivity of the Lower Sensor Detector. When executing a stop sequence, or when the drive is in the Safe condition, it is desirable to be able to detect any rotation of the spindle; this is accomplished by causing the Lower Sensor Detector to operate in a high sensitivity mode via the Threshold Control logic. This high sensitivity threshold is enabled when Drive Motor Enable (LDMEG) is not asserted. When LDMEG is asserted, the threshold is changed to a threshold similar to that used in the Upper Sensor Detector. LDMEG is asserted whenever the disk drive is in the Run condition.

The Lower Time Demultiplexer functions in a manner similar to the Upper Time Demultiplexer except that the Phase Lock Ring always has a single index notch per revolution which is interposed between the phase lock notches. The Lower Time Demultiplexer will output the Index pulse on one line and all the other phase lock notch pulses on the other line. Thus, the Lower Time Demultiplexer separates the pulses obtained from the phase-lock notches from the single index notch. The value of the gate time required by the Lower Time Demultiplexer is programmed by the jumper. The time reference is obtained from a clock signal generated by the Clock Countdown circuitry in the Start/Stop Control logic.

The specific sectoring configuration is selected by the connections of the Sectoring Selection Programming Array shown as two blocks in Figure 4-12. The raw pulses output from this interconnection array are unsuitable for application to the I/O interface directly and must be formed into suitable pulses by the Upper Sector Pulse Former, the Lower Sector Pulse Former, the Upper Index Pulse Former, and the Lower Index Pulse Former.

Each of these pulse former circuits takes the raw input pulse and converts it into a pulse having a time duration that is suitable for transmitting over the I/O interface. The outputs of the Upper Sector Pulse Former and Lower Sector Pulse Former are multiplexed onto the single Sector Pulse (ISPXD) line by the Sector Pulse Multiplexer according to the particular disk selected by the I/O interface.

Likewise, the outputs of the Upper Index Pulse Former and Lower Index Pulse Former are multiplexed by the Index Pulse Multiplexer and fed to the single Index Pulse (IIPXD) line according to the particular disk selected by the interface. The Multiplexer Control logic controls the pulse multiplexers according to the state on the Upper Platter Select (LUPSG), Not-Upper Platter Select (NLUPSG), and Selected And Ready (NLSARG) line.

Additionally, the raw pulses obtained from the Sectoring Selection Programming Array are applied to the sector number counters for generating the sector count. The Upper Sector Number Counter and Upper Count Control are used to generate the sector number count for the upper disk. The Lower Sector Number Counter and Lower Count Control are used for the lower disk. A particular sector count is multiplexed by the Sector Count Multiplexer logic according to the control signals generated by the Multiplexer Control logic. These control signals are a function of the specific disk selected and the Selected And Ready condition. The count control for each sector number counter determines when the counter will be returned to a zero count. This is determined automatically as a result of the count control action obtained from the raw index pulse occurrence.

Electronic pulses are generated by the drive as selected by the Sectoring Selection Programming Array when the removable cartridge has index only, or when it is desired to electronically sector a multi-notch removable cartridge. Additionally, the Sectoring Selection Programming Array causes the drive to generate pulses for sectoring the lower disk which is sectored electronically regardless of the configuration. These pulses are generated by counting down (with an electronic counter) the output of a high-frequency oscillator. Because sector pulses must be synchronous with the instantaneous speed of spindle rotation, it is necessary to phase lock this high-frequency oscillator to the spindle.

These particular functions are implemented by the Sector Phase Lock Loop through the Upper and Lower Sector Countdown Counters. Associated with these counters are Electronic Sector Programming Arrays used to determine a particular number of sectors and a synchronizer for each counter to synchronize the count with the Index pulse obtained from their respective Time Demultiplexer. The output derived from the phase lock ring notches are fed via the Lower Time Demultiplexer to a Phase Lock Flip-Flop which divides the frequency of that pulse train by a factor of 2 and converts it into a square wave. This square wave is used not only by the Sector Phase Lock Loop but is one of the outputs of the Phase Lock Flip-Flop fed to the Spindle Speed Control electronics.

The Voltage Controlled Oscillator (VCO) within the Sector Phase Lock Loop is electronically servoed to the square wave obtained from the Phase Lock Flip-Flop. This is accomplished by taking the output of the VCO and counting it down with the Sector PLL Countdown Counter. The specific countdown value is programmed by the Countdown Programming Array and the output of the counter is converted to a square wave by the Sector Countdown Divider Flip-Flop. The outputs of the Sector Countdown Divider Flip-Flop are compared with the Phase Lock Flip-Flop output by the Phase Comparator. The output of the Phase Comparator is suitably filtered and applied to a Sum-And-Difference Amplifier which generates the control voltage for servoing the frequency of the VCO. This causes the output of the VCO to become phase-locked to the phase lock pulses obtained from the phase-locked ring.

The output of the VCO may be taken directly or the frequency may be divided by a factor of 2 by the VCO Divider Flip-Flop and applied to the Sectoring Selection Programming Array for selecting the specific electronic sectoring configuration. This high-frequency oscillator signal is then frequency divided by the Sector Countdown Counter for the particular disk. The exact value of a count used for the division is determined by the respective Electronic Sector Programming Array. The count is synchronized to a specific disk by the associated synchronizer in conjunction with the index pulse derived for use with that particular disk. The pulse train output from the particular sector countdown counter has a repetition rate corresponding to the number of desired sectors as programmed by the respective Electronics Sector Programming Array. This pulse train is synchronized with the respective index pulse.

When electronic sectoring is selected by the Sectoring Selection Programming Array, this pulse train is fed directly to the respective pulse former.

4.8 MOTOR CONTROL

A functional element of disk rotational speed control is provided by the Motor Control circuitry. The current switching necessary to control drive current for the drive motor is provided by this subsystem. Additionally, provisions are made to accommodate drive motor operation at different line voltages in this subsystem.

The drive motor is a permanent split-phase induction motor with multiple windings to accommodate the two classes of line voltage operation. A permanent split induction motor requires the use of a capacitor or other type of phase shifting arrangement connected in series with the start winding (or windings). This is done to provide a current in that winding, phase shifted with respect to the main winding such that the net magnetic field produced by the windings is a pseudo rotating magnetic field. In the D3000 Disk Drive, motor capacitors mounted on the power supply chassis are connected to provide the phase shift of current in the start windings with respect to the main winding.

For 110v operation, main winding number 1 is connected in parallel with main winding number 2 and is operated directly from the line voltage. Current through the winding is switched on and off by a triac on the Motor Control PCBA. For 220v operation, main winding number 1 is connected in series with main winding number 2 and the series combination of these windings is operated directly from the line voltage. The current is switched on and off by the triac on the Motor Control PCBA. The motor capacitors are parallel-connected for 110v operation and series-connected for 220v operation.

Therefore, the effective arrangement for 110v operation is that the parallel combination of the motor capacitors is connected in series with the parallel combination of start winding number 1 and start winding number 2. This parallel series network is operated directly from the line voltage and is not switched by the triac. For 220v operation, the series combination of the motor capacitors is connected to the series combination of start winding number 1 and start winding number 2 and this series network is operated directly from the line voltage and is not switched by the triac. Thus, current flows in the start winding at all times when power is applied via the ON/OFF switch on the operator panel.

Torque will not be developed by the motor to an extent which will allow starting rotation of the disks unless the main winding is energized for a sufficient amount of time to provide the net rotating magnetic field. Likewise, sufficient torque to maintain rotation will be available only if the main winding is energized sufficiently often that the available field from a combination of the main and the start winding can provide the necessary torque to the load. Torque available from the drive motor is therefore provided by switching on and off the current in the main winding. The ability to control the speed of the drive motor and the torque that it supplies to the load is therefore contingent upon switching the triac on

the Motor Control PCBA at the correct times and allowing current to flow in the main winding as required.

The current amplification necessary to provide the high current drive for the gate of the triac is provided by transistor current switches on the Motor Control PCBA.

Since the main winding of the drive motor is an inductive load, there can exist a phase shift between the current through the motor and the applied voltage. This means that at the time the triac current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control will be lost. To achieve control with certain inductive loads, such as the drive motor, the rate of rise in voltage must be limited by a series R-C network across the triac. The capacitor limits the rate of change of voltage across the triac with respect to time; the resistor limits the surge of current from the capacitor discharging when the triac first conducts. It is also used to damp the ringing of the capacitance with the drive motor inductance and the inductance of a series inductor mounted on the Motor Control PCBA. This additional inductor is required to reduce transients caused by the triac switching into conduction.

4.9 POWER SUPPLY

Figure 4-13 is a block diagram of the drive power supply which is in two parts. The first part is the power supply module on the power supply chassis plate, which is fastened to the base casting, and contains the power transformer, rectifiers, capacitors, fuses, line filter, and power resistors. Three unregulated dc supplies are generated at nominal voltages of ± 25v and + 10v dc. Three ac supplies are generated at nominal voltages of ac line voltage, 8v ac (rms) and 25v ac (peak).

The second part of the power supply consists of the ± 12v and ± 5v voltage regulators which are located on the Servo PCBA. Interconnection between the two parts is provided by a harness from the power supply chassis which plugs into the Servo PCBA via a 12-pin connector. Interconnection for ac line voltage, ac common, and 8v ac (rms) to the Motor Control PCBA is provided via a 6-pin connector.

The transformer primary connections for several line voltages are shown in Figure 4-14. Line voltage is connected to the transformer via the ON/OFF switch. The ac line voltage is also used directly to power the drive motor and fan. Also, 8v ac (rms) and 25v ac (peak) are used for drive motor speed control circuits.

Unregulated dc (at a nominal ± 25v under load) is used to provide power to the positioner, voltage regulators, relay driver, and the solenoid driver. The voltage regulators generate four regulated supplies. The + 12 and − 5v supplies are zener regulated but not adjustable. The + 5v supply is adjustable and regulated.

All regulated dc voltages are protected against overvoltage by SCR *crowbar* protection circuits. When any of the regulated voltage lines exceeds its preset overvoltage value, the corresponding SCR fires. This holds the voltage down on the circuits connected to this voltage line until the fuse blows a few milliseconds later. The power resistors, in series with the unregulated ± 25v dc and + 10v dc, limit short circuit currents to a finite value when the SCR fires in the corresponding circuit. The bleeder resistors, provided across capacitors, discharge in the capacitors when the power supply input line cord is disconnected.

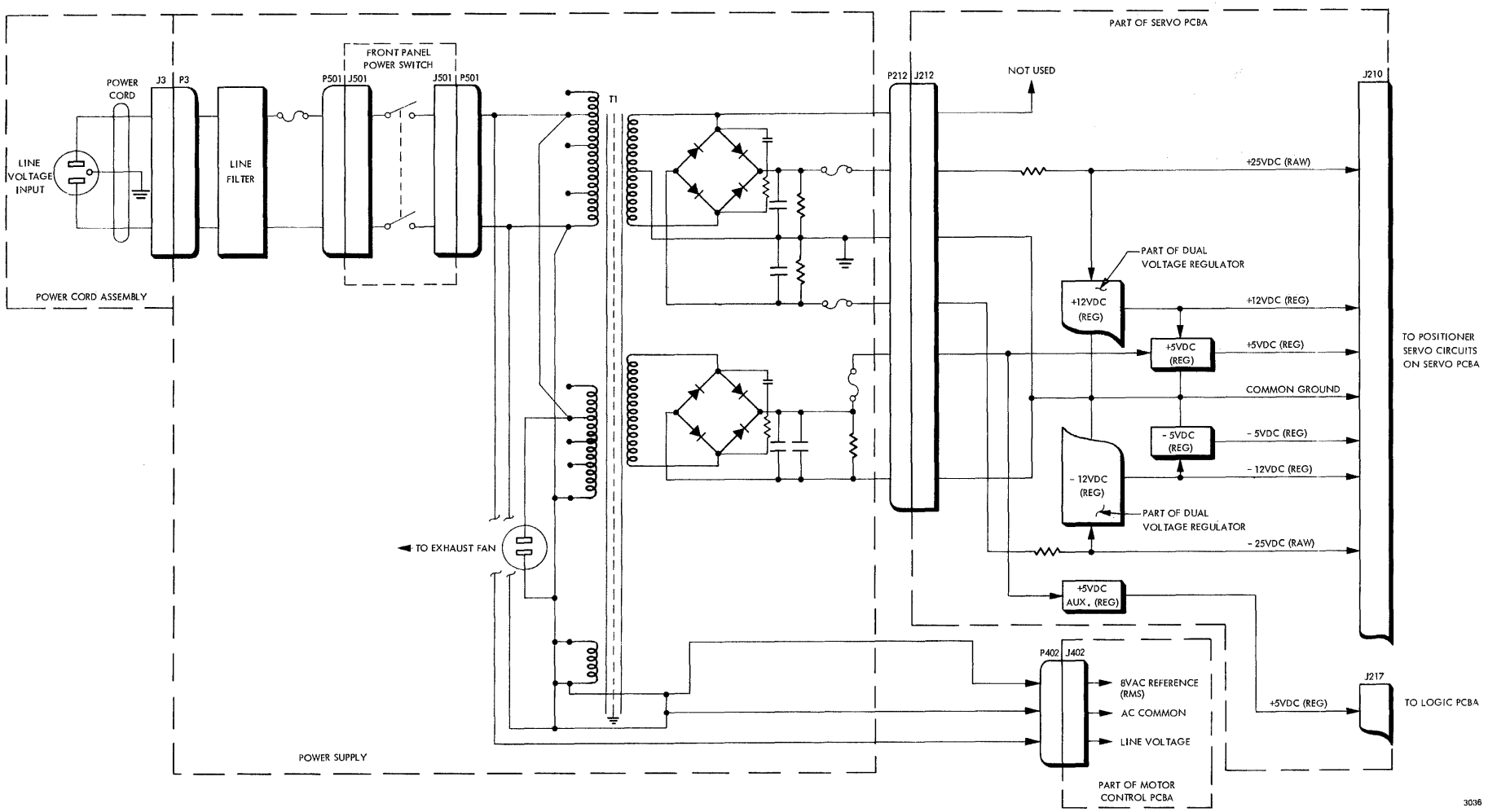
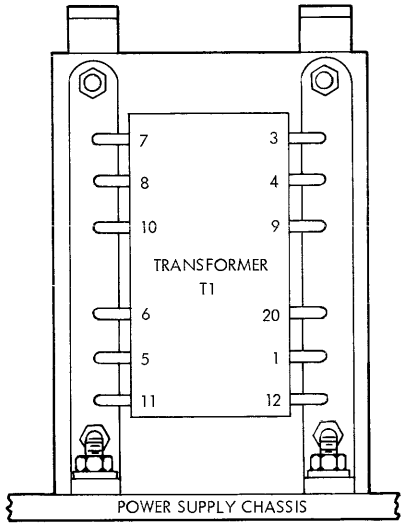


Figure 4-13. Power Supply Functional Block Diagram



LINE VOLTAGE	INPUT LINE BETWEEN	CONNECT
95	9 AND 3	9 TO 10 AND 3 TO 7
100	2 AND 3	2 TO 6 AND 3 TO 7
110	1 AND 3	1 TO 5 AND 3 TO 7
115	2 AND 4	2 TO 6 AND 4 TO 8
125	1 AND 4	1 TO 5 AND 4 TO 8
190	9 AND 7	3 TO 10
200	2 AND 7	3 TO 6
210	1 AND 7	3 TO 6
215	2 AND 7	4 TO 6
220	1 AND 7	3 TO 5
225	2 AND 7	4 TO 5
230	2 AND 8	4 TO 6
235	1 AND 7	4 TO 5
240	1 AND 8	4 TO 6
250	1 AND 8	4 TO 5

NOTE: FOR OPERATION AT OR BELOW 125V RMS THE TWO PRIMARY WINDINGS ARE OPERATED IN PARALLEL. FOR 200V RMS AND ABOVE THE TWO PRIMARY WINDINGS ARE OPERATED IN SERIES. THIS TABLE APPLIES TO POWER SUPPLY ASSEMBLY NUMBER 108151.

Figure 4-14. Transformer Primary Connections

4.10 TEMPERATURE COMPENSATION

Figure 4-15* is a functional block diagram of the temperature compensation circuitry used in both top and front load models. Two thermistors are employed; one to sense the ambient temperature of the removable disk and the other to sense the ambient temperature of the fixed disk(s). The analog signals from these thermistors are amplified and scaled to yield signals which are accurately related to temperature. These signals are then amplified and applied to the servo summing junction on the Servo PCBA and used as warm-up transient compensation.

The disk(s) ambient temperature signal is also compared to a temperature reference signal from the system compensation circuitry and the difference applied to a multiplying digital-to-analog converter. This converter also accepts as an input from the Logic PCBA the three most significant bits of the current address counter. These signals are then applied to the servo summing junction for compensation of the disk tracks.

In addition to temperature sensing circuitry, the Temperature Compensation PCBA includes logic to control the speed of the positioner assembly during emergency unloads. This protects the heads from crashing on the media if excessive speeds are reached by the positioner during the emergency unload condition.

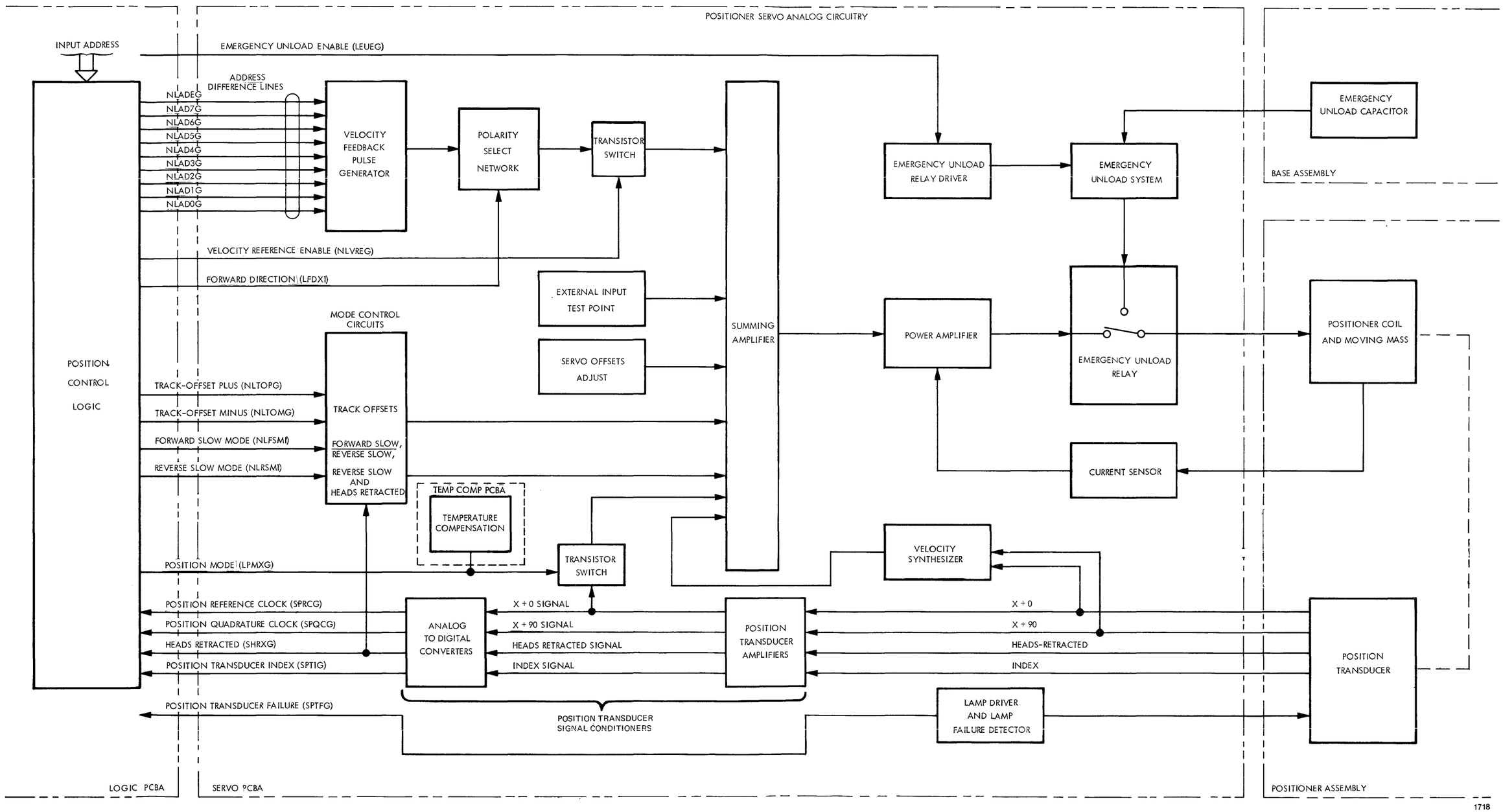


Figure 4-2. Positioner and Positioner Electronics, Functional Block Diagram

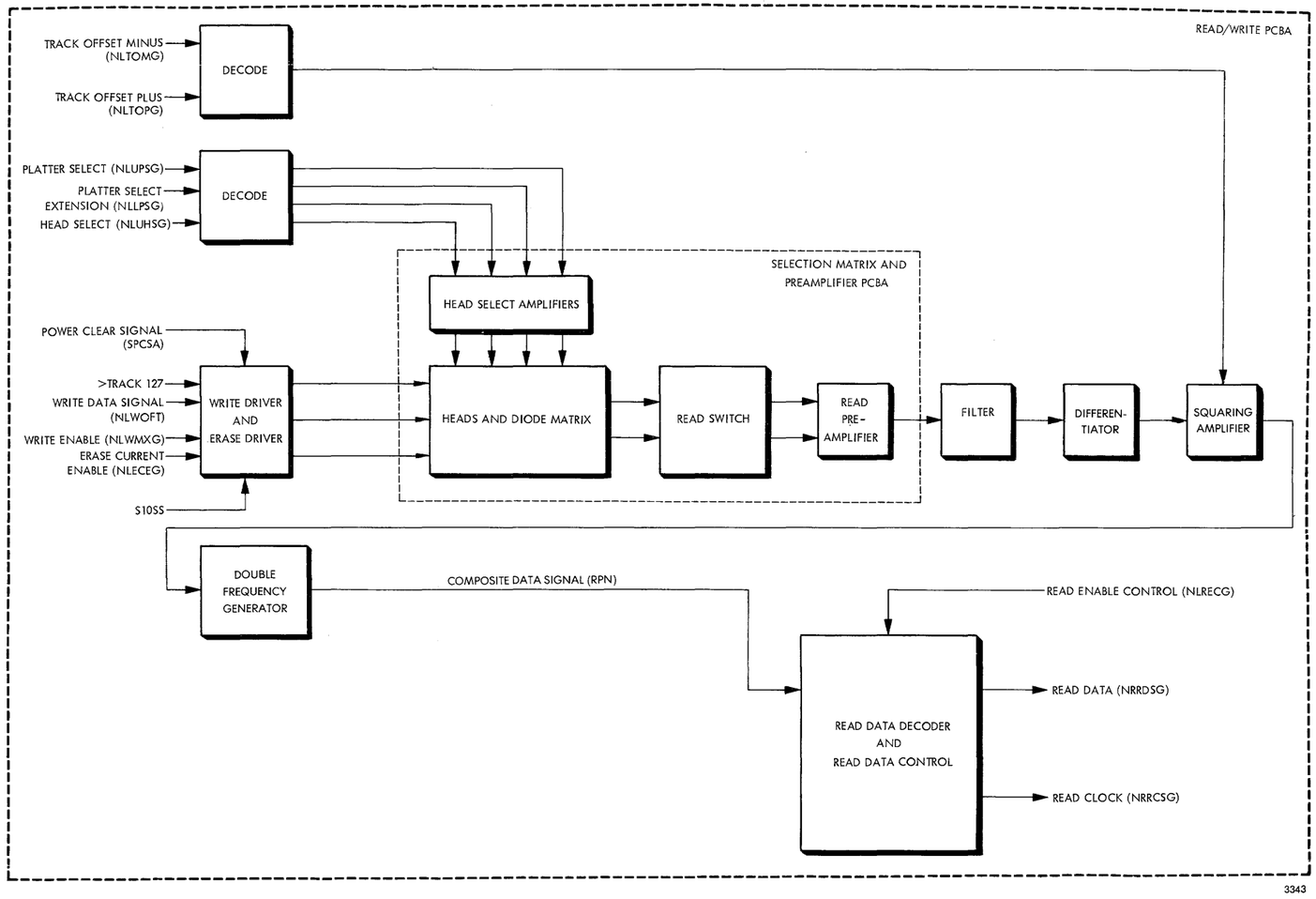


Figure 4-4. Read/Write Electronics, Functional Block Diagram

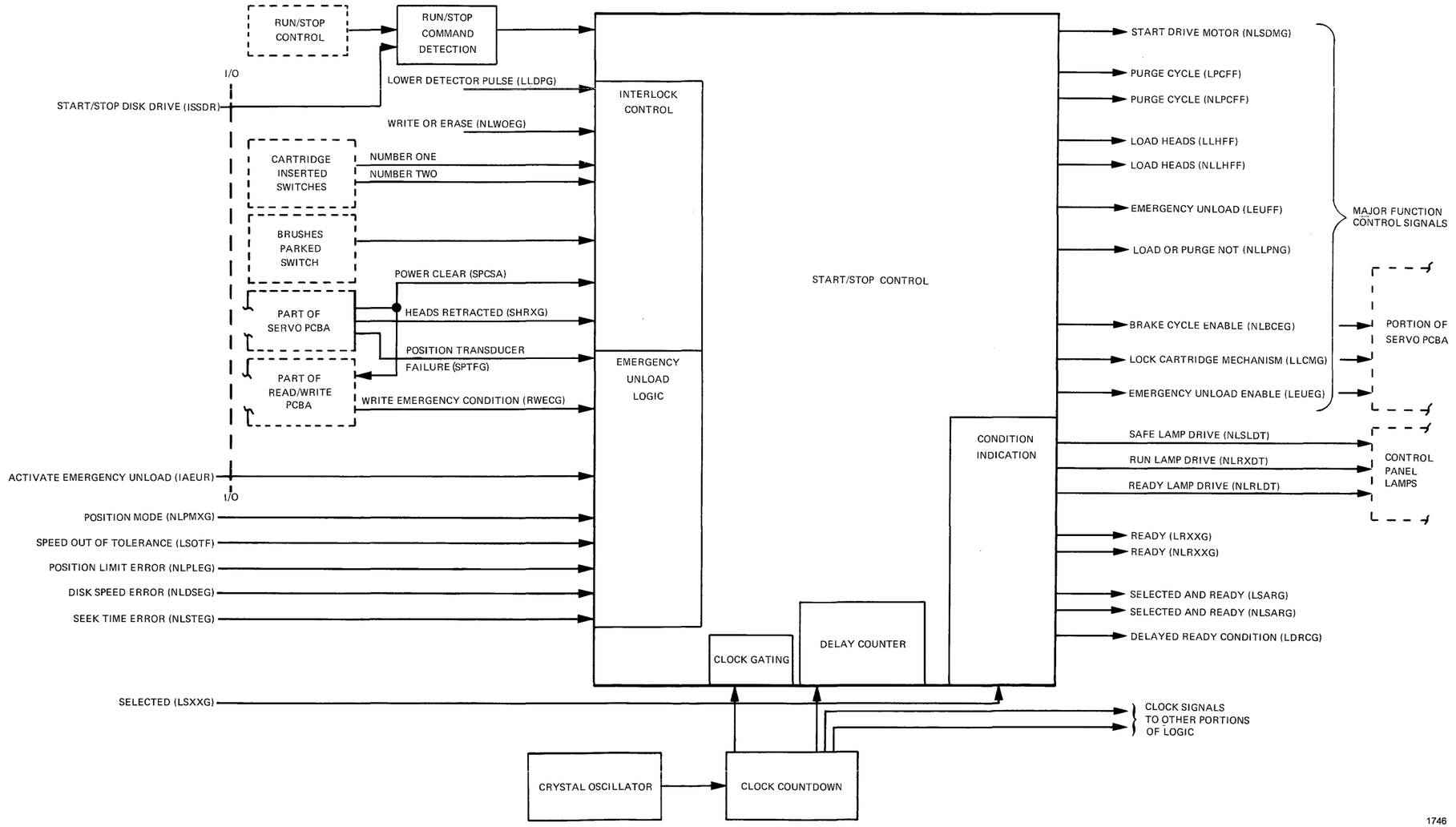
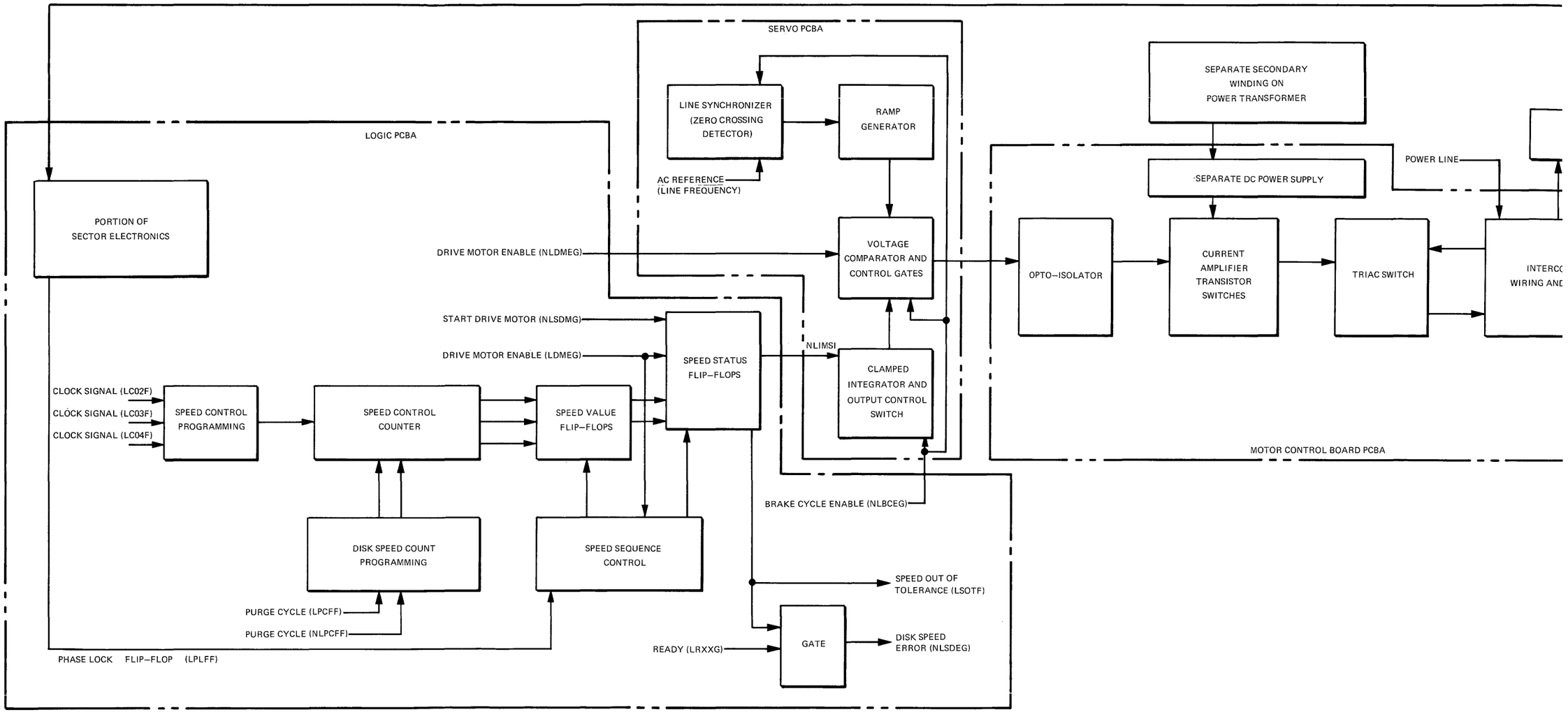


Figure 4-9. Start/Stop Control, Functional Block Diagram


LOGIC PCBA
PORTION OF SECTOR ELECTRONICS
SERVO PCBA
LINE SYNCHRONIZER (ZERO CROSSING DETECTOR)
RAMP GENERATOR
AC REFERENCE (LINE FREQUENCY)
DRIVE MOTOR ENABLE (NLDMEG)
VOLTAGE COMPARATOR AND CONTROL GATES
START DRIVE MOTOR (NLSDMG)
DRIVE MOTOR ENABLE (LDMEG)
SPEED STATUS FLIP–FLOPS
NLIMSI
CLAMPED INTEGRATOR AND OUTPUT CONTROL SWITCH
CLOCK SIGNAL (LC02F)
CLOCK SIGNAL (LC03F)
CLOCK SIGNAL (LC04F)
SPEED CONTROL PROGRAMMING
SPEED CONTROL COUNTER
SPEED VALUE FLIP–FLOPS
DISK SPEED COUNT PROGRAMMING
SPEED SEQUENCE CONTROL
PURGE CYCLE (LPCFF)
PURGE CYCLE (NLPCFF)
PHASE LOCK FLIP–FLOP (LPLFF)
BRAKE CYCLE ENABLE (NLBCEG)
SPEED OUT OF TOLERANCE (LSOTF)
READY (LRXXG)
GATE
DISK SPEED ERROR (NLSDEG)
SEPARATE SECONDARY WINDING ON POWER TRANSFORMER
SEPARATE DC POWER SUPPLY
POWER LINE
OPTO–ISOLATOR
CURRENT AMPLIFIER TRANSISTOR SWITCHES
TRIAC SWITCH
INTERCO
WIRING AND
MOTOR CONTROL BOARD PCBA

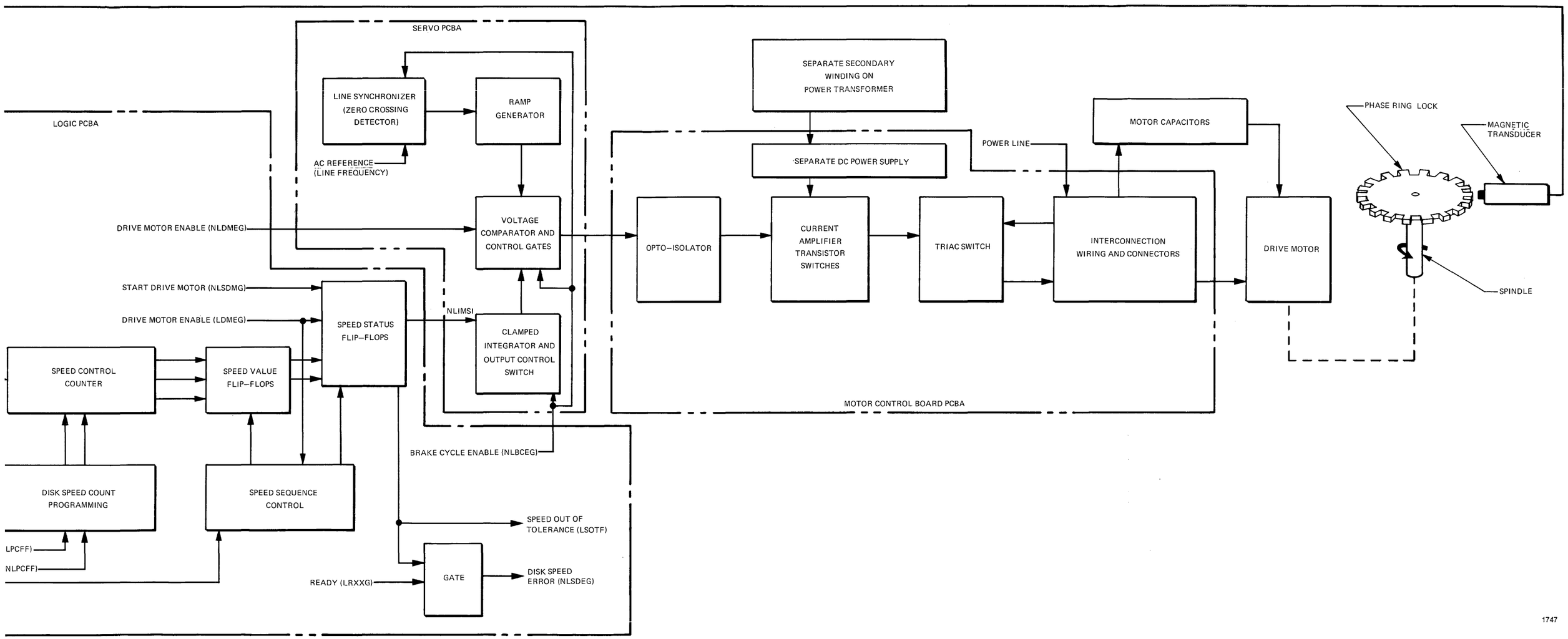


Figure 4-10. Spindle Speed Control, Functional Block Diagram

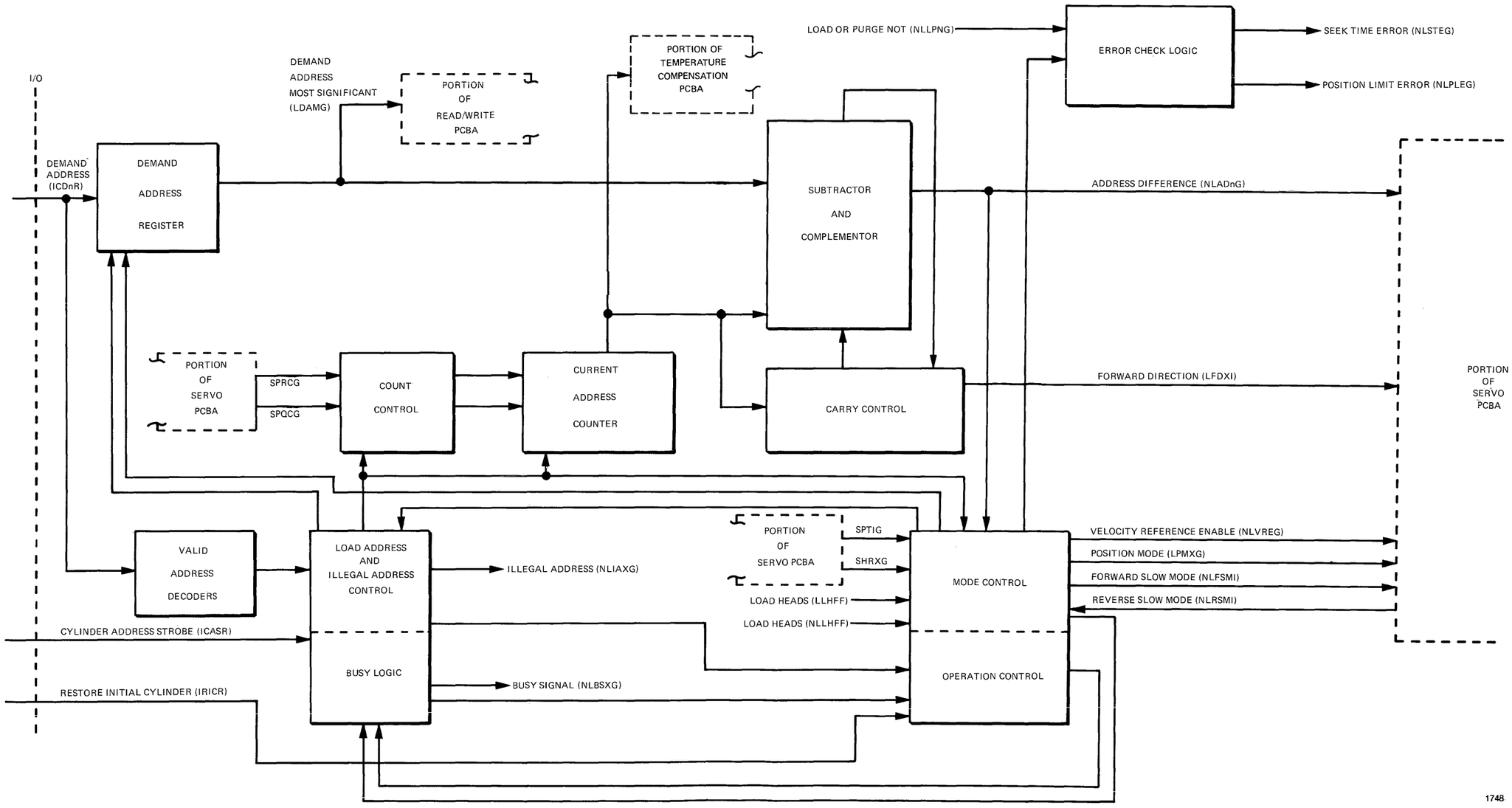
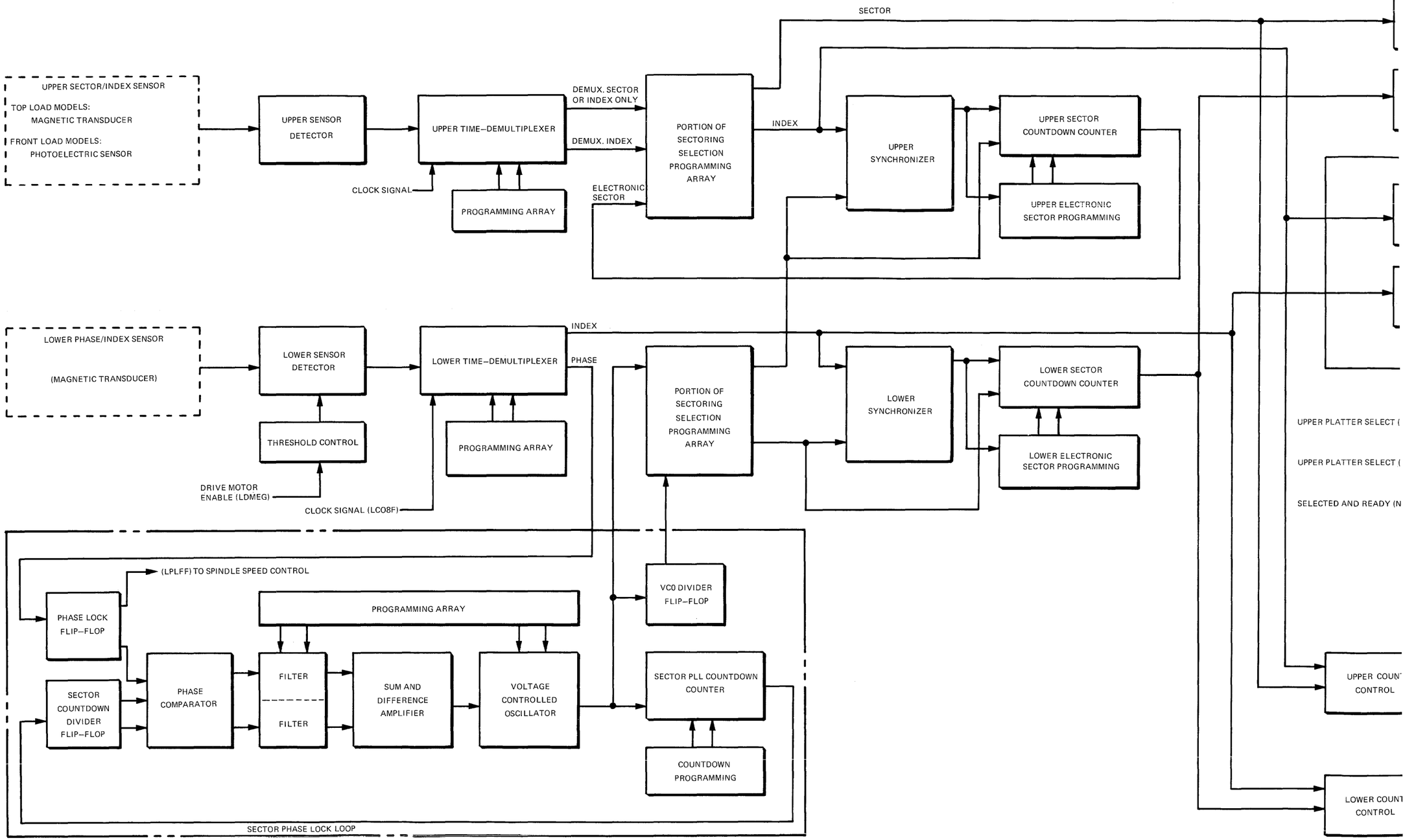


Figure 4-11. Position Control Logic, Functional Block Diagram


UPPER SECTOR/INDEX SENSOR
TOP LOAD MODELS:
MAGNETIC TRANSDUCER
FRONT LOAD MODELS:
PHOTOELECTRIC SENSOR
UPPER SENSOR DETECTOR
UPPER TIME–DEMULTIPLEXER
CLOCK SIGNAL
PROGRAMMING ARRAY
DEMUX. SECTOR OR INDEX ONLY
DEMUX. INDEX
ELECTRONIC SECTOR
PORTION OF SECTORING SELECTION PROGRAMMING ARRAY
SECTOR
INDEX
UPPER SYNCHRONIZER
UPPER SECTOR COUNTDOWN COUNTER
UPPER ELECTRONIC SECTOR PROGRAMMING
LOWER PHASE/INDEX SENSOR
(MAGNETIC TRANSDUCER)
LOWER SENSOR DETECTOR
LOWER TIME–DEMULTIPLEXER
THRESHOLD CONTROL
PROGRAMMING ARRAY
DRIVE MOTOR ENABLE (LDMEG)
CLOCK SIGNAL (LC08F)
PHASE
PORTION OF SECTORING SELECTION PROGRAMMING ARRAY
LOWER SYNCHRONIZER
LOWER SECTOR COUNTDOWN COUNTER
LOWER ELECTRONIC SECTOR PROGRAMMING
(LPLFF) TO SPINDLE SPEED CONTROL
PHASE LOCK FLIP–FLOP
PROGRAMMING ARRAY
VCO DIVIDER FLIP–FLOP
SECTOR COUNTDOWN DIVIDER FLIP–FLOP
PHASE COMPARATOR
FILTER
FILTER
SUM AND DIFFERENCE AMPLIFIER
VOLTAGE CONTROLLED OSCILLATOR
SECTOR PLL COUNTDOWN COUNTER
COUNTDOWN PROGRAMMING
SECTOR PHASE LOCK LOOP
UPPER PLATTER SELECT (
UPPER PLATTER SELECT (
SELECTED AND READY (N
UPPER COUN
CONTROL
LOWER COUNT
CONTROL

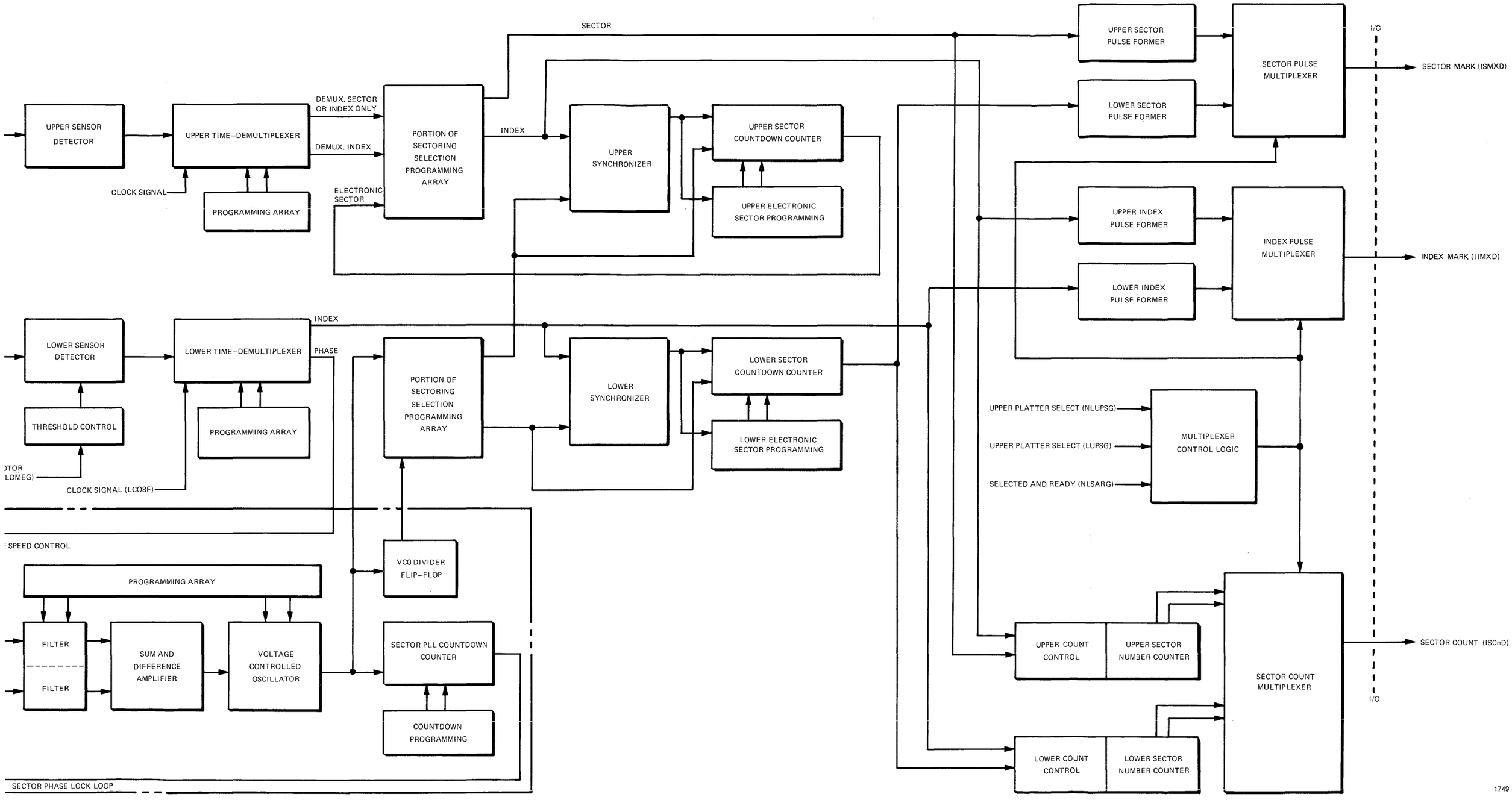


Figure 4-12. Sector Electronics, Functional Block Diagram

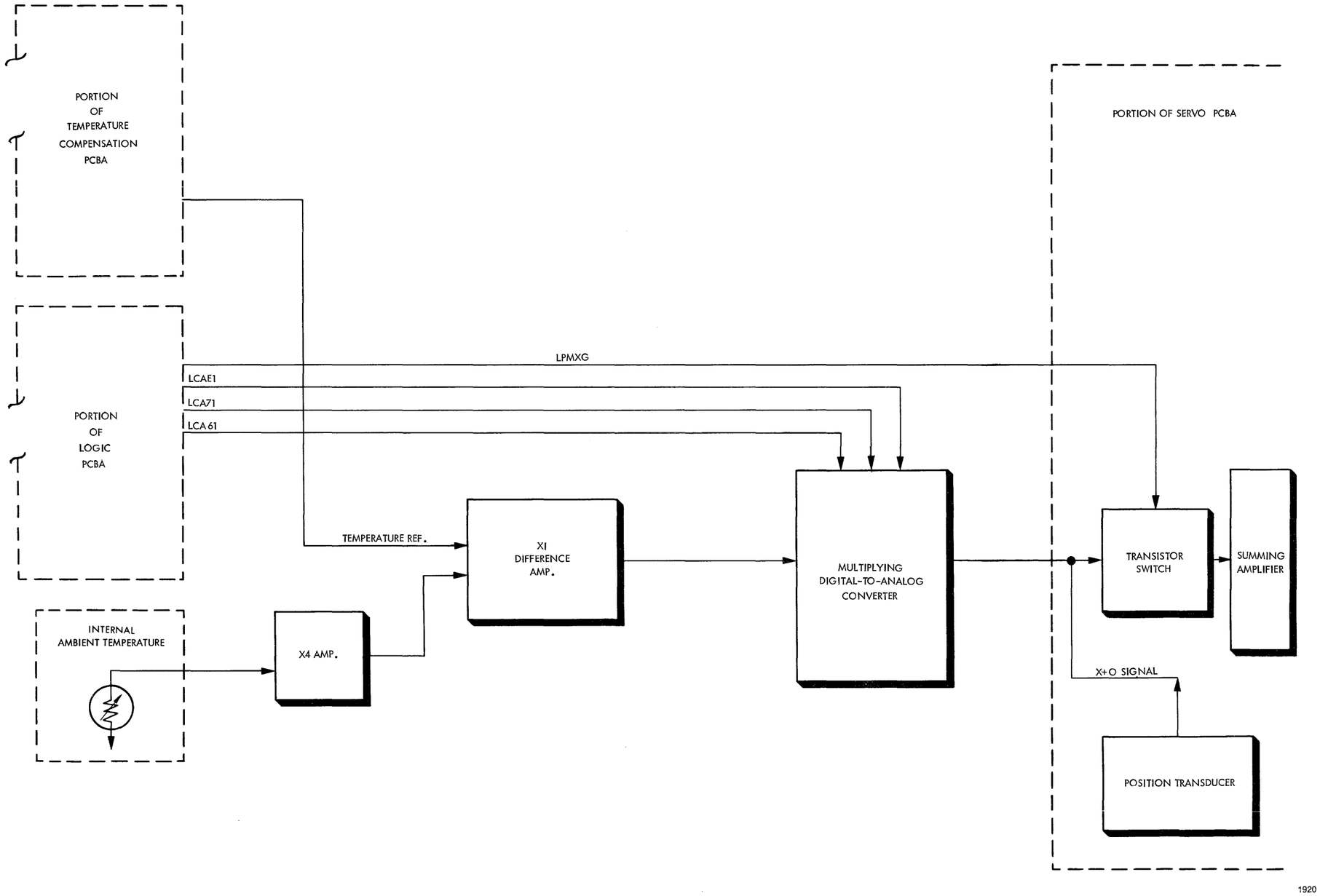


Figure 4-15. Temperature Compensation Functional Block Diagram

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SECTION V
DETAILED ELECTRICAL AND LOGIC DESCRIPTION

5.1 INTRODUCTION

This section contains the theory of operation of the PCBAs used in the D3000 Series Disk Drives. Schematic and assembly drawings for each board are contained at the end of Section VII.

5.2 LOGIC TERM MNEMONIC IDENTIFICATION

All digital signals in the D3000 Disk Drive are identified by a name which will be referred to as the logic term. Logic terms may be descriptive of a condition or an event, or they may be a generalized name used primarily for documentation purposes. If a descriptive name is essential to facilitate the understanding of a function, a generalized term is not used.

Appendix A of this manual contains the mnemonic listing for the D3000 Series Disk Drive. An understanding of the mnemonic scheme is essential to the total understanding of the D3000 logic drawings. Also included in Appendix A are figures and tables which provide the user with an understanding of the six character logic term.

5.3 SERVO PCBA

The following paragraphs describe the Servo PCBA installed in the D3000 Series Disk Drive. Refer to Schematic No. 108130 and Assembly 108131.

The Servo PCBA is approximately 254 mm (10 inches) square with two connectors along one edge. Figure 5-1 illustrates the placement of each connector, test point, and adjustable component on this board. J201 and J202 are the connectors which connect via mating plugs and 3M flat cables to the Logic PCBA. The remainder of connectors are of the Molex type.

In general, the connectors perform the following functions.

(1) Electrically connect the Servo PCBA to all base-casting-mounted assemblies, e.g., power supply, positioner coil, position transducer, emergency unload capacitor, cartridge lock solenoid, and heatsinks.

(2) Provide power to the Logic PCBA.

(3) Provide a path for signals and levels between the Servo and Logic PCBAs.

(4) Provide a path for the + 5v and control signals to the motor control board.

(5) Provide a path for temperature compensation and emergency unload signals from the Temperature Compensation PCBA to the Servo PCBA.

Contained on the Servo PCBA are the electronics for voltage regulators, positioner, emergency unload system, ac motor speed control circuits, cartridge lock solenoid driver, and power clear circuit. The following paragraphs describe the circuits associated with each of the connectors.

5.3.1 VOLTAGE REGULATORS

The power supply voltage regulators are shown on Schematic No. 108130, sheet 2. J212 (zone H16) connects unregulated + 25v, − 25v, + 10v to the Servo PCBA. Note that two pins are allocated to each of the high current lines to reduce current density in the pins.

The dual in-line regulator, U18 (zone F13), furnishes the regulated + 12v dc and − 12v dc voltages. Q1 (zone H12) and Q2 (zone D12) are the current pass transistors for the + 12v dc and − 12v dc regulated voltages, respectively.

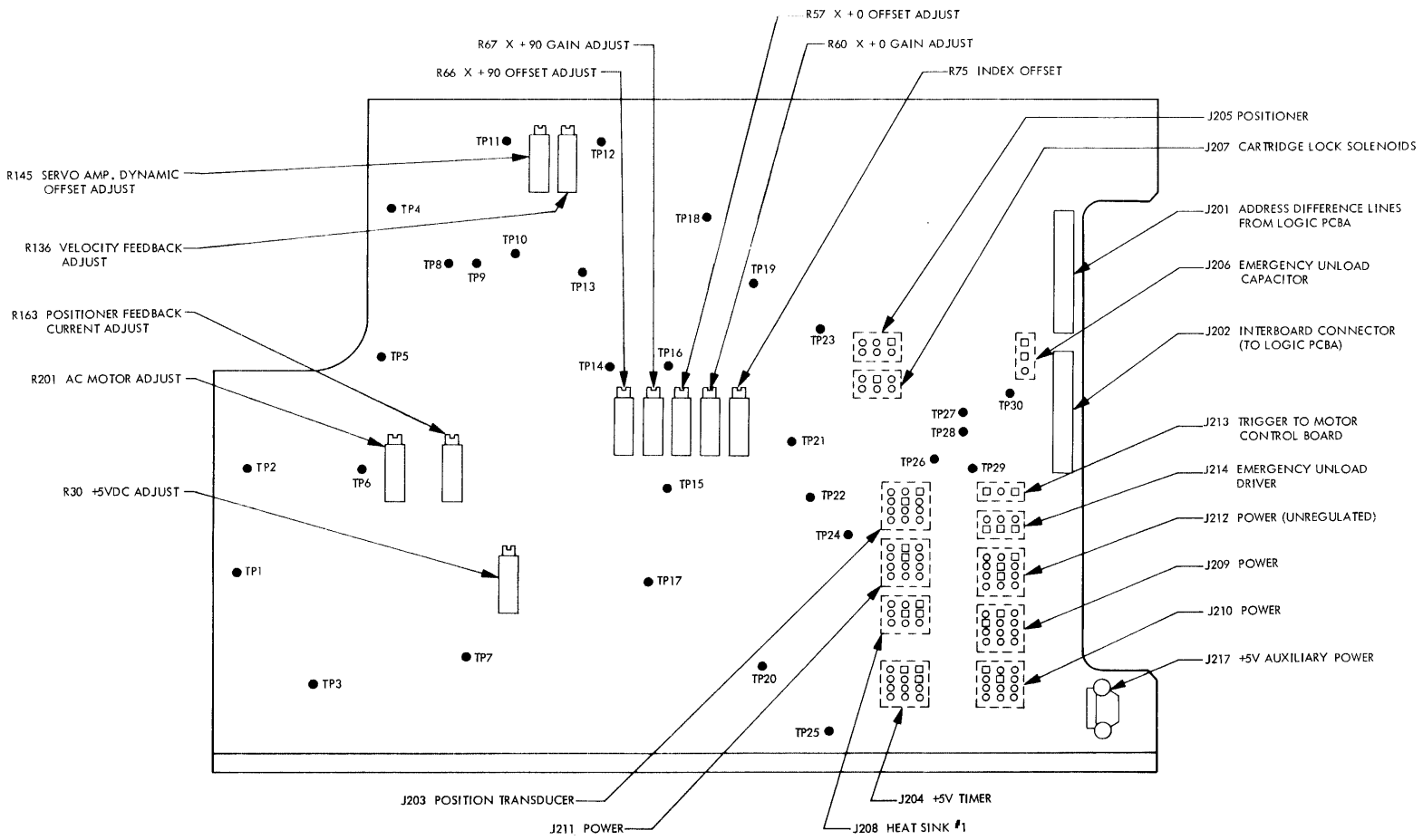

Figure 5-1. Servo PCBA Test Point and Connector Placement

The + 5v and − 5v regulators consist of U21 (zone B12) and U11 (zone E12), respectively. Potentiometer R30 (zone B12) regulates the output of the + 5v regulator and can be monitored at TP24. Operational amplifier U15 is used as a voltage follower in the regulating circuit. The high open-loop gain of the operational amplifier in the feedback regulating circuit offers improved line and load regulation characteristics to the − 5v supply. Zener diode VR3 provides the voltage reference for the − 5v.

Regulator power transistors Q1, Q2, and Q3 are mounted on heatsinks external to the Servo PCBA. J204 and J208 connect the regulators to the external heatsink.

A *crowbar* over-voltage protection circuit is provided for the + 5v and − 5v supplies. These circuits are employed to detect an increase of 3v in the + 5v supplies. Zener diodes VR7 (zone B11) and VR4 (zone E10) detect an increase in the + 5v and − 5v supplies, respectively. An increase to + 8v or − 8v causes SCR3 or SCR2 to fire, which in turn causes the + 10v or − 25v fuse on the power supply module to blow, thus removing the relevant voltage supply.

A *crowbar* over-voltage protection circuit is also provided on the + 12v and − 12v supplies and employs zener diodes VR1 and VR2 (zone F12), and VR5 and VR6 (zone E10), respectively, to detect an increase in the 12v supplies. A voltage increase to + 15v or − 15v causes SCR1 or SCR2 to fire, which in turn causes the + 25v or − 25v fuse on the power supply module to blow, thus removing the relevant 25v supply.

J209 (zone H14) and J211 (zone D14) are jumper plugs which connect unregulated ± 25v to circuits on the Servo PCBA. These jumper plugs enable the isolation of the regulators and power supply for maintenance purposes.

The unregulated 25v supplies are used in the positioner power amplifier and the power clear circuit. In addition, the − 25v supply is used in the emergency unload relay driver. The 5v regulators supply power to the digital ICs, mode control electronics, ac motor control circuit, relay driver, and cartridge lock solenoid driver. The 12v regulators supply power to the operational amplifiers, velocity function generator, mode control electronics, position transducer signal conditioners, and position transducer lamp driver.

5.3.2 POSITIONER SERVO ELECTRONICS

The positioner electronics consists of the Velocity Function Generator, Mode Control circuits, Position Transducer Signal Conditioners, Velocity Synthesizer, Summing Amplifier, Positioner Power Amplifier, Position Transducer Lamp Driver Failure Detector, and the Emergency Unload System. Refer to Paragraph 5.2 for a definition of logic term mnemonics used in the following descriptions.

J201 provides a path for the majority of logic command signals for the positioner servo system from the Logic PCBA to the Servo PCBA. J202 provides a path for the remaining logic signals from the Logic PCBA to the Servo PCBA, and vice versa.

5.3.2.1 Velocity Function Generator

The Velocity Function Generator is shown on Schematic No. 108130, sheet 2. This circuit generates a step voltage signal of known polarity (positive or negative) which can be monitored at TP18 (zone H2). The polarity of this signal is dependent upon the state of logic command signals NLAD1G through NLAD7G, NLADEG, and LFDX1. Assume that the address difference is non-zero and is such that the signals at pins 18, 27, 28, 29, 30, 33, 31, 32 of J201 are in the logic low state, i.e., signals are active. Correspondingly, the output logic state of IC U44 pins 11, 3, 6, and 8, plus U40 pins 3, 8, and 6 will be high causing diodes CR5, CR7, CR9, CR11, CR13, CR15, and CR17 to be reverse biased.

Diodes CR6, CR8, CR10, CR12, CR14, CR16, and CR18 are forward biased and current flowing through resistor network R40 and R47, R48 and R49, etc., is summed at the summing junction (pin 2) of operational amplifier U30 (zone H3). The output at TP18 will be ± 6v depending on the state of Forward Direction (LFDX1) logic signal. When LFDX1 is high, the output at TP18 will be + 6v and when LFDX1 is low, the output at TP18 will be − 6v. Similarly, when the address difference is zero, the state of the logic command signals (NLAD1G through NLADEG) is such that the output logic state of IC U44 pins 11, 3, 6, and 8, plus IC U40 pins 3, 8, and 6 will be low, and diodes CR5, CR7, CR9, CR11, CR13, CR15 and CR17 will be forward biased. Diodes CR6, CR8, CR10, CR12, CR14, CR16, and CR18 are reverse biased and no current flows from the resistor network into the summing junction of U30 except from R53. Consequently, the output of TP18 will be + 0.3v depending on the state of logic signal LFDX1.

A third possibility exists when the address difference is non-zero and the state of signals NLAD1G through NLADEG is such that some of the output logic states at the outputs of U44 pins 11, 3, 6, and 8, plus U40 pins 3, 8, and 6 are high and others are low. In that case, the output at TP18 will be a voltage step between + 6v and − 6v depending on the output logic states of U40, U44, and the LFDX1 signal.

Velocity Reference Enable (NLVREG) going low at pin 20 of J201 turns U23 (zone G7) on and SVRVA current flows through R134 into the summing junction (pin 2) of the summing amplifier U16 (zone G6). When NLVREG is high, U23 is turned off and no current flows into the summing junction of U16. Hence, U23 acts as a switch that enables the output of U16 which can be observed at TP9.

5.3.2.2 Mode Control

The Mode Control circuitry is shown on Schematic No. 108130, sheet 3. When Track Offset Plus (NLTOPG) at pin 26 of J201 (zone G13) is low and Track Offset Minus (NLTOMG) at pin 25 of J201 is high, the signal at the output of U12 pin 7 will be − 4.5v ± 0.5v. Conversely, a high state of NLTOPG and a low state of NLTOMG will make the voltage at the output of U12 pin 7 + 4.5v ± 0.5v. When NLTOPG and NLTOMG both are high, the voltage at the output of U12 pin 7 will be 0v.

Forward Slow Mode (NLFSM1) low at pin 24 of J201, Reverse Slow Mode (NLRSM1) high at pin 23 of J201, and the high output of U25 pin 4 (i.e., Heads Retracted (SHRXG) low at TP13, zone C15) causes the signal at U16 pin 6 (zone G6) to be − 0.55v ± 0.05v. Conversely, when NLFSM1 is high, NLRSM1 is low and SHRXG is low, the signal at U16 pin 6 is − 0.55v ± 0.05v. When NLFSM1 is high, NLRSM1 is low and SHRXG is high, the signal at U16 pin 6 is approximately 0.11v. Finally, when NLFSM1 and NLRSM1 are high, regardless of the state of SHRXG, the voltage at U16 pin 6 is 0v.

Potentiometer R145 (zone G7) is used to adjust the dc offsets when the servo is in the Position Mode. TP11 and R143 (zone H7) provide a means to introduce an external perturbation signal into the summing amplifier.

5.3.2.3 Position Transducer Signal Conditioner

The Position Transducer Signal Conditioner circuitry (zone H17) is shown on Schematic No. 108130, sheet 3. These circuits are employed to amplify the low level position transducer signals (X + 0, X + 90, Index, and Heads Retracted) and convert them to appropriate logic signals (SPRCG, SPQCG, SPTIG, and SHRXG). J203 (zone A—H18) connects all position transducer signals and velocity synthesizer signals to the Servo PCBA. Outputs from the Position Transducer Signal Conditioners are routed to the Logic PCBA via edge connector J202 (zones A—H15).

Figure 5-2 describes the position transducer output signals, namely Heads Retracted, Index, X + 0 and X + 90, at pins 6, 1, 3, and 2, respectively, of connector J203, as the positioner carriage is moved in the forward direction, i.e., toward the spindle. The amplitude of the Heads Retracted and Index signal is approximately 10 mv at pins 6 and 1 of J203. The amplitude of X + 0 and X + 90 signal is approximately 120 mv to 200 mv at pins 3 and 2 of J203.

The output of the Heads Retracted, Index, X + 0, and X + 90 amplifiers can be monitored at TP13, TP16, TP14, and TP19, respectively. Figure 5-3 describes the output of these amplifiers and should be referenced in conjunction with Figure 5-2.

Potentiometers R57 (zone H18), R66 (zone F18), and R75 (zone E18) provide dc bias for balance adjustments of the X + 0, X + 90, and Index signals, respectively. R60 (zone H17) provides gain adjustments for the X + 0 signal at TP21. Type 741 operational amplifiers (U38, U37, U34, and U33) are used as high gain inverting amplifiers to amplify these signals. Potentiometer R69 (zone F17) provides gain adjustments for the X + 90 signal at TP15.

When R60 (the X + 0 gain potentiometer) and R57 (the balance potentiometer) are properly adjusted, the output at TP21 should be 4v peak-to-peak. When R69 (the X + 90 gain potentiometer) and R66 (the balance potentiometer) are properly adjusted, the X + 90 amplifier output at TP15 should be 4v peak-to-peak. The change in transition (from positive to negative and vice versa) at TP27 should be from − 3v to + 3v and vice versa when R75 (the Index balance potentiometer) is properly adjusted.

The amplified Heads Retracted, Index, X + 0, and X + 90 signals shown in Figure 5-2 are then converted into their corresponding logic signals shown in Figure 5-3, namely, SHRXG, SPTIG, SPRCG, and SPQCG. These logic signals can be monitored at TP13, TP16, TP14, and TP19, respectively. Type 75107 dual line receivers U19 and U20 are used in the circuit as comparators for analog-to-digital conversion.

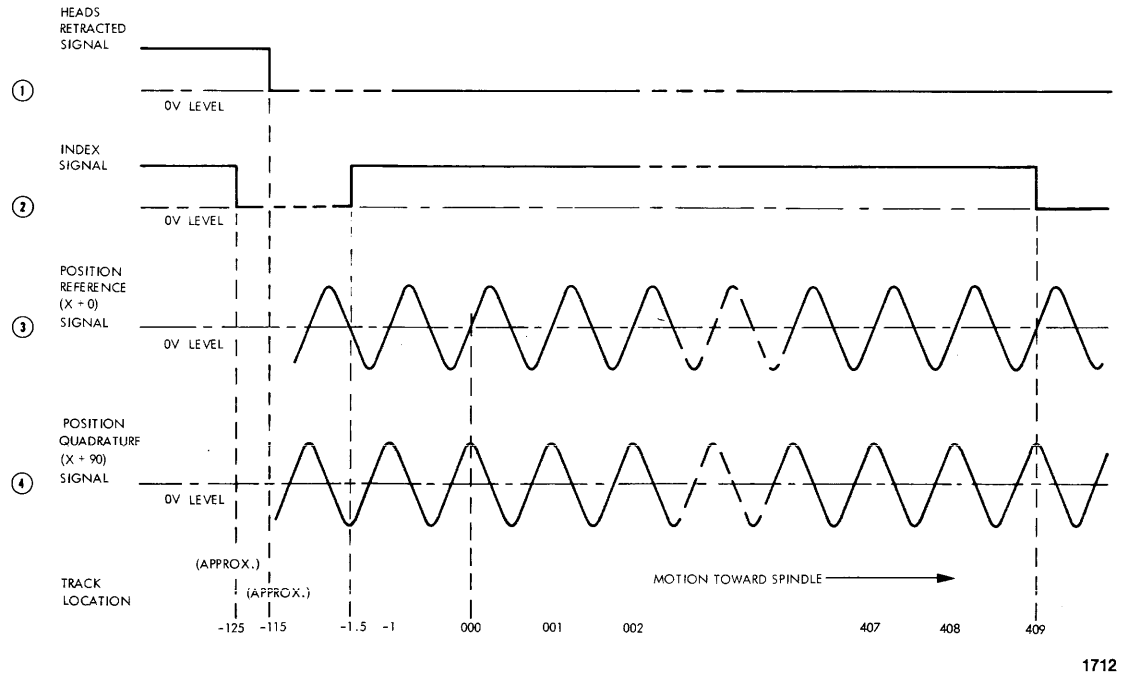

Figure 5-2. Position Transducer Output Signals

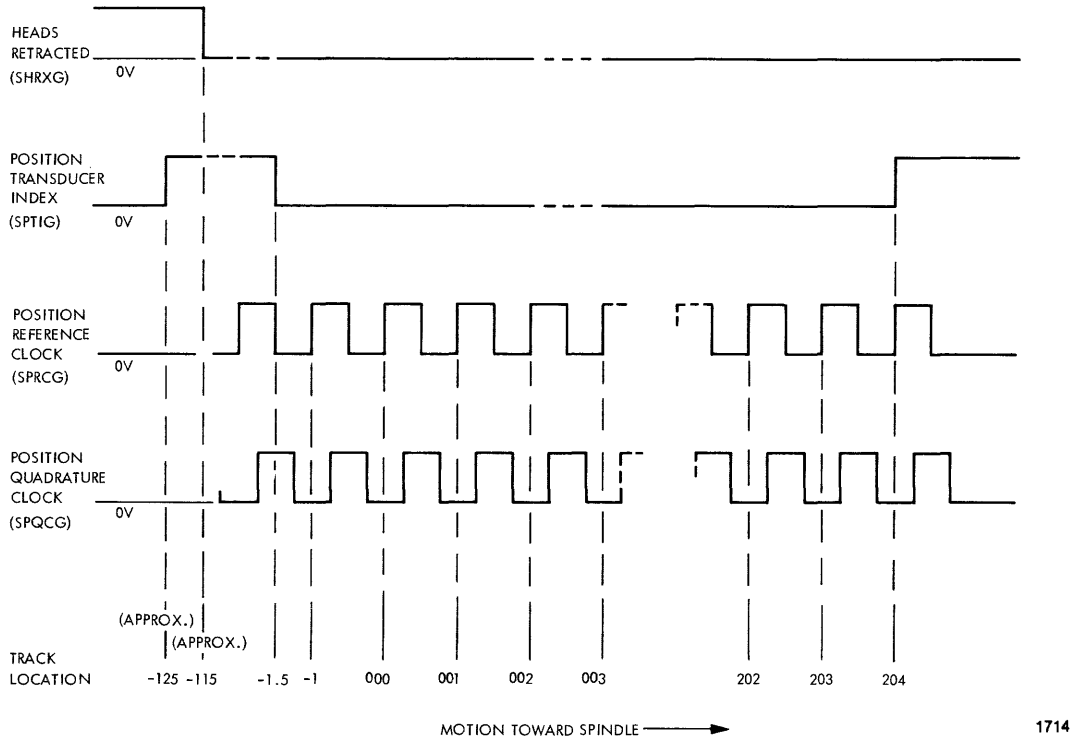

Figure 5-3. Position Transducer Signal Amplifier Outputs

The R-C network in the feedback loop around comparators U19 and U20 provides ac and dc hysteresis. An example of this network is C32, R81, R82, and R83 in the feedback path of U19 (zone D16). These networks assure a single transition crossover detection of the analog input signals and provide good dc noise margins for analog inputs to the comparators.

5.3.2.4 Velocity Synthesizer

The Velocity Synthesizer circuitry shown on Schematic 108130, sheet 3, uses the X + 0 and X + 90 signals (converted to their logic signals) to develop positioner velocity by hybrid (digital and analog) means. This circuit synthesizes the time derivative of the position of the head carriage. The resulting differentiation is then used as a null signal for the Position Power Amplifier.

The signal at U29-11 (zone B14) consists of the exclusive-OR of the X + 0 and X + 90 signals, which results in a signal that changes state twice as often as either signal. This is applied to two shift registers, U35 and U36 (zone B13) in series. Two taps on these registers are combined by another exclusive-OR gate at U29-3 (zone C12). The resultant output is high for a predetermined interval after U29-11 changes state. Thus, the ratio of this interval to the total interval between transitions at U29-11 is a measure of the velocity of the positioner carriage. This ratio is computed in the analog portion of the circuit by U17 (zone C10), which is operated as a low-pass filter, but whose function is equivalent to that of a passive integrator. The resulting analog voltage at U17-6 is equivalent to approximately + 10v per inch per second of positioner carriage velocity. This voltage, however, is always positive, so U15 (zone C9) is used to invert this signal whenever SFWDG from the velocity polarity generator is low. This voltage is then applied to the servo summing junction via U23-6 (zone G8) whenever the servo is in the velocity mode.

5.3.2.5 Summing Amplifier

The Summing Amplifier U16 (zone G6) is shown on Schematic No. 108130, sheet 3. This amplifier sums the following reference, feedback, or control signals of the positioner servo system.

(1) Velocity reference signal.

(2) Velocity feedback signal.

(3) (X + 0) position feedback signal.

(4) Offset signal.

(5) Track offset plus and track offset minus signal.

(6) Reverse slow velocity mode, forward slow velocity mode, and reverse slow and heads up velocity mode signal.

(7) External perturbation input signal.

(8) Temperature compensation and head alignment (200 tpi).

The positioner servo system normally operates in the Velocity Mode. Velocity feedback is provided continuously except when Reverse Slow Mode (NLRSM1) is low and Heads Retracted (SHRXG) is high (i.e., the servo is in the Reverse Slow Mode and the heads are retracted), then velocity feedback is cut off.

The Velocity Reference Enable signal (NLVREG, pin 20 of J201) going low turns on U23 pin 2 (zone G7) and enables the velocity reference signal into the summing junction of U16 (zone G6). The Position Mode signal (LPMXG, pin 22 of J201) going high turns on U23 pin 15 (zone G7) enabling the X + 0 signal from U12 pin 1 (zone F10) into the summing junction of U16. Thus, the servo is placed in the Position Mode.

The Forward Slow Mode signal (NLFSM1) low and Reverse Slow Mode signal (NLRSM1) high at pins 24 and 23 of J201, respectively, introduces a Forward Slow Mode signal into the summing junction of U16. Conversely, NLFSM1 high and NLRSM1 low introduces a Reverse Slow Mode signal into the summing amplifier.

Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) signals are introduced at the summing junction of U16 only when the servo is in the Position mode of operation. NLTOPG (pin 26 of J201) low and NLTOMG (pin 25 of J201) high introduces the Track Offset Plus signal; NLTOPG high and NLTOMG low introduces the Track Offset Minus signal into the summing junction of U16. TP11 is provided to introduce an external perturbation signal into the summing junction. Potentiometer R145 (zone G7) is provided for nulling the signal at TP9 in reference to servo ground.

Referring to the summing junction of U16, the amplifier gains for any particular input signal is determined by the ratio of feedback resistor R144 (zone H6) and the resistor in series with the input signal. For example, the gain of the summing amplifier for any external input signal at TP11 (external perturbation signal) is R144 divided by R143. Zener diodes VR10 and VR11 (zone G6) are employed to limit the output of summing amplifier at TP9 to ± 6v. TP10 is the test point for servo ground. It should be noted that servo ground is depicted on the schematic as G(S) and logic ground is shown as G(L). The summing junction of U16 (pin 2) also receives the Temperature Compensation signal from the Temperature Compensation PCBA via pin 6 of connector J215 (zone F9), U12 and U23.

5.3.2.6 Positioner Power Amplifier

The Positioner Power Amplifier is shown on Schematic No. 108130, sheet 3 (zone G5). This amplifier is a linear feedback transconductance amplifier. It is referred to as a transconductance amplifier because its output current is proportional to the input voltage to the power amplifier.

The input to the power amplifier circuit is the output signal of Summing Amplifier U16, which can be monitored at TP9. When the signal at TP9 is positive, Q17 turns on causing Q5 to conduct which, when relay K1 (zone C2) is energized, connects – 25v through R172, the positioner coil via J205, and R164 to ground. Conversely, when the signal at TP9 is negative, Q15 turns on, causing Q4 to conduct which, when relay K1 is energized, connects + 25v through R156, the positioner coil via J205 and R164 to ground.

J205 (zone C1) connects the positioner coil to the Servo PCBA, thus establishing a path for current through the coil and corresponding series resistors. The voltage drop across R164, which is proportional to the current through R164, is fed back to the power preamplifier U14 (zone G5). U14 compares the input voltage and the feedback voltage which is proportional to the current through the coil, and turns off Q17 or Q15 and Q5 or Q4 when the output current at TP22 is equal to some constant of proportionality times the input voltage at TP9. Potentiometer R163 (zone F5) is provided to adjust and vary this trans-conductance of the power amplifier.

Q16 (zone G4) and Q18 (zone E4) limit the maximum output current of the amplifier. The voltage drop across R172 or R156, and the value of R171 and R170 or R155 and R154 determine the maximum value of current through Q5 or Q4, respectively.

Additional current limiting is provided by VR10 and VR11, which limit the voltage and the adjustment of R163 to + 6v at TP9. This value of current is normally adjusted lower than that provided by the limiting values of Q16 and Q18.

Resistors R160 and R161 (zone F4) provide an internal voltage feedback loop in the power amplifier stage. R-C networks C45 and R157, C47 and R167, C46 and R168 assure the high frequency stability of the power amplifier and eliminate high frequency oscillations.

5.3.2.7 Position Transducer Lamp Failure Detector

J203 pins 10 and 12, shown on Schematic No. 108130, sheet 3 (zone A18), connect the Position Transducer Lamp to the Servo PCBA. In normal operation, the lamp is driven from + 5v with resistor R93 in series between the lamp and ground. When the lamp is illuminated the voltage drop across R93 turns on U1. Thus, the Position Transducer Failure signal (SPTFG) at pin 18 of J202 is low. Should the lamp fail, U1 is turned off and SPTFG goes high, thereby detecting the lamp failure.

5.3.2.8 Emergency Unload System

The Emergency Unload system, shown on Schematic No. 108130, sheet 3, consists of Emergency Unload Relay K1 (zone C3), a Relay Driver (zone C5), and an Emergency Unload Charging Network (zone B3). The Emergency Unload Enable signal (LEUEG) going low at J202 pin 32 turns on Q19 (zone C4), energizing relay coil K1. The relay contacts are connected so that when the relay is energized, the Positioner Power Amplifier (zone G5) is connected to the positioner coil. When the relay is de-energized, the positioner coil is connected to the unload capacitor via contacts 8/9 on Emergency Unload Relay K1 (zone D3). Normally, K1 is energized and the positioner coil is connected in the Servo Loop to the output of Positioner Power Amplifier (zone 3-5G) via pins 9/10 of K1. The Power Amplifier provides a current to the positioner coil that is proportional to the applied input voltage to U14.

LEUEG from pin 32 on J202 activates Q35 which turns on Q36, triggering SCR5 which puts a direct short across the positioner coil via contacts 16/15 of K1, into pin 5 and out of pin 2 of J205, and then back through SCR5. This halts the positioner immediately regardless of what mode it is in.

A few milliseconds after SCR5 is triggered, the current in Q19 decreases (zone 3-4G) and deactivates K1, which releases the short across the positioner coil at the same time connecting the emergency unload driver across the positioner coil causing the positioner to retract. The amount of current applied to the positioner coil is sensed at pin 4 of J214 and used by the emergency unload driver to limit the maximum unload velocity.

5.3.3 AC MOTOR CONTROL CIRCUITS

Ac Motor Speed Control circuits, shown on Schematic No. 108130, sheet 4 (zone H17), convert logic control signals Increase Motor Speed (NLIMS1), Brake Cycle Enable (NLBCEG), and Drive Motor Enable (NLDMEG) at J202 pins 21, 23, and 20, respectively, to the appropriate control signal at TP2 which fires the triac control circuit on the Ac Motor Control PCBA. This control signal and + 5v is connected via J213 (zone H14) to the Motor Control PCBA.

The 25v ac (peak) 60 Hz sine wave (zone E19) is converted into a 60 Hz square wave digital signal by comparator U6 pin 4.

Referring to the 25v (peak) voltage at zone D19, the voltage is phase advanced by the network formed by C60, R207, and R208, then converted into a 60 Hz square wave digital signal at U6 pin 9.

The digital signal outputs of comparators U6 pin 4 and U6 pin 9 are fed into an Inverse Exclusive OR circuit formed by U9 pins 4 and 12 and U10 pins 8 and 11. The output signal at pin 11 of U10 is a 120 Hz digital signal which is used as the switching signal for transistor switch Q21 (zone D16).

A circuit consisting of R201, R203, R204, C63, and transistor switch U21 generates a sawtooth waveform at 120 Hz. When the signal at U9 pin 9 is high, the transistor in the output state is cut off and capacitor C63 charges through R201, R203, and R204 to generate a ramp output at TP6. Conversely, when the signal at U9 pin 9 goes low, the transistor in the output stage is turned on and discharges capacitor C63 through R204. Since the value of R204 is much smaller than the sum of R201 and R203, the discharge time constant is much smaller than the charge time constant. Thus, the 120 Hz sawtooth waveform is generated and can be monitored at TP6. Potentiometer R201 (zone E16) is used to adjust the peak-to-peak amplitude of the sawtooth waveform which is fed to pin 1 of comparator U1 (zone E15) along with the output of operational amplifier U8 (zone G18).

The network associated with the operational amplifier U8 (zone G18) is an integrator circuit. When NLIMS1 is high, the output at TP5 is a ramp function whose time constant is dependent upon the value of R183, R185, R186. Diode CR30 and VR13 limit the maximum positive voltage to approximately 6v. Diode CR31 and VR13 limit the lower voltage excursion to approximately – 1.4v. Thus, when NLIMS1 is low, the steady state value of the output voltage at TP5 is approximately – 1.4v.

The dc voltage at TP5, which is proportional to the NLIMS1 pulses, and the reference 120 Hz sawtooth waveform from Q21 (zone D16) are compared in comparator U1 (zone E15). Thus, the signal at TP2 is either high or low, depending on the error in voltage between these two signals.

The operation of the Ac Motor Speed Control circuit during startup, constant speed control and brake cycle can be summarized briefly as follows. During startup, NLIMS1 is low, NLBCEG is high, and NLDMEG is high at J202 (zone C19). The output of the integrator at TP5 is approximately – 1.4v which, when compared with the reference 120 Hz sawtooth waveform, makes TP2 low. The low output of U1 at TP2 triggers the triac on the Motor Control PCBA every cycle, with practically full cycle power to the motor, allowing the motor to come up to the speed.

When the motor comes up to the correct speed, depending on the error in speed, NLIMS1 is either high or low, and the voltage at TP5 is such that, when compared with the reference sawtooth waveform at TP6, will generate a correction pulse at TP2. This correction pulse triggers the triac on the Motor Control PCBA at a specific part of the ac waveform so that power is on for only part of the cycle. In other words, firing the triac at a specific time in one cycle of an ac waveform achieves the phase angle control of the ac waveform, thereby controlling the power to the motor.

During a stop sequence, NLDMEG is high. When NLBCEG is also high (i.e., brake cycle is not enabled), the output at U10 pin 6 (zone H19) is low and the signal at TP2 is high all the time, and the triac is turned off. Hence, the power to the motor is cut off and the motor speed coasts down. When a brake cycle is enabled, NLBCEG is low, the signal at U10 pin 6 is high. Also, the signal at U6 pin 9 (zone D18) is high all the time; hence, signals at U6 pin 4 and U10 pin 8 (zone D17) are 60 Hz square wave digital output. Consequently, the frequency of the reference sawtooth waveform at TP6 is 60 Hz. Since NLIMS1 is high, the voltage at TP5 and U1 pin 2 is approximately 0.7v. Thus the output at TP2 is a 60 Hz pulse train. Since the frequency of the trigger pulses at TP2 is 60 Hz, as opposed to 120 Hz, the triac fires during only one-half of each cycle. The width of the pulse at TP2 controls the firing angle on the ac waveform, therefore, braking power is applied during each half cycle.

5.3.4 CARTRIDGE LOCK SOLENOID DRIVER

The Cartridge Lock Solenoid Driver circuit is shown on Schematic No. 108130, sheet 4 (zone C4). This circuit consists of a transistor switch connected in series with lock solenoids across + 5v and – 25v. J207 (zone B1) connects the coil of the lock solenoids to the Servo PCBA circuitry.

The Lock Cartridge Mechanism signal (LLCMG) low at J202 pin 33 causes Q34 and Q33 to turn on. This action applies approximately 24v across the solenoid coil which energizes the solenoids, pulling the plungers into the coil. When LLCMG is high, Q34 and Q33 are turned off and the solenoid coil is de-energized, releasing the plungers.

5.3.5 POWER CLEAR CONTROL CIRCUIT

The Power Clear Control circuit is shown on Schematic No. 108130, sheet 4 (zone E11). This circuit detects fault conditions in the ± 5v, ± 12v, + 25v, and – 25v dc supplies and provides the Power Clear Signal (SPCSA) to the Logic PCBA via J202 pin 31 (zone E7). J202 pin 30 (zone F13) connects the Plus 5 Volts Reference signal (LP5VA) to the Power Clear Circuit.

Figure 5-4 illustrates the waveforms associated with fault detection on the + 5v line. The signals at various nodes in the circuit have been drawn on the functional timing diagram for explanation purposes and should be referred to in conjunction with the schematic.

LP5VA high (plot 1) charges capacitor C70 (zone E8) through R231. Zener diode VR19 clamps and maintains the base of Q30 to + 2.7v nominal (plot 2). Capacitor C68 (zone E8) is charged to approximately + 2.1v nominal through diode CR36 and resistor network R228 and R244. The charging time constant of C68, R228 and R244 is much longer than that of C70 and R231. Consequently, the base of Q29 comes to the + 2.7v level with a slow rise time (plot 3). When the base of Q29 is + 2.7v nominal, transistor Q29 turns on and lowers the voltage on the base of Q25 to less than + 5v, turning on Q25. The collector of Q25 will be at approximately + 4.8v nominal. Resistor R233 provides positive feedback to the base of Q29, hence, a clean, fast edge of the signal is obtained at the point of transition (plot 4) and at J202 pin 31 (SPCSA) (plot 5). The amplitude of SPCSA is approximately 3.3v when high since there is a 150-ohm resistor inserted on the Logic PCBA between the SPCSA signal line and ground.

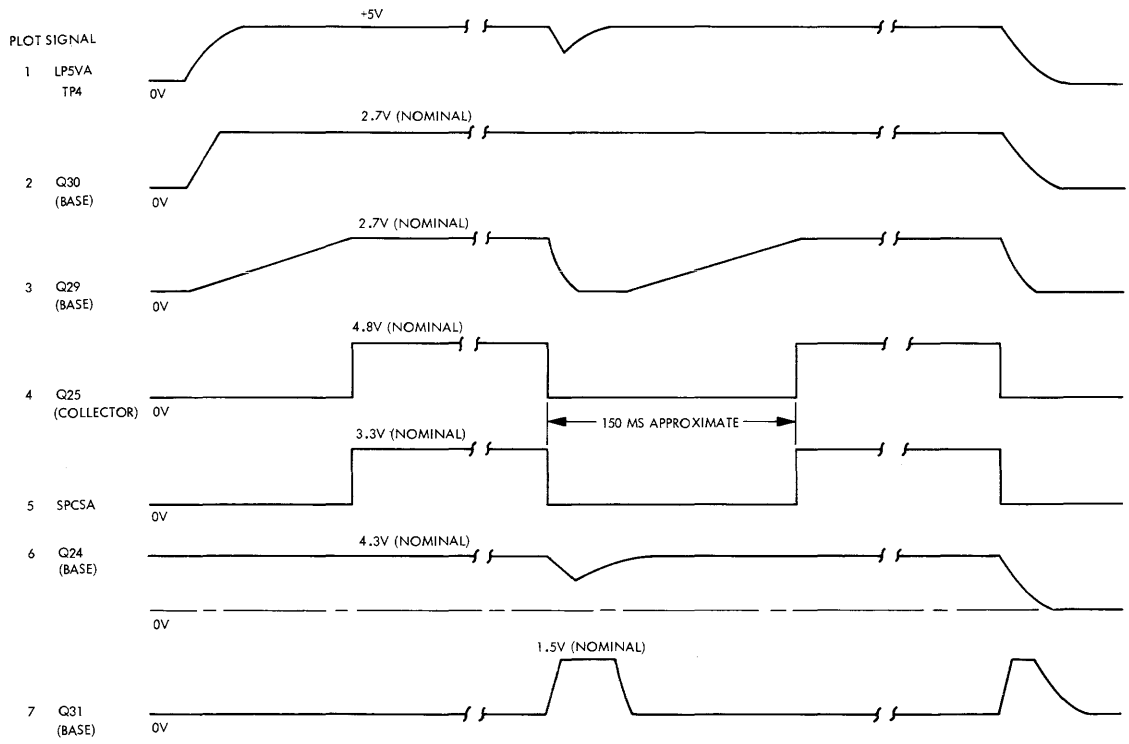

Figure 5-4. Fault Detection Waveforms

In the case where the + 5v sags momentarily, and correspondingly the voltage at the base of Q29 goes below 2.7v so that Q29 is turned off, the following actions occur. Q25 turns off instantaneously and R233 provides positive feedback to achieve the sharp transition at the collector of Q25. Since Q25 is off, the collector of Q25 is at ground potential and capacitor C66 is charged from the charge of C65. The difference in potential at the base of Q24 turns on Q24 which turns on Q31. Capacitor C68 discharges through R237. The discharge and charge time constants associated with C65 and C66 are such that Q24 is turned on for a longer time than the time required to discharge C68 through R237. Plots 6 and 7 of Figure 5-4 describe typical waveforms of Q24 base and Q31 base voltages, respectively. SPCSA will also be low since the collector of Q25 is at ground potential.

Once the base of Q24 recovers to the same potential as its emitter (4.3v), Q31 is turned off and C68 charges through the network formed by R228 and R244 until the base of Q29 is at + 2.7v. This turns on Q29 and Q25 and the collector of Q25 goes to + 4.8v and SPCSA goes high (plots 3, 4, 5). The approximate time for SPCSA to go high after it has been in a low state is 150 msec.

If the − 5v goes below approximately − 2.7v nominal, Q28 turns off and the cathode of CR36 goes to ground potential. This causes Q9 to turn off and the sequence of events is identical to the + 5v dropoff previously described.

The following action occurs when LP5VA goes low permanently from its high state. The collector Q25 goes to ground potential and SPCSA goes low. The signals at the base of Q30, Q29, Q24, and Q31 are shown in plots 2, 3, 6, and 7, respectively.

Similarly, if the – 25v goes below approximately – 17v nominal, Q28 turns on and the cathode of CR36 goes to ground potential. This causes Q29 to turn off and the sequence of events that occurs is identical to the + 5v drop-off previously described. When the + 25v is more negative than – 20v, Q28 turns off and the cathode of CR36 is at approximately 3.3v which turns on Q29.

Similarly, if the + 25v is maintained at its nominal potential, Q26 is on and the base of Q27 is at approximately 0v which turns off Q27. The cathode of CR36 is at + 3.3v, and a normal charging sequence of C68 occurs until Q29 turns on. When the + 25v goes to + 20v, Q26 turns off and Q27 turns on. CR36 cathode goes to ground potential and the sequence of events that occurs is identical to the + 5v drop-off previously described.

If the – 12v goes below approximately – 10v nominal, Q28 turns on and the cathode of CR36 goes to ground potential. This causes Q29 to turn off and the sequence of events is identical to the + 5v drop-off previously described. When the – 12v is more negative than – 10v or more, Q28 turns off and the cathode of CR36 is at approximately 3.3v which turns on Q29.

Similarly, if the + 12v is maintained at its nominal potential, Q26 is on and the base of Q27 is at approximately 0v which turns off Q27. The cathode of CR36 is at + 3.3v, and a normal charging sequence of C68 occurs until Q29 turns on. When the + 12v goes to + 10v, Q26 turns off and Q27 turns on. CR36 cathode goes to ground potential and the sequence of events that occurs is identical to the + 5v drop-off previously described.

It should be noted that resistors R233 and R236 provide hysteresis in the circuit so that the voltage (– 5v, + 5v, + 12v, + 25v, – 12v, or – 25v) at which SPCSA goes high is always slightly higher than when it goes low.

5.4 READ/WRITE PCBA, HEAD SELECTION MATRIX AND PREAMPLIFIER PCBA

The following paragraphs describe the Read/Write PCBA installed in D3000 Series Disk Drives. Refer to Schematic No. 108140 with Assembly 108141, and Schematic 108145 with Assembly 108146.

The Read/Write PCBA is approximately 247.7 mm (9.75 inches) long by 165.1 mm (6.5 inches) wide. Figure 5-5 illustrates the placement of each connector, test point, and adjustable component on the PCBA. J305 is connected to the Logic PCBA via a mating plug and 3M flat cable. J304 is a molex connector which supplies power to the Read/Write PCBA via a mating plug and standard cabling. J306 interfaces with the Temperature Compensation PCBA. J310 connects the read signals and write driver outputs to the Matrix PCBA. Head and Platter Select signals are connected to the Matrix PCBA via J311.

The Read/Write PCBA description is divided into the following elements.

(1) Head Selection Matrix and Preamplifier
(2) Write and Erase Driver
(3) Read Switch
(4) Read Preamplifier
(5) Filter
(6) Differentiator
(7) Squaring Amplifier and Frequency Doubler

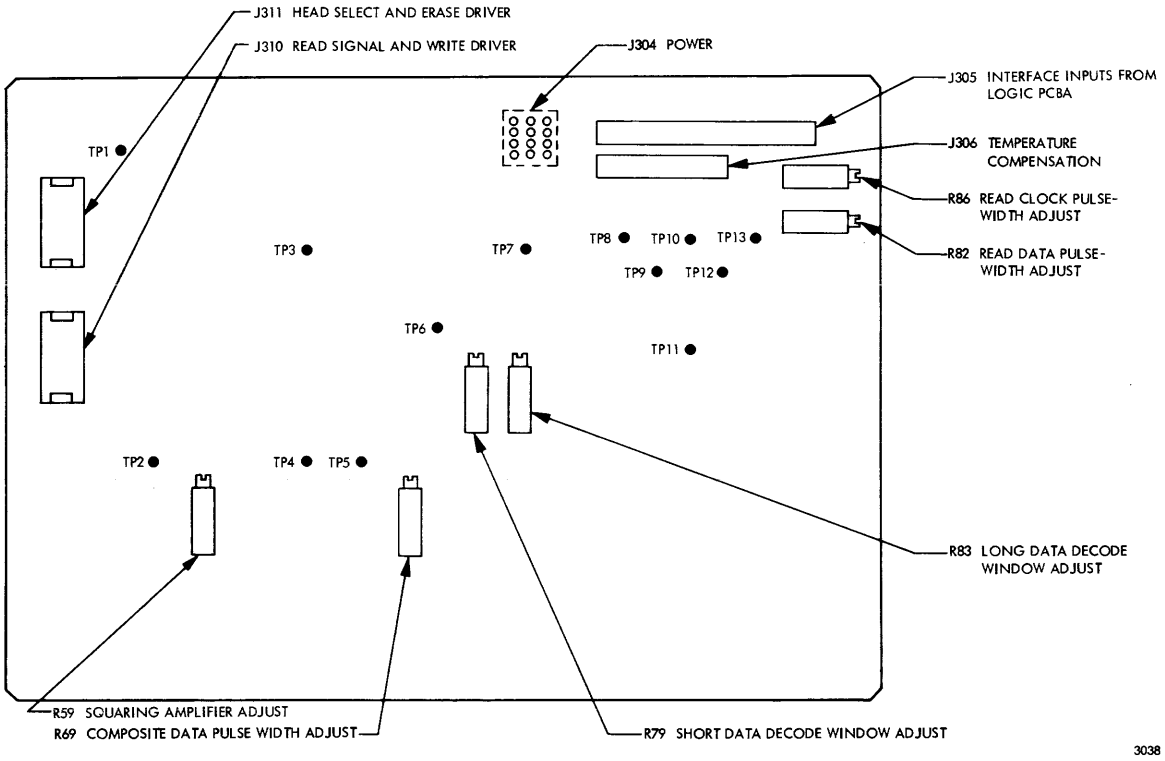

Figure 5-5. Read/Write PCBA Test Point and Connector Placement

(8) Data Decoder

(9) Emergency Condition Detection

A block diagram of the Read/Write electronics is shown in Figure 4-4 and should be referred to in conjunction with Schematic No. 108140 and the electrical description in the following paragraphs.

5.4.1 HEAD SELECTION MATRIX AND PREAMPLIFIER PCBA

Mounted at a 90-degree angle to the Read/Write PCBA is the Head Selection Matrix and Preamplifier PCBA which is 256.7 mm (10.5 inches) by 101.6 mm (4.0 inches). Figure 5-6 illustrates the placement of each connector on the PCBA. There are no test points or adjustable components on this PCBA.

Head selection is accomplished using a conventional diode matrix in conjunction with center-tapped heads. Each head is comprised of a balanced Read/Write (R/W) center-tapped winding, and a separate erase winding, which has one end connected to the R/W center tap.

Referring to Schematic No. 108145, zone E7 through E3, eight heads are shown connected to J600 through J607. Three diodes are associated with each head; two of the diodes (CR28 and CR30 for the J600 head) are connected to the balanced R/W bus and the third diode (CR31) is connected to the erase bus.

The eight head center taps are pulled to – 12v by resistors R41, R43, R45, R47, R49, R51, R53, and R55 when the associated head is not selected. When selected, the appropriate head center tap is pulled positive by the corresponding head select switches (Q6 through Q13).

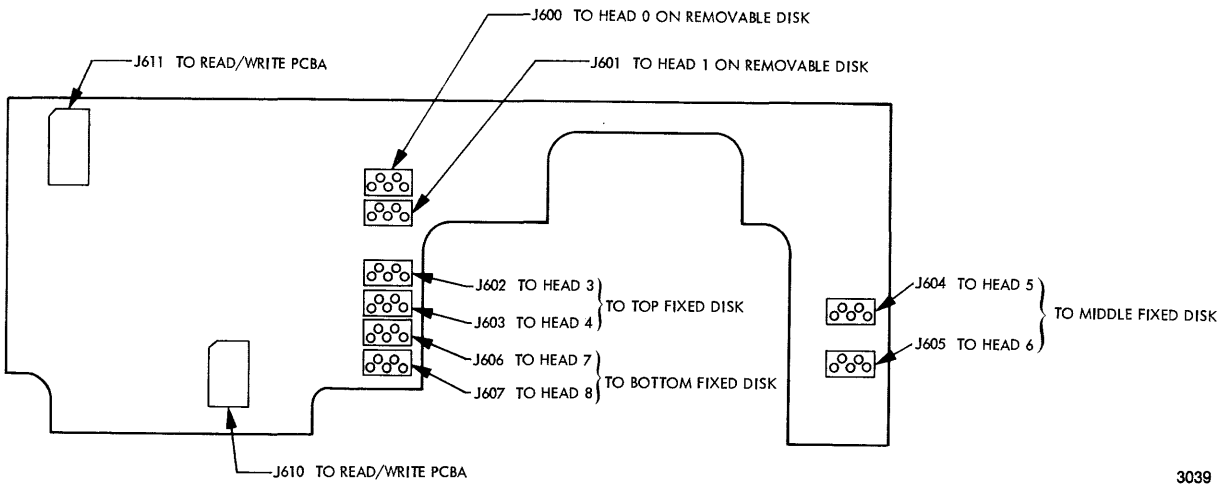

Figure 5-6. Head Selection Matrix PCBA

During a write operation when LDMAG (J305 pin 21, zone E12) is low, the output of inverter U12-4 will be high. This is fed to AND gate U10 whose output will become low thereby causing Q9 to turn on. This causes Q10 to also turn on, which puts R30 in parallel with R31 and R32. This lowers the resistive load on Q10, resulting in an increased current when the heads are over the outer tracks (0 through 255). Conversely, when LDMAG is high, Q10 is not activated, keeping R30 out of the load circuit to ensure a low writing current through the heads when over the inner tracks (256 through 405). The appropriate selection is performed as follows. The Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are inverted by U12-5 and U12-1, respectively. The Demand Address Most Significant Bit (256) signal (LDAMG) is fed directly to U12-3 and ANDed with NLWMXG by U10. The output of U10 is fed to Q9 (zone C8) which turns on Q10. This system ensures that write current is appropriately reduced when writing on inner tracks where the flying height of the head is reduced.

During a Read operation, the head select switches are fed via Q1 through Q4. The NOT (Write Mode or Erase Enable) signal from U8-10 is used to drive the open-collector inverters at U8-6 and U8-4, which are fed into the Read/Write Matrix Selection PCBA as Write Mode and Read Switch signals.

5.4.2 WRITE AND ERASE DRIVERS

During a Write operation, the Write Mode (NLWMXG) signal is inverted and, when true, enables J-K flip-flop U5 (zone E9). U5 is always enabled in the reset state. Write Double Frequency (NLWDFT) pulses are received and fed to the clock input of U5. These clock pulses toggle the flip-flop for every pulse received as required by the double-frequency code used.

The Q and $\overline{Q}$ outputs of U5 are fed to two identical predrivers, Q5 and Q6. The outputs of Q5 and Q6 drive write drivers Q7 and Q8 whose emitters are returned to approximately – 11v. When Q7 or Q8 conduct, write current flows in one half of the selected head. This current is defined by resistor R31 and R32 (as appropriate). This yields typical write currents of 68 ma peak for tracks 0 through 255 and 58 ma for tracks 256 through 405. The base drive circuits of all four transistors have anti-saturation diodes CR1 and CR2 incorporated. Diodes CR3 and CR4 are used to isolate the head bus from the write circuitry during a Read operation, thus reducing noise injection.

The erase driver is separately enabled by the Erase Current Enable (NLECEG) signal since the erase current can be left on for a longer time than the write current. When NLECEG is low, Q11 (zone C6) is turned on via inverters U12-2 and U12-12. This causes the base of Q12 to be switched on allowing R36 to control the erase current.

The return path for both write and erase drivers is via the emitter base junction of Q15 through Q16, and then to – 12v via the S12SS line which is returned to – 12v through the emergency unload relay. Q16 is only enabled via Q13 and Q14 when the Power Clear Signal (SPCSA) is at a high (positive) level. Q15 is used as a write current detector and is detailed in Paragraph 5.4.9.

5.4.3 READ SWITCH (SCHEMATIC 108145, SHEET 2)

The diode switch CR53, CR55 (zone E3), CR54 and CR56 (zone D3) is used to isolate the head bus from the read amplifier during Write operations to prevent overload of the read preamplifier.

During a Write operation, Q5 (zone G2) is turned on via open-collector driver U8-4. This pulls the junction of R33 and R34 (zone E3) to + 12v cutting off all four diodes. This follows since the head bus voltage cannot exceed + 12v and the anode voltage of CR55 and CR56 cannot exceed + 0.7v due to CR57 and CR58.

During a Read operation, Q5 is turned off and the junction of R33 and R34 is returned to approximately – 6v via R35. Approximately 1 ma flows through R33 (and R34) and approximately 0.5 ma is supplied by R29 (and R28). Thus, a current of 0.5 ma flows through each of diodes CR53, CR55, CR54, and CR56, enabling the read switch.

5.4.4 READ PREAMPLIFIER (SCHEMATIC 108145, SHEET 2)

The balanced read signal from the head bus is terminated by R37 and R38 (zone D,E,2) and fed to the type 592 differential video amplifier U1 . When used in this configuration, the amplifier has a wide bandwidth and a balanced output gain of approximately 150.

5.4.5 FILTER (SCHEMATIC 108140, SHEET 3)

The balanced preamplifier output of video amplifier U1 (Paragraph 5.4.4) is fed to a linear phase filter (zone D18,16). This filter has sharp cut-off characteristics combined with a group delay characteristic which is constant over the signal frequency band. The insertion loss of this filter is 0.5.

5.4.6 DIFFERENTIATOR (SCHEMATIC 108140, SHEET 3)

The differentiator is comprised of U1 (zone E16), a NE592 differential video amplifier with the differentiation capacitor C21 acting as the gain determining element. Resistor R48 is a high frequency gain limiting resistor. R46 and R47 terminate the linear phase filter and provide the input dc bias path for U1.

5.4.7 SQUARING AMPLIFIER AND FREQUENCY DOUBLER (SCHEMATIC 108140, SHEET 3)

The balanced output from U1 is fed through coupling capacitors C22 and C23 to U2 (zone E15) to the Squaring Amplifier stage. R49 and R50 provide a nominal load for U1. Q18 provides a means of reducing the electronic gain by one-half for margin checking at TP5 and TP4. CR8 through CR11 are input limiters; C24 and C25 provide a high frequency rolloff for the circuit. R60, R61, R64, and R65 are biasing resistors. R56, R57, R62, R63, C26, C27, C28, and C29 provide a balanced differential feedback for the two stages, thus stabilizing the operating point of the circuit. The read pulse balance is adjusted by potentiometer R59.

The 8T20B crossover detector U7 provides an output pulse for each zero-crossing of the square wave signal from U2, doubling the frequency of the signal from the Squaring Amplifier. Width of the output pulse is determined by potentiometers R69, R70, and C33. These composite data pulses contain both clock and data and can be monitored at TP9.

5.4.8 DATA DECODER CIRCUITRY (SCHEMATIC 108140, SHEET 3)

The Data Decoder circuitry acts upon the pulse former output to generate separated data and clock signals. Paragraph 4.6.3.6 contains a functional description of this circuit.

The composite data signal waveform consists of clock pulses which occur every 640 nsec (1500 rpm and 2200 bpi) interspersed with a pulse for every one bit (data bit) recovered.

The composite data signal from U7 pin 11 is gated through U15-6 (zone G6) and its leading edge is used to clock the appropriate one-shot to set the ones window. If the preceding clock period had a one interspersed, then the short one-shot (U9-12, zone G8) is used to form the ones window via U16-6 (zone G6). If the preceding clock period did not contain a one, then the long one-shot (U9-4, zone D8) is used to form the ones window via U16-6. R79 and R83 are used to set the period for the short and long one-shots, respectively.

If a data pulse occurs during the time that the ones window is high, it will be gated through U16-12. This pulse sets U14 (zone E10) which results in the short one-shot determining the next one-shot period.

The output of U16-12 (zone D6) and U15-6 (zone G6) are fed back to the inputs of U16-3 and U16-11, respectively, and act as pulse stretchers. The outputs are also applied to U17-1 and U17-9 where the decoding pulse is lengthened prior to transmission down the interface lines. The output of U17-13 (zone D5) is adjusted by R86. The output of U17-5 (zone G5) is adjusted by R82.

5.4.9 EMERGENCY CONDITION DETECTION

Two conditions are detected by the Emergency Condition Detector circuitry and cause the Write Emergency Condition (RWECG) signal to go high. The NRWECG signal is fed to the Logic PCBA via J305 pin 30 (Schematic 108140, sheet 3, zone F2) where it is used to initiate an emergency unload sequence. The emergency unload sequence causes the unit to go Not Ready, thereby turning off write current in less than 1 μsec. The emergency unload sequence also causes the emergency unload relay to operate, thereby interrupting the S12SS supply. Interruption of this supply precludes any write current flowing in the heads.

One emergency condition detected is the condition when more than one head is selected while the drive is in a Write mode of operation. When a head is selected in the Write condition (e.g., the head connected to J600), the appropriate center tap is pulled to approximately + 12v. This voltage is transmitted via CR59 (Schematic 108145, zone C7) to amplifier Q17 (Schematic 108140). A precision current drain for this circuit is established via R43 to − 12v.

The non-inverting input of Q17 is set at a nominal voltage of − 4.5v such that when one head is selected, the inverting input is more negative than + 0.2v and the output of Q17 is high. When two heads are selected (e.g., the head connected to J600 and J601), additional current is fed to R43 via CR60 to the input of Q17 raising this point to + 0.2v causing the output of Q17 to switch to a negative state. This output is fed to one input of the low active OR gate U10-13 (zone A4) causing RWECG to go high at J305 pin 30 (zone G2). CR7 prevents the input to Q17 from going more negative than − 0.7v.

The second emergency condition detected by this circuitry is when write current is on during a Read operation. It is important to note that during a Read operation, no write current or erase current should flow.

Write and Erase current must flow through R39 (zone B7) and the emitter base diode of Q15. If a total current in excess of approximately 0.7 ma flows, then the voltage across R39 (1K ohm) will exceed 0.7v causing Q15 to turn on. Q15 conducting causes the input to inverter U6-13 (zone B6) to go low which enables one input of NAND gate U11-9 (zone A5).

Recall that during a Read Mode, the Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are high, thus the output of U10-8 (zone A6) is low.

In the Read Mode, the output of inverter U8-8 (zone B5) is high, enabling the remaining input of NAND gate U11-8. Thus, the output of OR gate U10-11 (zone A4) goes high and the RWECG waveform goes high at J305 pin 30 (zone G2). Resistor R41 and capacitor C6 (zone B5) are used to provide masking delays to avoid false indications during Read/Write mode switching.

During a Write operation, transistor Q15 is on, but one or both of the NLECEG and NLWMXG waveforms are low. Therefore, the output of U10-8 is high, inhibiting U11-8 and preventing RWECG from going high.

5.5 LOGIC PCBA

The following paragraphs describe the Logic PCBA installed in the D3000 Series Disk Drive. Refer to Schematic No. 108165 and Assembly No. 108166.

The Logic PCBA is approximately 393.7 mm (15.5 inches) long by 273.1 mm (10.75 inches) high. Figure 5-7 illustrates the placement of each connector, test point, and adjustable component on this PCBA. J104 and J105 connect to the Servo PCBA via 3M flat cable. J108, J109, J110, J111, and J112 are Molex connectors which also connect to the controls, indicators, and sensors. J103 connects to the Read/Write PCBA via 3M flat cable. J101 provides for connection between the D3000 and a controller or another drive. J102 provides connection to the PCC PD I/O terminator PCBA or another drive.

For ease of understanding, the description of this PCBA is addressed on a sheet-by-sheet basis beginning with sheet 3. Note that signals are cross referenced between sheets and within a sheet by numbers appearing under the associated logic term mnemonic. For example 12-7E, the 12 refers to the schematic sheet number; the 7E refers to the zone on that page.

5.5.1 SHEETS 3, 4, 5 AND 6 (SCHEMATIC 108165)

Sheet 4 of the Logic PCBA schematic contains the Start/Stop Control Logic portion of the drive function control logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The output of crystal oscillator Y1 (zone 6-7B) is fed to the clock countdown circuitry and can be monitored at TP14. The clock countdown circuitry consists of cascaded 4-bit binary counters operating in a binary countdown mode. The first counter of the countdown chain is a synchronous counter, the remainder are ripple counters. The clock signals derived from the clock countdown chain are square waves which are fed to various parts of the logic to provide the primary timing.

One of the clock signals is used in the spindle speed control logic to determine the disk speed, and functions as the primary time reference for the spindle speed control. Another of the clock signals, LC09F (U305-11 zone 6-3C) is ANDed with the Sequence Timing Pulse F/F (U345 zone 3-3H) output pulse at AND gate U284-13 (zone 4-7F) to produce the gated clock to the Purge Cycle F/F (U344 zone 4-4G) and the Load Heads F/F (U344 zone 4-3G). The frequency and the period of each one of the clock signals is listed in Table 5-1 which

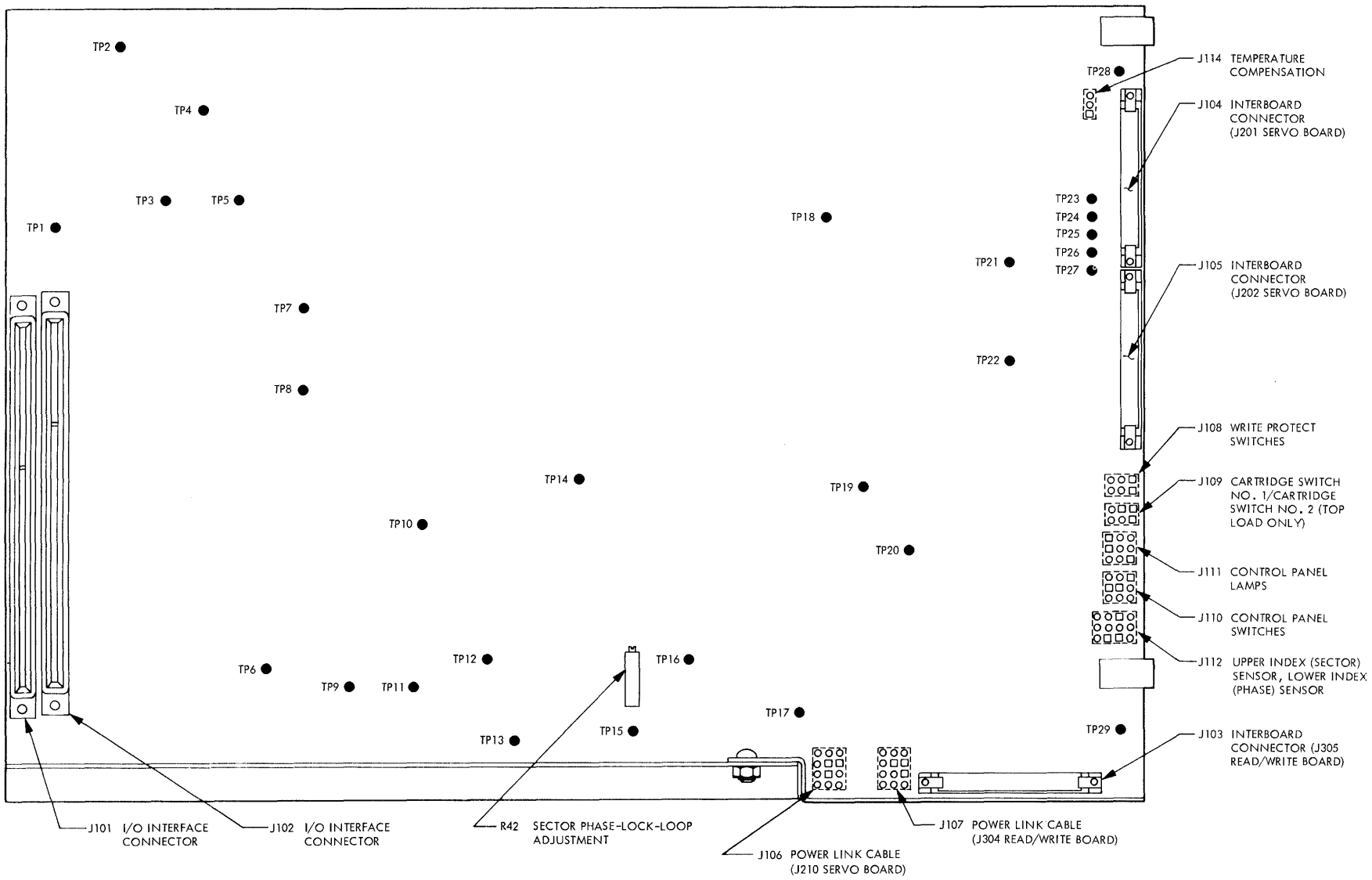

Figure 5-7. Logic PCBA Test Point and Connector Placement

Table 5-1
Clock Countdown

Clock No.	Frequency (in Hz)	Period
01	5000000.0	200 nsec
02	2500000.0	400 nsec
03	1250000.0	800 nsec
04	625000.0	1.6 μsec
05	312500.0	3.2 μsec
06	156250.0	6.4 μsec
07	78125.0	12.8 μsec
08	39062.5	25.6 μsec
09	19531.25	51.2 μsec
10	9765.625	102.4 μsec
11	4882.8125	204.8 μsec
12	2441.40625	409.6 μsec
13	1220.703125	819.2 μsec
14	610.3515625	1.6384 msec
15	305.17578125	3.2768 msec
16	152.5878906250	6.5536 msec
17	76.2939453125	13.1072 msec
18	38.14697265625	26.2144 msec
19	19.073486328125	52.4288 msec
20	9.5367431640625	104.8576 msec

shows that each successive clock signal is one-half the frequency and twice the period of the previous signal in the clock countdown.

NOTE

Generated clock signals are listed in Table 5-1 to aid in troubleshooting; however, all of these signals are not used in the D3000.

The major states of the Start/Stop Control Logic are defined by the Run Flip-Flop U364 (zone 4-6H), End Of Run Flip-Flop U364 (zone 4-5H), Purge Cycle Flip-Flop U344 (zone 4-4H), Load Heads Flip-Flop U344 (zone 4-3H), Sequence Control Flip-Flop U384 (zone 4-5E), Brake Cycle Enable Flip-Flop U384 (zone 4-4E), Emergency Unload Flip-Flop U345 (zone 3-2E), and Disk Rotation Detector Counter U283 (zone 3-2D).

A delay counter is mechanized by taking the last of the Clock Countdown, LC21F, and applying it to the input of binary counter U325 (zone 3-7G). The delay counter, in conjunction with Sequence Timing Pulse F/F U345 (zone 3-3G) and the appropriate combinational logic, generate timing sequence pulses at specific time intervals according to the states of the logic. The counter is controlled by resetting it with a pulse via U267-9 (zone 6-2C).

NOTE

External commands, directly or in conjunction with the combination of external commands and the present states, may affect the next state of the Start/Stop Control Logic. Refer to the block diagram of the digital sequential machine (Figure 4-9) used to mechanize the Start/Stop Control Logic.

The logic is initialized during power ON and power OFF events by the Power Clear Signal (SPCSA) from the Servo PCBA at J105 pin 31 (zone 3-8E). SPCSA is an analog signal which is converted into logic levels by U286-9 (zone 3-7E). It should be noted that when the output of U286 pin 9 is high, power to the machine is either off or below the minimum acceptable value as determined by the Power Clear circuit on the Servo PCBA.

SPCSA clears Disk Rotation Detector Counter U283-1 (zone 3-2D), presets Emergency Unload F/F U345-2 (zone 3-2F), clears End of Run F/F U364-8 (zone 4-5G), and Sequence Timing Pulse F/F U345-8 (zone 3-3H). SPCSA assures that the logic is properly initialized during power turnon and that the logic assumes the correct states in the event of power removal.

Commands which can cause the Start/Stop Control to execute either a start or a stop sequence are obtained from the RUN/STOP control signal (CRSSS) connected to J110, pins 2 and 3 (zone 4-8B). A cross-coupled inverter latch U447 is used to clean up the input signal and eliminate the problem of switch contact bounce. The output of this latch is tied with the inverted Start/Stop Disk Drive (ISSDR) of U85 (zone 3-7B) and then fed directly to U328 (zone 4-6B). The output of U328, pin 11, is the input to Start/Stop Pulse Register U347 (zone 4-6B). A level change occurring either from an assertion of the Start/Stop Disk Drive line or from actuation of the RUN/STOP control is edge-detected by the Start/Stop Pulse Register. The Start/Stop Pulse Register is a shift-register type of edge detector whose purpose is to produce a pulse having a period of one clock time upon detection of the leading edge of a level change propagating through the register.

The one-clock period pulse output from U346 is the Run Switch Pulse (LRPXG) used for clocking Run F/F U364 (zone 4-6H). In addition, the Start/Stop Pulse Register generates the Start Drive Motor (NLSDMG) signal if, and only if, the Run F/F is one-set as a result of the level change propagating through the Start/Stop Pulse Register. This will be the case when the Run F/F has been properly enabled and is one set to commence a start sequence. The NLSDMG pulse initializes flip-flops in the Spindle Speed Control logic shown on sheet 7 (zone 3G) of the schematic.

The Delay Counter Decode logic (zone 3-7G) is enabled by the outputs of the Sequence Control Logic as well as the Sequence Control F/F. Delay Counter Decode decodes specific values of delay by ANDing various bits from the Delay Counter according to the states presented by the Sequence Control Logic and the Sequence Control F/F.

The Sequence Timing Pulse F/F U345 (zone 3-3H) is used to generate a pulse with a period of one clock interval, when a high level is applied to the J input from Delay Counter Decode Logic. The sequence timing pulse is used to define the timing of events during the start sequence and stop sequence. It also tests the states of certain signals during the start sequence for the purpose of determining if an emergency condition exists.

The timing of two of the flip-flops is accomplished by using the sequence timing pulse to gate the clock to the Load Heads F/F and the Purge Cycle F/F. This is done to ensure clocking these flip-flops only at the end of specific delay intervals.

The Disk Rotation Detector Counter is used to detect disk rotation for purposes of interlocking, and to determine the duration of the brake cycle. Additionally, the Disk Rotation Detector Counter provides a time delay at the end of the power clear condition.

The Sequence Control Logic (zone 4-3G) is employed to decode the states of the Purge Cycle F/F and the Load Heads F/F. This provides signals for steering the start sequence and for initializing the position monitor circuit in the Position Control Logic. The signal

outputs from the Sequence Control Logic are also used to enable the tests in the Emergency Unload Logic (zone 3-5C).

The Run F/F (zone 4-6H) will be zero-set by any Run Switch Pulse (LRPXG) if it is already one-set. If the Run F/F is previously zero-set, then LRPXG will one-set the flip-flop only if proper interlocking has occurred. Detection that the disk cartridge is correctly inserted interlocks the Run F/F. Gate U346-3 (zone 4-6G) ANDs the Cartridge Correctly Inserted (LCCIG) signal with the Clear Or Unload (NLCOUG) signal to clear the Run F/F if either or both of these signals are low. LCCIG is developed from the states of the cartridge inserted switch. NLCOUG is the OR condition of the Power Clear Signal and the output of the Emergency Unload Logic.

Determination of correct cartridge insertion is accomplished by one switch in top load models and one in front load models. These switches connect to J109 (zone 4-8G) and operate the Cartridge Inserted Latches. The output of the Cartridge Inserted Latches generates the LCCIG signal. The latches are cross-coupled inverters in the same configuration as those used at the input to the Start/Stop Pulse Register. In front load models, one of the latches is held permanently in the correct state by a jumper at P109.

The Run condition is defined as any time the disk is rotating and a stop sequence is not in progress, i.e., Run F/F is one-set. The Run F/F cannot be one-set by a Run Switch Pulse signal unless the J input to the flip-flop is at a logic one level. The signal that enables the Run F/F J input is NLLCMG, which is the result of combinational logic containing the remaining interlocking signals. These interlocking signals are: Heads Retracted (SHRXG) which prevents entering a run condition unless the heads are retracted; Not Disk Rotating (NLDRXG) from the Disk Rotation Detector Counter, which prevents entering a run condition unless the disk is stationary; Not Brake Cycle (NLBCFF) from the Brake Cycle F/F, which prevents entering a run condition if a brake cycle is in progress; and finally, the logic condition resulting from the combination of the state of the Sequence Control F/F (LSCFF) and the Run F/F (LRFFF) which are combined in U385 (zone 4-4D). NLLCMG is used in the interlocking control portion of the logic. The use of this arrangement prevents reentry into a run condition (Run F/F one-set) unless a correct stop sequence has been executed.

As previously mentioned, there are two basic sequences executed by the Run/Stop Control Logic; the start sequence and the stop sequence. A start sequence begins when the Run F/F is one-set and progresses through the one-setting of Purge Cycle F/F U344 (zone 4-4G), the one-setting of Load Heads F/F U344 (zone 4-3G), and finally, the one-setting of Sequence Control F/F U384 (zone 4-5E). One-setting the Run F/F defines the run condition. The Purge Cycle F/F then defines that portion of the start sequence when the disk speed is increased to 10 percent above the nominal speed. This is done to increase the air flow across the disk(s) prior to loading the heads. The Load Heads F/F is used to define that state when the heads are loaded onto the disk(s). The Sequence Control F/F defines the state which indicates the successful completion of a start sequence, or the beginning of a stop sequence.

A stop sequence begins with zero-setting the Run F/F. This causes one-setting the End Of Run F/F which causes the Sequence Control F/F to be preset in the event that it has not yet been one-set. To complete the stop sequence, the Brake Cycle Enable F/F is one-set at the same time that the Sequence Control F/F is zero-set. The stop sequence ends with zero-setting the Brake Cycle Enable F/F. The End Of Run F/F is used to detect the high-to-low transition of the Run F/F when it is zero-set. The End Of Run F/F, therefore, acts as an edge detector which is used to force a preset condition to the Sequence Control F/F. This guarantees correct entry into the stop sequence. The Brake Cycle Enable F/F is then one-set to define that portion of time when braking current is supplied to the disk motor to stop the disk.

The Emergency Unload F/F U345 (zone 3-2F) defines the condition which causes the emergency unload relay to disconnect the positioner servo from the positioner coil and connect the positioner coil to the emergency unload network. This is done when executing an emergency unload, or for preventing the connection of the positioner coil to the servo electronics, prior to the time when the drive logic is capable of detecting certain positioner electronic faults.

The Emergency Unload Logic is comprised of three basic parts: U266 (zone 3-6D) which ANDs the Sequence Timing Pulse F/F with outputs from the Sequence Control Logic and the specific signals to be tested for emergency condition indications during a start sequence. The signals tested by U266 logic are NLPMXG, and LSOTF. The ANDing of these signals generates, respectively, Head Loading Error (NLHLEG) and Disk Starting Fault (NLDSFG).

Position Transducer Failure (SPTFG) from the Servo PCBA is ORed with Write Emergency Condition (RWECG) from the Read/Write PCBA at gate U327 (zone 3-7D) to produce NLEOFG, which is the Emergency Or Failure condition.

These signals plus Position Limit Error (NLPLEG), Disk Speed Error (NLDSEG), and Seek Time Error (NLSTEG) from other portions of the logic are combined in OR gate U306 (zone 3-5C) to produce Any Emergency (LAEXG). Assertion of LAEXG by one or more of the emergency situations detected by the Emergency Unload Logic results in clearing the Run F/F and aborting the run condition. This presets the Emergency Unload F/F U345-2 (zone 3-2E) causing emergency retraction of the heads.

Lamp drivers U406-5, U386-5 (zone 4-2C,B), and U406-3 (zone 3-2D) provide drive to the front panel indicator lamps for the SAFE, RUN, and READY lamps, respectively.

The Ready signal is combined with the Selected signal at U385 (zone 3-3C) to obtain the Selected And Ready condition for gating the line receivers and drivers for the I/O interface.

The decade counter consists of two independent logic sections of *divide by five* and *divide by two.* The counters U205, U305 and U285 are used to count down the 10 mHz clock to obtain clocks which are used in the Position Control Logic.

Sheet 5 shows four of the I/O interface lines that control drive functions which are routed directly to the Holding Register (U308 zone 5-6H) on the Logic PCBA. These lines are: Head Select (IHSXR), Platter Select (IPSXR), Track Offset Plus (ITOPR), and Track Offset Minus (ITOMR). Note that Selected And Ready (NLSARG) is brought to the holding register load-input. When NLSARG is low, the states of these I/O interface lines will be copied into the register. Thus, the state on the register will correspond to the state at the I/O interface line and will change accordingly for any changes on the I/O interface line.

When the drive is deselected, NLSARG will go high causing the holding register to trap the last value of the inputs from the I/O interface. The register will then hold that state until the next time the drive is selected. Note that Ready (NLRXXG) is used as the clear input to the Holding Register 308-14 (zone 5-6G). When high, NLRXXG causes the register to be cleared to the all-zeros condition on each of its outputs. This condition will occur at any time the machine is in the Not-Ready condition. In other words, the predetermined states of logic zero on each of the output lines from the Holding Register determine specific states for the Upper Head Select (NLUHSG), Upper Platter Select (NLUPSG), Track Offset Plus (NLTOPG), and Track Offset Minus (NLTOMG) lines on the Logic PCBA.

NLUHSG is routed directly to the Read/Write PCBA for head selection according to the state in the Holding Register. LUPSG and its complement, NLUPSG, are connected to various circuits on the Logic PCBA. These circuits are the Write Protect Logic for

determining which Protect switches will be sampled, and the Multiplexer Control Logic for determining which platter information will be multiplexed to the I/O interface output lines. In addition, NLUPSG is routed to the Read/Write PCBA for selecting a specific storage surface.

NAND gates U328 (zone 5-2G) combine the Track Offset signals from the Holding Register with NLODAG (via NOR gate U327-13 zone 6-7C) from the Position Control Logic. The results are that the Track Offset signals will not be asserted to the Read/Write PCBA and the Servo PCBA during the time that the positioner is busy. The outputs of these NAND gates are connected to the Servo PCBA and the Read/Write PCBA via pins 22 and 23 of J103 (zone 6-1G) and pins 26 and 25 of J104.

NOTE

These signals control change of gain in the read amplifier on the Read/Write PCBA when both signals are asserted. The signals are also fed to the Servo PCBA and are used to assume operation of the Track Offset circuitry.

The Write Double Frequency Data Retransmitter (U70 zone 5-6F) functions as a line receiver and a line driver. The Write Data Signal (IWDSR) from the I/O interface (J101 pin A-28, zone 5-8F) is received by U70 acting as a line receiver. IWDSR is the double frequency encoded write data from the I/O interface which must be transmitted to the Read/Write PCBA. Transmission of the write data signal is also accomplished by U70. Acting as a line driver, it drives the NLWDFT signal to the Read/Write PCBA through J103 pin 27 (zone 5-1G) where it is used by the Read/Write electronics.

The Unit Select Logic and the Busy Output Logic are shown on sheet 6 in zone 6-7G through 6-5G. The Unit Select Logic is the decoding arrangement and the Busy Output Logic is an encoding arrangement. Four separate Unit Select lines (IUS1R—IUS4R) are provided at the I/O interface and are presented to the circuit via J101 (zone 6-8G). This allows selection of one of four drives on the common I/O bus. Internally, it is necessary for the drive to provide a signal which indicates that it is being selected by the I/O interface.

Since there are four separate and distinct lines presented to the drive, they must be decoded. The Unit Select lines are brought through J101, J102, and are decoded according to the state of the Unit Number Selector Switch, which connects to J110, pins 5, 8, 9, 6, and 7, by U448, and U89 to produce the Select Signal (LSXXG). When the Unit Number Selector Switch on the front panel is set to one of the position numbers (1 through 4), one and only one of the signals at U448-4, U448-10, U448-8, and U448-6 (zone 6-6D,E,F) will be high. This will result in LSXXG being generated only when there is an assertion on the specific Unit Select line that corresponds with the number as designated by the Unit Number Selector Switch on the operator's panel.

The busy output utilizes the same signals developed from the Unit Number Selector Switch to gate the Busy Signal from the Position Control Logic onto the specific busy seeking line that corresponds to the particular setting of the Unit Number Selector Switch. This is accomplished by U86-6, U86-3, U86-8, and U86-11 (zone 6-5D,E). The common inputs to these NAND gates are enabled by the AND condition of the Busy Signal (from the Position Control Logic) and the Ready signal. When the drive is Ready, NLRXXG will be low, enabling U126-10 (zone 6-7D) to provide a high output level whenever the Busy Signal (NLBSXG) is low. This condition causes the Busy Signal to be transmitted on that line selected by the setting of the Unit Number Selector Switch. U68 and U69 (zone 6-3D,F) are line drivers for driving the Busy Seeking signals onto the respective I/O lines.

The Read/Write Control Logic controls the Write, Erase, and Read signals to the Read/Write PCBA. These signals depend upon the conditions of the input interface lines and certain signals generated on the Logic PCBA.

The Write Enable (IWEXR) and Erase Enable (IEEXR) signals are received and gated with NLSARG by U48-1 and U48-4 (zone 5-6E). These gates provide outputs only if the drive is selected and ready. The outputs of U48-1 and U48-4 are then gated by the AND condition of Position Mode (NLPMXG) and Write Protect Mode (LFPML). These signals are then routed to the Read/Write PCBA via J103. The Write and Erase signals to the Read/Write PCBA will be asserted if, and only if, the respective signal is received from the I/O interface, the drive is selected and ready, the drive is not in a file protect mode, and the positioner is in the position mode.

If either IWEXR, IEEXR, or both, is present, the low active Write Or Erase signal (NLWOEG) will be generated at the output of U48-13 (zone 5-6E). This signal is used in the Run/Stop Control Logic to prevent clearing the Load Heads F/F when either a Write or Erase operation is in progress. The Read Enable signal (IREXR) from the I/O interface is gated only by LSARG at NAND gate U87-8 (zone 5-6E) before being supplied to the Read/Write PCBA at J103.

The File Protect Logic performs several functions on the Logic PCBA. It provides front panel indication via the Protect Lamp indicators as to the state of the Protect Switches. The Write Protect Switches connect to J108 and their states are sampled by the Protect Switch Latches (U446 zone 5-7B) and the Protect Lamp Drivers (U426 zone 5-3A). Drive is provided to the front panel Protect Lamp indicators according to the states of the respective Protect Switch Latches. For those machines not fitted with Write Protect switches, jumpers in P108 will permanently disable both Write Protect Switch Latches. The state of the Protect Switch Latches is decoded according to the specific disk selected by the interface. This is accomplished by U405 (zone 5-6B). LRCSG and NLRCSG are inputs to this AND/OR gate and determine the specific Protect Switch Latch which is to be sampled and fed to the File Protect Mode Latch (U88 zone 5-5B).

The state of the respective Protect Switch Latch is fed to the File Protect Mode Latch if, and only if, a Write or Erase operation is not in progress. This is the result of NAND gates U88-11 and U88-3 (zone 5-5B). This is to provide a signal that indicates the specific disk protected from Write and/or Erase operations. The state of the File Protect Mode Latch is driven onto the File Protected (IFPXD) I/O interface line by the File Protected Status driver (U44 zone 5-1C) according to the state of a File Protect Mode Latch.

Also included on sheet 5 are line drivers for several of the interface output lines. The Read Signal Drivers (U67 zone 5-3D) take the Read Clock Signal (NRRCSG) and the Read Data Signal (NRRDSG) from the Read/Write PCBA via J103 (zone 5-8D) and drive these signals onto the Read Clock (IRCXD) and Read Data (IRDXD) interface lines via J102 (zone 5-1D).

The Malfunction Signal Driver (U65 zone 5-3D), and associated gate U403 provide an indication when an internal malfunction is detected. The Malfunction Detected (IMDXD) line is pulsed when an internal malfunction is detected. This is accomplished by NANDing the Delayed-Ready Condition (LDRCG) with the Emergency Unload F/F (LEUFF) at NAND gate U403-3 and driving the resulting signal onto the IMDXD line at J102.

Assuming that the drive is in the Ready condition as evidenced by the high level of LDRCG at pin 2 of U403 (zone 5-3E), any emergency will cause the Emergency Unload F/F to one-set, which causes the other input to U403 to go high. The high level at pin 2 will persist for

a short period of time even though the drive will go Not-Ready as soon as the Emergency Unload F/F is one-set. This is true since the transition from Ready to Not-Ready will take a short period of time to propagate through the Delayed Ready Condition circuit. Therefore, for that length of time, both inputs of U403 will remain at the high logic level.

As soon as the Ready to Not-Ready transition has propagated through the Delayed Ready Condition circuit, pin 2 of U403 will go low. This terminates the Malfunction Detected pulse that is applied to the interface output by line driver U65-5.

Double Track Drive (IDTDD) is indicated by driving the Selected (NLSXXG) signal onto this interface line. Illegal Cylinder Address (IICAD) is indicated at the interface by driving that line with NLIAXG via U3 (zone 5-3C). NLIAXG is generated in the Position Control Logic.

A split-quad (emulates two duals in one drive) drive is indicated at the interface by driving the Dual Platter Drive line with the Dual Platter signal (NLDPSG) via U45 (zone 5-3B). NLDPSG is made up in Programming Array plugged into J125 (sheets 9 through 12 of the Logic PCBA schematic) from either a steady logic-one signal or the low active NLSXXG signal depending on whether the machine is a quad-disk or a split-quad drive.

The Termination Voltage Power Supply is shown in zone 5-1E of the schematic. This is a nominal +3.5v source which is provided to the interface for those models requiring compatibility with D5000 termination voltage. This supply is derived by using diodes CR1 and CR2 in conjunction with R10 to provide a voltage drop from the internal +5v supply for supplying termination voltage to connector J102. Likewise, CR3 and CR4, in conjunction with R11, provides a reduced voltage from the +5v supply at J101. For those versions of the Logic PCBA that do not use the Termination Voltage Power Supply, pins A45 and B45 on J102 are wired to like pins on J101 by jumper W3. This provides feed-through of the termination voltage when this voltage is supplied by the controller. In that case, CR1, CR2, R10, CR3, CR4, and R11 are omitted.

The Special Signal Driver (U44 zone 5-2C) is a line driver reserved for driving special interface signals in those machines having that option (see Paragraph 3.17.13).

The Chassis Ground Connection is shown in zone 5-6C of the schematic. For drives having ordinary grounding, W5 connects the I/O ground directly to the chassis. For machines requiring ground isolation, W21 is omitted and the I/O ground is connected to the chassis ground through a complex impedance consisting of R14 and C3, W4 and W6.

5.5.2 SHEET 7 (SCHEMATIC 108165)

Sheet 7 of the schematic pertains to the speed control electronics. The purpose of this circuitry is to compare the time of occurrence of the positive transition of the LPLFF flip-flop square wave with the time reference obtained from the crystal oscillator countdown (refer to Paragraph 5.8.1). The result of the comparison is two signals, one indicating the Instantaneous Motor Speed error (NLIMSI) and, if appropriate, another signal which will indicate a gross malfunction of the speed control, Speed Out of Tolerance (LSOTF).

When the Drive Motor Enable (LDMEG) signal is high and the drive motor is enabled, Speed Sequence Register U244 (zone 7-7D), Increase Motor Speed F/F U243 (zone 7-2G), and Speed Out Of Tolerance F/F U243 (zone 7-2F) are released to operate. The Speed Sequence Register, in conjunction with gates U165-6 and U223-3, functions as an edge detector. It also establishes the sequencing of the events in determining the disk speed. For each low to high transition of the Phase Lock F/F signal (LPLFF), a one-clock-time pulse, Transfer Speed Count (LTSCG), is generated. One clock time thereafter Speed Count Reset (NLSCRG) is generated to reset the speed counting logic. The clock frequency utilized by the Speed Sequence Register is the same clock frequency counted by the Speed Control Counter and is determined by the Speed Control programming array plugged into J121 (zone 7-8G). This selects one of three possible clock signals from the clock countdown.

At the time LTSCG is generated, the states held in Speed High Limit F/F U143 (zone 7-4H), Disk Speed Low F/F U242, and Speed Low Limit F/F U242 are transferred into Increase Motor Speed F/F U243 (zone 7-2G) and Speed Out Of Tolerance F/F U243 (zone 7-2F). Specifically, the state of the Disk Speed Low F/F is transferred to the Increase Motor Speed F/F. Either a one-set condition of the Speed High Limit F/F, or a one-set condition of the Low Limit F/F is transferred to the Speed Out Of Tolerance F/F if either of those flip-flops were one-set. This would be the case only if a gross speed error is being detected.

The Speed High Limit F/F, the Disk Speed Low Limit F/F, and the Speed Low Limit F/F are referred to as the speed value flip-flops. The specific values stored in these flip-flops are the result of the previous speed count. After the values stored in the speed value flip-flops are transferred to the speed status flip-flops (Increase Motor Speed and Speed Out of Tolerance F/F) by the Transfer Speed Count (LTSCG) pulse, then, one-clock time later the speed control logic is reset by NLSCRG which is a one-clock period low active pulse. This resets the Disk Speed Low F/F, the Speed Low Limit F/F, and presets the Speed High Limit F/F to establish the initial conditions at the speed value flip-flops for the next count. Also, the Speed Control Counter is loaded with a predetermined number from the Disk Speed Count Programming array plug J122. This determines the disk speed count programming according to the state of the Purge Cycle F/F.

The speed control counter, U202, U221, and U241 (zones 7-7F, 7-6F, and 7-5F) counts from the value loaded until the next Transfer Speed Count pulse occurs. The count rate is determined by the specific clock signals selected by the Speed Control Programming array plug, J121. If a count condition occurs in the Speed Control Counter which satisfies the decode of either U223-8 or U223-11, then that value will be stored in the respective speed value flip-flop. At the time of the next Transfer Speed Count pulse, the value decoded and stored in the speed value flip-flop will then be transferred to the speed status flip-flops. Note that two different values may be loaded into the Speed Control Counter at the time of a Speed Count Reset pulse. One is the normal running speed which will occur when the Purge Cycle F/F is zero-set, and the other value is a 10 percent overspeed which will be loaded when the Purge Cycle F/F is one-set.

The state of the Speed Out of Tolerance F/F is directly tested during a start sequence to determine if there is a gross speed error prior to loading the heads. Once the machine has reached the ready condition, an occurrence of a logic one at the Speed Out of Tolerance F/F output (LSOTF) will be gated by U262 with the Ready signal (LESDG) producing the Disk Speed Error (NLDSEG) signal at pin 8 in U262 (zone 7-2G). Disk Speed Error can therefore occur only during the time that the drive is Ready.

The state of the Increase Motor Speed F/F at the end of each speed count interval will indicate a basic binary error derived from the comparison of the time reference to the actual speed. This flip-flop will be preset by the Start Drive Motor (NLSDMG) pulse as a means of initializing the speed status during a start sequence. Note that the result of the time-speed comparison is a single binary digit that can have only two possible states; one or zero, indicating that the speed is either too fast or too slow. If it is too slow, the Increase Motor Speed F/F will be in the one-set condition indicating that the motor speed should be increased. Conversely, if the speed is too fast, the Increase Motor Speed F/F will be zero-set, indicating that it is unnecessary for the motor speed to be increased and allowing the motor to coast down through the desired speed value.

5.5.3 SHEETS 8 AND 9 (SCHEMATIC 108165)

Sheet 8 of the Logic PCBA schematic contains the Position Control Logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The overall purpose of the Position Control Logic is to accept cylinder addresses from the I/O interface and control the positioning and holding of the positioner at these addresses. The subsidiary function of this logic is to execute Restore operations and to control loading and unloading of the heads. The actual control functions within this logic are performed by the Load Address Logic, Busy Logic, Mode Control Logic, and Operation Control Logic.

The Mode Control portion of the Position Control Logic consists of the Position/Velocity Mode Logic (zone 8-4A), the Forward Slow Mode F/F (zone 9-3C), and the Reverse Slow Mode F/F (zone 9-3D). The Position/Velocity Mode Logic determines when the positioner servo should be operated in the Position Mode and when it should be operated in the Velocity Mode. This logic also supplies the Position Mode (LPMXG) signal and the Velocity Reference Enable (NLVREG) signal to the Servo PCBA.

The Forward Slow Mode F/F U167 (zone 9-3D) determines the state of the Forward Slow Mode (NLFSM1) signal on pin 24 of J104 (zone 9-1D), which is supplied to the Servo PCBA, to cause the positioner servo to operate in the Forward Slow Velocity Mode. Likewise, the Reverse Slow Mode F/F U207 (zone 9-3C) functions to store and provide a state which asserts Reverse Slow Mode (NLRSM1) to the positioner servo for operating the positioner in the Reverse Slow Velocity Mode. The Forward Slow Mode is used when loading heads and during the last portion of a Restore operation. The Reverse Slow Mode is used when unloading heads and during the first portion of a Restore operation.

The Forward Slow Mode F/F U167 is released for operation when the Load Heads F/F (LLHFF) is one-set. Prior to loading, the heads will be retracted. This condition is indicated by Heads Retracted (SHRXG) being high, which in conjunction with one-setting the Load Heads F/F, results in a high logic level from U187-4 (zone 9-4D). A high output at U187-4 causes the Forward Slow Mode F/F to be preset to commence loading the heads.

When performing a Restore operation, presetting the Forward Slow Mode F/F is controlled by the setting of the Restore Operation F/F U207 (zone 9-3B). The Restore Operation F/F determines whether the address as asserted by the interface will be examined or whether it will be disregarded and a Restore operation performed.

The Restore Operation F/F U207 will be preset by the low active pulse from U49-6 (zone 9-4D). This pulse will occur if the Restore Initial Cylinder (IRICR) line is active at the time that a Cylinder Address Strobe (ICASR) is supplied from the I/O interface. At that time, pins 4 and 5 of U49 will be high, presetting the Restore Operation F/F. When this flip-flop is preset, U187-10 is enabled to preset the Forward Slow Mode F/F by the negation of Position Transducer Index (SPTIG) during the latter portion of a Restore operation.

The Forward Slow Mode F/F is zero-set by the first high-to-low transition of Position Quadrature Clock (SPQCG) that occurs after the change-of-state of SPTIG during loading of the heads. Since this occurrence must follow after the change-of-state of SHRXG, both SHRXG and SPTIG are ANDed by U187-1 (zone 9-4D).

The Reverse Slow Mode F/F U207 (zone 9-3C) is preset at the same time that Restore Operation F/F U207 (zone 9-3B) is preset when a Restore operation is commanded. The Reverse Slow Mode F/F can also be one-set when the Load Heads F/F is zero-set. This results from NLLHFF being high, enabling the J input of the Reverse Slow Mode F/F. The Reverse Slow Mode F/F is cleared when the Forward Slow Mode F/F is preset.

When either of the slow mode flip-flops are one-set, the demand address clear condition will occur via U165 (zone 9-2D). This will clear Demand Address Registers U301, U321, and U302 (zone 8-6F,G,H). In addition, Demand Address Clear, in the form of a low active signal (NLDACG), will disable Count Clock Detector Register U323 (zone 8-6B) by clearing it to an

all zeros condition and will cause the Current Address Counter, U322, U381, and U342 (zone 8-4D) to load all ones. NLDACG also forces NLVREG to the high logic level via U403-8 (zone 8-3B) disabling the velocity reference and forcing Not Position Mode (NLPMXG). In this manner, the logic is initialized and conditioned during the time the heads are being loaded or retracted, or during execution of a Restore operation.

When a demand address clear condition does not exist (both the Forward Slow Mode and Reverse Slow Mode F/Fs zero-set), the Count Clock Detector Register U323 (zone 8-6B), Demand Address Registers U301, U321, and U302, and Current Address Counter (zone 8-4D) will be released. The Velocity Reference Enable and Position Mode signals will be under control of the other gates.

In the Position/Velocity Mode Logic when Not Demand Address Clear (NLDACG) is high (a Demand Address Clear condition is not occurring), the Position Mode signal will be asserted when the address difference is zero and the Position Quadrature Clock is low. This will be the case when the Current Address Counter contents agree with the Demand Address Register contents and the positioner is within one-quarter track of the true-track center line.

The purpose of the Load Address Logic is to generate a low-active pulse, Load Address (NLLAXG), when a Cylinder Address Strobe (ICASR) is received from the I/O interface and the address on the Cylinder Address Lines is a valid address. Another function of this circuitry is to generate a Busy Signal to the I/O interface when a Strobe is received, or when the positioner is Busy Seeking. Another function of this logic is to generate an illegal address indication to the I/O interface when the address on the interface lines is invalid at the time that a Strobe is received.

ICASR is received via J101, inverted, and shifted through the Strobe Shift Register U108 (zone 9-6G). When the level change first occurs at bit A of the strobe shift register, the Hold Busy Time F/F U128 (zone 9-4G) is caused to one-set, which results in immediate assertion of the Busy Signal to the interface. This also releases the previously cleared Hold Delay Shift Register U147 (zone 9-3F). The Hold Delay Shift Register, however, does not propagate logic ones because the A bit is still in the logic one condition. The strobe trailing edge is edge-detected by the combination of U127-4 and U127-1 to generate Address Pulse (LAPXG zone 9-5H). LAPXG samples the state on the Restore Initial Cylinder Line (IRICR) at U49-6 (zone 9-4D) to determine if the Restore Operation F/F and Reverse Slow Mode F/F should be preset to commence a Restore operation.

The Address Pulse also enables the input (pin 1) of U107 (zone 9-5H) and, if the cylinder demand address is valid (as determined by the Valid Address Decoder), and if the positioner is not seeking (as determined by the state of the Busy Time F/F), then the Load Address Pulse (NLLAXG) will be generated. This pulse causes the Demand Address Register to load the address that is present on the Cylinder Demand Address Lines.

NLLAXG also clears the Illegal Address F/F U167 (zone 9-2G) if it was one-set from any previous illegal address condition. When Strobe Shift Register Bit A goes low, at the time of the trailing edge of the Strobe, this causes logic ones to propagate through the Hold Delay Shift Register. This level change propagating through the register will result in zero-setting the Busy Hold Time F/F U128 (zone 9-4G). This removes the Busy Signal from the interface if the positioner has not gone busy. This would be the case if an illegal address or an address that is the same as the current position has been received.

It is important to note that the Strobe Shift Register is able to accept Cylinder Address Strobes from the I/O interface only when it is released for operation by a high-logic level on the Selected And Ready (LSARG) line. Note also that the Illegal Address F/F U167 (zone 9-2G) is clocked by the high to low transition of the Strobe Shift Register, bit A. If the J

input of the flip-flop is a logic one at the time of that transition, then the Illegal Address F/F will be one-set. This would be the case if the Busy Time F/F is one-set, or if the output of the Valid Address Decoder is at the low logic level, indicating an invalid address. Therefore, the Illegal Address F/F will indicate an illegal address if the positioner is already busy, or if the address is invalid at the time of a Cylinder Address Strobe. Notice that the Illegal Address F/F can be cleared by either unloading of the heads (LLHFF goes low), or by a valid address being accepted (NLLAXG generated), or by one-setting the Restore Operation F/F when a restore operation is commenced.

The Illegal Address (NLIAXG) signal from U107 (zone 9-1G) is supplied to the interface by a line driver (sheet 5, zone 3C) only if LSARG is at a logic one level. Also, during the time that the Strobe Shift Register, bit B, is in the logic one condition, the illegal address signal to the interface is disabled by U107-11 (zone 9-1G). If an address is loaded into the Demand Address Register (zone 8-6G) which is different than the address stored in the Current Address Counter (zone 8-4E), then an address difference will be produced. This difference results in the Position Mode (LPMXG) signal going low (zone 9-6E). This will cause presetting of the Busy Time F/F which indicates that the positioner will be busy executing a seek. This signal is supplied to the I/O interface. Additionally, the Settle-Time Delay Register U109 (zone 9-5E) is cleared in preparation for determining the settling time at the end of the seek.

Notice that the Busy Signal (NLBSXG) to the I/O interface from the Hold Busy Time F/F U128 (zone 9-4G) and the Busy Time F/F U128 (zone 9-5F) is enabled only when these flip-flops are released by a high logic level of the Ready signal (LRXXG). As the positioner completes the seek, the address difference will reach zero and the positioner will reach a position that is within a quarter-track of the true-track center line. At this time, Position Mode will be asserted causing LPMXG (zone 9-6E) to go high. Since LPMXG is applied to the Settle-Time Delay Register, it will commence propagating logic-ones through the register. After the delay, determined by the register propagation time, the End Busy (LEBXG) signal will cause zero-setting of the Busy Time F/F and the Restore Operation F/F. This terminates the Busy Signal to the interface and also terminates any restore operation status in the Operation Control portion of the Position Control Logic.

The Settle-Time Delay Register U109 (zone 9-5E) is clocked by LC13F from the clock countdown. Therefore, the delay time established by the Settle-Time Delay Register is determined by the clock frequency and the number of bits that must be propagated after the level change on the Position Mode (LPMXG).

The validity of a demand address on the I/O interface lines is tested by the Valid Address Decoder (zone 8-6E). The Valid Address Decoder is a combinational logic configured to provide an output signal that will be high if the input Cylinder Demand Address is within the legal range of values, and to provide a low logic level output when the Cylinder Demand Address lines have an address outside the legal range. The range of legal addresses for 406 cylinder models is from 000 to and including 405.

As previously described, the Demand Address Register (U301, U321, and U302 zone 8-6G) will either hold the last value, load a new value if the NLLAXG pulse occurs, or will be cleared and held if a Demand Address Clear condition occurs. Therefore, the contents of the Demand Address Register will either be all zeros or the last Demand Address loaded. The contents of the Demand Address Register therefore specify the present cylinder demanded.

The current position of the positioner is stored in the Current Address Counter (zone 8-4D). The Current Address Counter is an up/down counter. The direction and amount of the count is determined by the count control on the basis of the Position Reference Clock (SPRCG) and the Position Quadrature Clock (SPQCG) signals from the Servo PCBA. These

digital signals are derived from the outputs of the position transducer. During loading of the heads, the Current Address Counter is first loaded to a condition of all ones and then counted by one upcount clock to an all zeros condition to initialize the Current Address Counter at cylinder 000.

Each high-to-low transition of SPQCG is edge detected by the Count Clock Detector Register U323 (zone 8-6B). A one-clock time pulse is generated for each high-to-low transition of SPQCG and this pulse, via U383-4, is used to strobe the Up/Down Count Logic. If during the time of the count clock pulse, SPRCG is high, the Current Address Counter will be counted down. If, however, SPRCG is low during the time of a count clock, the Current Address Counter will be counted up. An UP count increases the value in the address counter indicating that the positioner is moving toward the spindle, and a DOWN count clock decreases the value stored in the address counter indicating that the positioner is moving away from the spindle.

During a seek, the positioner servo is operated as a velocity type of servo. A particular velocity level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Function Generator on the Servo PCBA by the Address Difference lines (NLAD0G through NLAD7G, including NLADEG) (zone 8-1G).

The address difference, that is the difference between the Current Address Counter contents and the Demand Address Register contents, is obtained by performing a ones-complement arithmetic subtraction on the binary values of those counter and register contents. This subtraction process is performed by the Subtractor (zone 8-3G) and Complementor (zone 8-2G). The actual subtraction is mechanized using an integrated circuit binary full-adder.

Since the arithmetic is ones-complement arithmetic, an end around carry is used. This carry is under control of the Carry Control Logic (zone 8-2D). The algebraic sign of the velocity is determined on the basis of the binary value of the carry which specifies the binary state that is on the Forward Direction Line (LFDX1).

The end around carry circuit can be traced on the schematic starting at U402 (zone 8-3H) at the pin 14 output and proceeding to U361, pins 2 and 13, and from there through the Carry Control F/F U341, pin 15, and then to the input of U382. Note that the input to the Carry Control F/F determines the state on LFDX1.

As shown on the schematic, the integrated circuit binary full-adder is connected in a ripple-carry fashion to close the remainder of the end around carry loop. Notice also that the input to the least significant adder from the output of the Carry Control F/F U341-15 also controls the Complementor.

The Complementor circuit is required for the situation where negative arithmetic is being performed. The Complementor provides conditional inversion of the outputs of the Subtractor according to the state of the carry into the Subtractor.

When the heads are being loaded, it is necessary to force the carry to a particular state. This is accomplished by the Carry Control on the basis of the states from certain bits in the Current Address Counter. U361-6 (zone D10) essentially decodes all-ones states in the most significant bits of the Current Address Counter and forces the carry to a specific state during the time that the heads are being loaded. Only during that time will the Current Address Counter have logic ones in the most significant positions of the counter. By forcing the carry during the loading of the heads, a least significant velocity reference level is specified by NLAD0G, such that between the time when the Forward Slow Mode operation is ended and the Position Mode is commenced, the positioner servo is operated

as a true velocity servo with a least significant velocity reference. The three most significant bits of the Current Address Counter are buffered by U441 and U443 (zone 8-2E) and sent to the Temperature Compensation PCBA via J114.

The Error Check Logic (zone 9-6B) performs two types of checks concerned with the operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This is done by the Seek Time Error Check Counter U287 (zone 9-7C). This is a gross type of check to determine that the positioner has not become stalled due to a fault. While each seek is checked by the circuit, it does not verify that a specific distance moved was accomplished within the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The Seek Time Error Check Counter is enabled to count the LC17F clock, from the clock countdown, whenever the Busy Time F/F is one-set. This is a result of Not Busy Time (NLBTFF) being fed to the input of U247 pin 9 (zone 9-7B).

If the counter has not counted up to the state where the carry-out has occurred, then the inputs at pins 9 and 10 of U247 will be high when the positioner is not busy. This causes U247-8 to go low, loading all zeros into the Seek Time Error Check Counter U287. When all zeros are loaded into the counter and the load input is held at the low level, the counter is locked up and cannot count the LC17F clock. However, when the positioner goes busy, NLBTFF goes low causing U247-8 to go high, releasing the counter and allowing it to count the LC17F clocks.

If the Busy Time ends before the counter has counted up to the carry-out condition, then the seek has been completed well within the maximum allowable time, the Busy F/F will again load zeros into the counter before the carry-out has occurred. Should the positioner become stalled however, or other faults develop which cause the Busy signal to exist for a sufficient period of time for the counter to count to the carry-out condition, then the carry-out U287 pin 12 will go low indicating a Seek Time Error (NLSTEG). This results in execution of an Emergency Unload.

Notice that the Restore Operation F/F (LROFF) is fed to the clear input of the Seek Time Error Check Counter. This signal clears the counter during the time of a Restore operation. It is not desirable to check Seek Time during a Restore operation.

The other check performed by the error check logic is to determine that the positioner has not traveled outside the legal range of travel. This is performed by the Position Limit Monitor circuitry shown in zone 9-6B. This circuit generates a Position Limit Error signal (NLPLEG) if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded on the disk.

The Position Limit Monitor F/F U267 (zone 9-6B) is cleared by NLLPNG. This signal will be low and therefore clear the flip-flop whenever the Purge Cycle F/F and the Load Heads F/F are both zero-set. This will occur when the drive is not in a Run Condition or it is in the Run Condition but not yet in a Purge Cycle. This can be seen by examining the logic shown on sheet 4 of the Logic PCBA schematic.

When loading heads, the Load Heads F/F will be one-set, thus assuring that the Position Limit Monitor F/F is released for operation. Note that the J input of the Position Limit Monitor F/F is continuous logic one, and therefore any high-to-low transition on the clock input of the flip-flop U267 pin 1 will clock the flip-flop into a one-set condition. The flip-flop will remain one-set until it is cleared by NLLPNG going to the low-logic level.

During the loading of the heads, the Restore Operation F/F will be zero-set. As the positioner moves forward, SPTIG will come to the high logic level causing pins 4 and 5 of U247 (zone 9-7B) to be high, thus causing a low-to-high transition at U267 pin 1. As the heads load, SPTIG will go from high back to low, which will cause U267 pin 1 to go from a high to a low. This will one-set the Position Limit Monitor F/F, arming the monitor.

When the Position Limit Monitor F/F one-sets, the NAND gate U247 (zone 9-5B) is enabled at its input on pin 12. A positioner fault may be indicated by either an occurrence of SPTIG, or by the occurrence of Heads Retract, after the heads have been loaded. If SPTIG goes high, it indicates that the positioner has traveled outside of its legal range. This will cause U247 pin 2 to go low which in turn will result in U247 pin 11 going low, thus indicating Position Limit Error (NLPLEG).

The other method for detecting a fault is if SHRXG goes high. This will force U247, pin 1 (zone 9-6A), to the low logic level, and again U247, pin 11 will go low, indicating NLPLEG. Either condition results in emergency unload. The success of emergency unload will depend on the nature of the fault that originally caused the occurrence of SPTIG or SHRXG.

If a multiple SPTIG occurs during the loading of the heads, this circuit will detect that occurrence and immediately commence an emergency unload before allowing completion of loading the heads. Likewise, this circuit will detect faults in the position transducer.

5.5.4 SHEETS 10, 11 AND 12 (SCHEMATIC 108165)

Sheet 10 of the Logic PCBA schematic contains the Sector Electronics portion of the D3000 logic. Refer to the functional discussion and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The purpose of this circuitry is to provide pulses at the I/O interface for electrically subdividing the storage surface into sectors. In addition to the pulses provided, the specific number of the sector passing under the Read/Write heads is also transmitted as a sector count which is used for addressing data stored on the disk. An index pulse is provided as an output. This provides a signal which is a pulse occurring once per revolution of the disk that can be utilized to define the sector reference.

There are two basic types of sectoring; mechanical and electronic. The electronic type may be further classified into electronic sectoring with the index-only type of cartridge, and electronic sectoring with a multi-notch cartridge.

The primary inputs to the sector circuits are derived from two sensors located in the drive, and from clock signals derived from the Clock Countdown (sheet 6). The Drive/Motor Enable signal is also used in the sector electronics circuits. The Upper Platter Select signal and Selected And Ready signal are employed to control the output multiplexer. These signals are also obtained from the Start/Stop Control Logic.

The outputs of the sector electronics are the Sector Pulse (ISPXD), the Index Pulse (IIPXD), zones 10-1C and 10-1A, and the Sector Count (ISC0D—ISC6D), zone 12-1A—D.

ISPXD provides a train of pulses at regular intervals during each revolution of the disk. These pulses divide the disk surface into 'n' equal segments, where 'n' is the number of pulses and the number of sectors.

IIPXD is a pulse train with a single pulse occurring once per revolution of the disk. This pulse always occurs just prior to sector zero.

The Sector Count lines specify the sector count, which is presented to the I/O interface in a binary format. This count indicates the particular segment of the disk surface currently under the Read/Write heads. The signals on these lines are, in essence, the states of a binary counter and in all cases correspond only to the respective disk as selected by the Platter Select line.

The particular type of sectoring for which a drive is configured is determined by the programming arrays that are installed in the Logic PCBA. The parameters that are programmed into these arrays determine the nature of the sectoring. These parameters are: type of sectoring, number of sectors, and related disk speed.

The type of sectoring is programmed by the programming array plug installed in J125 (zone 11-1D). The values for the Upper and Lower Demultiplexer Counters, which are relative to the speed of the disk, are programmed by J121 (zones 11-2H and 11-2E).

The number of sectors for electronic sectoring for the lower and upper platters is programmed by J126 and J127, respectively, shown on sheet 12.The PLL sectoring is configured by the programming array plug installed in J123 shown on sheet 10. These arrays determine certain parameters of the electronic sectoring.

The Upper Sensor Detector (zone 11-6G) and the Lower Sensor Detector (zone 11-6D) receive signals from the upper and lower sensors via J112 (zone 11-8D—G) and convert these analog signals into digital form. The Lower Sensor Detector circuit is similar to the Upper Sensor Detector except that it has the additional capability of changing thresholds.

The Upper Sensor Detector has two amplifiers, U429 and U389, which are not required in the Lower Sensor Detector. Otherwise, the circuit functions are similar. The Upper Sensor Detector receives the signal derived from sensing the upper cartridge sector ring or armature plate and converts it into a digital pulse train. The Lower Sensor Detector converts the analog signal obtained from the Lower Magnetic Sensor, which senses the Phase Lock Ring into a digital pulse train.

NOTE

The removable cartridge may be sectored either electronically or mechanically. The lower disk is always sectored electronically.

Standard top loading cartridges are fitted with an armature plate having one notch which is the Index notch. Some specially modified top loading cartridges will also have notches used for mechanical sectoring.

Standard front loading cartridges have slots for mechanical sectoring, and a single index slot. The sector slots and index slot are located in the sector ring. Some specially designed front-load cartridges have only an index slot in the sector ring.

Front loading models of the D3000 employ a photoelectric type of sensor for the upper sensor. Top loading models use a magnetic transducer for the upper sensor. On all models, the lower sensor is a magnetic transducer. The upper sensor for front loading models connects to J112 pin 9 (zone 11-8G). For top loading models, the upper sensor is connected to J112 pin 6 (zone 11-8G).

U429 (zone 11-7G) serves as a fixed voltage gain amplifier when the magnetic sensor is connected and functions as a current-to-voltage converter when the photoelectric sensor is connected. Gain for the circuit is established by R51, R52, and R53 (or W24) for the magnetic sensor connection and by R50, R52, and R53 (or W24) for the photoelectric sensor. C22 determines bandwidth. C20 and C21 decouple power supply voltages for U429. The signal from U429 is coupled to voltage follower U389 by an R-C network, C23 and R54.

The output of voltage follower U389 is fed directly to a Schmitt trigger comprised of one section of U408. The Schmitt trigger threshold is determined by R57, R56, R55, and the + 5v power supply voltage. The output of the Schmitt trigger is buffered by U407-8 and fed to the Upper Time Demultiplexer. The signal at this point will be a pulse train with one pulse per slot, or notch, detected by the sensor. Power for operating the photoelectric sensor for front load machines is supplied via connector J112 (zone 11-1G).

The lower sensor detector functions in a manner similar to the upper sensor detector. The lower magnetic sensor connects to J112 pin 4 (zone 11-8D). The output of this sensor is filtered by R61 and C27, then fed directly to a Schmitt trigger consisting of the other half of U408 (zone 11-6D). The threshold for the high threshold mode is determined by R66, R68, R64, R62, and R63. For the high threshold mode, the output of U446-10 (zone 11-6C) will not be conducting; therefore, R67 will be essentially open circuited. In the low threshold mode, which will be the case whenever Drive Motor Enable (LDMEG) is low, the end of R67, which is connected to U446-10, will be connected to ground. Therefore, the threshold for the low threshold mode will be determined by R66, R67, R68, R64, R62, and R63. The outut of the Schmitt trigger is buffered by U407-4 and U222-8 and fed to the Lower Time Demultiplexer. U407-4 also feeds the Lower Detector Pulse (LLDPT) to the Disk Rotation Detector Counter (sheet 3) for detecting disk rotation.

The pulse trains obtained from the Sensor Detectors will have an index pulse intermixed with the other pulses if the sensor is detecting multiple notches. This will be the case at all times for the Lower Magnetic Sensor which senses the Phase Lock Ring. However, the pulse obtained from the index notch from the Upper Sensor will be interspersed with the pulses obtained from the sector notch only if it is a multi-notch cartridge. In the case of an index-only cartridge, the pulse train will be comprised entirely of index pulses. The pulse obtained from the index notch must be separated from the sector notches as appropriate. This function is performed by the time demultiplexers for those situations requiring demultiplexing. The pulse obtained from the index notch is placed on a line separate from the other pulses.

The Lower Time Demultiplexer (zone 11-2D) separates the pulse obtained from the index notch on the Phase Lock Ring from the phase lock pulses. The phase lock pulses will be demultiplexed and output at U183 pin 13 (zone 11-2C). The index notch pulse is output at U183-10 (zone 11-2C). Only a single clock frequency is utilized by the Lower Time Demultiplexer; this is LC08F (zone 11-4C), obtained from the clock countdown in the Start/Stop Control Logic (sheet 4).

In index-only cartridges, the Upper Time Demultiplexer outputs the pulse obtained from the index notch at U183 pin 4 (zone 11-2F). Since there are no sector notches, there will be no output at U183 pin 1.

When using a multi-notch cartridge, the Upper Time Demultiplexer will output the demultiplexed index pulse at U183 pin 1 (zone 11-3E) and the demultiplexed sector pulses at U183 pin 4. The clock frequencies used with the Upper Time Demultiplexer are determined by a jumper installed at W20, W19, or W21 (zone 11-4F). Clock LC08F, LC09F, or LC10F from the clock countdown is available at W20, W19, and W21, respectively.

For both time demultiplexers, the specific value of the demultiplexing gate time is determined by the programming array installed in J121 (zone 11-2E). The time demultiplexer functions by generating a gate time according to the value loaded into the demultiplexer counter. The Upper Time Demultiplexer Counter (Upper Demux. Counter) is U184 (zone 11-2G) and the Lower Time Demultiplexer Counter (Lower Demux. Counter) is U164 (zone 11-2D). The value loaded into these demultiplexer counters is determined by the programming array plug in J121.

Generation of the demultiplexer gate is controlled by the respective Demultiplexer Control F/F U203 (zone 11-4G) for the Upper Time Demultiplexer and U163 (zone 11-3D) for the Lower Time Demultiplexer. The outputs of U203 and U163 are fed to the Upper and Lower Time Demultiplexer Gate F/Fs, respectively. The actual demultiplexer gate is obtained from the respective demultiplexer gate flip-flop. The output of the respective demultiplexer flip-flop is the enabling input to demultiplexing gates U183-4, U183-1, U183-10, and U183-13 (zone 11-3F and 11-2C).

The time demultiplexer functions on the principle that for a pulse occurrence, a gate is generated. If, during the time of that gate, another pulse occurs, that pulse is derived from the index notch. All other pulses are taken as being derived from other than the index notch. The specific demultiplexed pulses are connected to the Sectoring Selection Programming array at J125 (zone U-11B—F). The outputs of the Sectoring Selection Programming array are fed to pulse formers and sector number counters.

The pulses obtained from the time demultiplexers or from the electronic sectoring electronics are unsuitable for direct output at the I/O interface; therefore, they must be formed into pulses compatible with the interface requirements. This is accomplished by the Pulse Formers shown in zones 10-5C and 10-5B. There are four pulse formers; one for the Upper Sector Pulse, one for the Lower Sector Pulse, one for the Lower Index Pulse, and one for the Upper Index Pulse.

The pulse formers are essentially shift registers (U22, U2, U23, and U43) connected as delays and edge detectors. The actual pulse forming is accomplished by NOR gates U63. The clock used for determining pulse timing and delay is LC04F, which is obtained from the clock countdown in the Run/Stop Control Logic.

The outputs of the Upper and Lower Sector Pulse Formers are multiplexed onto the single Sector Pulse line (ISPXD) U62-8 (zone 10-2D). The pulse driven by U64-5 (zone 10-2D) depends upon the particular disk selected by the interface. Likewise, the outputs of the Upper and Lower Index Pulse Formers are multiplexed by the Index Pulse Multiplexer U62-6 and fed to the single Index Pulse line (IIPXD), according to the particular disk selected by the interface.

The Sector Pulse Multiplexer and the Index Pulse Multiplexer are controlled by the Multiplexer Control Logic (zone 10-5A) which also controls the Sector Count Multiplexer according to the states of the Platter Select line (LUPSG) and the Selected And Ready line (NLSARG). NLSARG enables the Multiplexer Control gates only when the drive is selected and ready. Thus, the output of the Multiplexer Control Logic is gated with NLSARG.

The specific multiplexer (upper or lower) enabled is determined at the input to the Multiplexer Control Logic by the states on NLUPSG and LUPSG. These signals are derived from the LUPSG input to the Disk Drive Function Control Logic, as shown on sheet 5 of the schematic.

When the drive is not selected, or not ready, then both LUMEG and LLMEG will be low, disabling the multiplexers. When the drive is selected and ready, then either LUMEG or LLMEG will be high, according to whether the upper or lower disk is being selected by LUPSG. Thus, the action of the Multiplexer Control Logic is to determine which of the pulse and sector count outputs will be enabled and supplied to the I/O interface, J102.

The pulses obtained from the Sectoring Selection Programming array at J125 are also applied to the Sector Number Counters and the Count Control Logic to generate the sector count. The Upper Sector Number Counter (zone 12-5D) and the Upper Count Control F/F (zone 12-6D) generate the upper sector number count. U144 and U145 are the Upper Sector Number Counters, and the count is controlled by the Upper Count Control F/F U83. The

Lower Sector Number Counter (zone 12-5B) and the Lower Count Control F/F (zone 12-7B) generate the sector number count for the lower disk. U125 and U124 are the Lower Sector Number Counters, and the count is controlled by the Lower Count Control F/F U83.

The contents of the particular sector number counter are multiplexed onto the Sector Count lines (ISC0D—ISC6D) through the Sector Count Multiplexer (zone 12-3C) according to the control signals generated by the Multiplexer Control Logic. U104 and U105 form the Sector Count Multiplexer. One or the other of the sector number counter contents will be selected and supplied to the line drivers according to the control signals from the Multiplexer Control Logic. For each sector count line, there is a separate line driver. The specific sector number count multiplexed onto the sector count lines is determined by which disk is selected by LUPSG and will only be presented to the I/O interface if the drive is selected and ready.

The mechanization of the Upper Sector Number Counter and Upper Count Control is identical to that used with the Lower Sector Number Counter and Lower Count Control. Therefore, only the Upper Sector Number Counter and Upper Count Control F/F will be explained.

The sector number count is represented by the binary value contained in the sector number counter. The Q_A output of U145 (zone 12-5D) is the least significant bit and the Q_C output of U144 (zone 12-4D) is the most significant bit. The counter is clocked, or counted up, by the raw sector pulse obtained from the Sectoring Selection Programming array plug at J125 (zone 11-1B—F). For each pulse, the counter will be incremented by one count. The Index Pulse, which occurs once per disk revolution, is defined as occurring during the sector just prior to sector zero; i.e., during sector N minus one where N is the maximum number of sectors. Therefore, at the time of occurrence of the Index Pulse, U83, the Upper Count Control F/F (zone 12-6D) will be preset by the occurrence of the Index Pulse.

This will cause the Q output of U83 pin 7 to go low enabling the load inputs (LD) of U145 and U144. However, the counter will not load zeros until the next sector pulse. At that time, instead of incrementing the count, it will be clocked to load all zeros. At the time that this clocking occurs, the Upper Count Control F/F will be zero-set since the K-input of the flip-flop is enabled at all times. This will remove the enable from the load inputs of the Upper Sector Number Counter and allow it to be incremented or clocked by the raw sector pulse. The Sector Pulse immediately following an Index Pulse defines the beginning of sector zero. At the time of that Sector Pulse, the Sector Count lines will present a zero value as the result of having loaded the Sector Number Counter with all zeros. Thereafter, the value will be incremented until the maximum count is achieved. The maximum count that will occur is N minus one, where N is the number of sector pulses.

Recall from the previous discussion that the lower disk is always sectored electronically in dual-disk machines. Recall also that the removable cartridge in either dual-disk or quad-disk machines may be sectored electronically. The exception to this is if the cartridge has an index-only notch, then it must be sectored electronically.

Electronic sectoring is selected by the Sectoring Selection Programming array installed in J125. When electronic sectoring is selected, the output of the electronics is connected to the Upper Sector Pulse Former, the Upper Sector Number Counter, and the Upper Count Control F/F.

NOTE

The Lower Sector Number Counter, Lower Count Control and Lower Sector Pulse Former are connected to the electronic sectoring electronics at all times since the lower disks are always sectored electronically.

Electronic sectoring requires that the drive generate pulses electronically for sectoring in lieu of the mechanical slots normally used for sectoring. Since the lower disk is sectored electronically regardless of the mechanical configuration, pulses must always be generated for sectoring the lower disk. These pulses are generated by counting down (with an electronic counter) the output of a high frequency oscillator. Because the sector pulses must be synchronous with the instantaneous speed of spindle rotation, it is necessary to phase lock this high frequency oscillator to the spindle.

The high-frequency oscillator is a voltage controlled oscillator (VCO) which is part of the Sector Phase Lock Loop. The function and purpose of the Phase Lock Loop is to phase-lock the voltage controlled oscillator frequency to the phase lock pulses obtained from the Phase Lock Ring through the Lower Time Demultiplexer. The sector phase lock loop is shown in zones 10-1G—8G on the schematic. The input to the Sector Phase Lock Loop is from U183 pin 13 (zone 11-2C), which is the phase lock pulse output from the Lower Time Demultiplexer. Recall that the phase lock pulses are separated from the lower index pulse by the Lower Time Demultiplexer.

It is necessary to count down the output of the high-frequency voltage controlled oscillator to obtain the desired number of pulses per revolution for sectoring. This is accomplished by the Upper and Lower Sector Countdown Counters shown in zones 12-4G and 12-4F, respectively. Also associated with these counters are the Upper and Lower Electronic Sector Programming arrays that are installed in J126 and J127 respectively. These programming arrays determine the particular number of sectors.

Since it is necessary to synchronize the countdown with the index for the respective disk, there is a synchronizer for each counter. These are used to synchronize the count with the index pulse. The index pulse is obtained from the respective time demultiplexer. In the case of the lower disk, the index notch on the Phase Lock Ring generates a pulse which is separated by the time multiplexer and is applied to the Lower Synchronizer. In the case of the upper disk, the index notch generates a pulse which is separated as necessary by the Upper Time Demultiplexer and applied to the Upper Synchronizer.

The output of the respective countdown counter is a pulse, which is the raw sector pulse, for use by the pulse formers and the Sector Number Counter when electronic sectoring is employed.

The Sector Phase Lock Loop is, in essence, an electronic servo loop designed to servo the voltage controlled oscillator frequency to phase lock that frequency to the pulse train derived from the demultiplexed phase lock ring notches.

The Sector Voltage Controlled Oscillator (Sector VCO), which consists of Q1, R43, R42, U209, C14, C15, C16 or C17, R41 and R46. C13 and C12, are used only to decouple the power supply voltages that are supplied to U209. The voltage controlled oscillator is an R-C oscillator with part of the resistive component comprised of Q1, which is made variable by the voltage applied to the gate of Q1. The output of the oscillator is derived from Q1 and directly coupled into a Schmitt trigger. The Schmitt trigger consists of one section of U268 with its threshold established by R48 and R49. The output of the VCO is at U268 pin 4. Thus, U268 converts the output of the oscillator into a digital signal that is suitable for use by the counters. In order to phase lock the VCO frequency to the phase locked pulses derived from the spindle, it is necessary to detect the phase difference between the Sector VCO and the phase lock pulses to produce a control voltage to servo the frequency of the Sector VCO to the proper value. This is accomplished using a Phase Comparator and Filter, shown in zones G7—G5 sheet 10.

The phase lock pulses are applied to the clock input of the Phase Lock F/F U129 (zone 10-7H). The Phase Lock F/F divides the frequency of the phase-lock pulse train by a factor of 2 and converts it into a square wave. This square wave is then applied to the Phase Comparator and Filter. Additionally, the Phase Lock F/F, Q output (LPLFF), is also fed to the Spindle Speed Control Electronics as previously described.

The other input to the Phase Comparator is the output of the VCO, suitably counted down. The countdown of the Sector VCO is accomplished by the Sector PLL Countdown Counter. The particular division ratio obtained with this countdown counter is determined by the programming which results in wiring the A, B, C, and D inputs to U106, U146 and U166 (zone 10-7,6,5E).

The output of the Sector PLL Countdown Counter is fed to the clock input of the Sector Countdown Divider F/F U129 (zone 10-7F), which converts the output of the Sector PLL Countdown Counter into a square wave. This square wave is the other input to the Phase Comparator and Filter. The Phase Comparator is comprised of U149 (zone 10-6G), R26, R27, R28, and R21.

The output of the Phase Comparator is filtered and applied to the input of the Sum-And-Difference Amplifier U209 (zone 10-5G). The filter is comprised of R32, R31, R23, R24, C5, R29, R23, R22, R30, and C6. The particular filter characteristics required are programmed by part of J123 depending upon the disk speed utilized in the particular drive.

R23, R24, R25, and R34 determine the characteristics and gain of the Sum-And-Difference Amplifier, U169. C9 and C8 decouple the power supply to U169. Adjustment of the PLL is accomplished by R42 (zone 10-3H). The combination of R41, CR5, and VR1 provide a bias to the Sector VCO.

The output of the Sum-And-Difference Amplifier, U169 pin 6, is the control voltage to control the frequency of the Sector VCO. It is filtered by R36 in conjunction with C11. This control voltage causes the Sector VCO frequency to become phase-locked to the pulse train derived from the Phase Lock Ring.

The output of the VCO through Q1 and the Schmitt trigger is the input to the Countdown Counter and the VCO divider flip-flop, U143 (sheet 11, zone 3B). The Divider F/F divides the frequency of the Sector VCO by a factor of 2 for use as an alternate input to the Countdown Counters depending upon the desired number of sectors. Whether the output of the VCO Divider F/F, or the output of the VCO directly is applied to the Sector Countdown Counter, is a function of the particular programming array installed in J125.

The Lower Sector Countdown Counter consists of U121, U161, and U181 (zone 12-5,4,3E). These are 4-bit binary synchronous counters that may be loaded with one of two different values obtained from the Lower Electronic Sector Programming array installed at J127. The value loaded is determined by the Lower Synchronizer Register and associated circuitry which generate the I and NI signals applied to the Lower Electronic Sector Programming array, pins 5 and 6, respectively. The Lower Sector Countdown Counter is clocked by the signal obtained from the Sectoring Selection Programming array which will be either the output of the VCO Divider F/F or the output of the Sector VCO directly.

When the Lower Sector Countdown Counter is counted from the value loaded until a carry-out occurs at U181 (zone 12-3E), a pulse will be output at U122 pin 4. This pulse train output has a frequency which corresponds to the number of desired sectors. This pulse train will be synchronized with the index by the Lower Synchronizer Register U182 (zone 12-7E) and the associated synchronizing circuitry. That circuitry consists of the Lower Synchronizer Register U182, U162-12, and U122-1, which edge detects the pulse obtained for the lower disk index by the Lower Time Demultiplexer, which outputs from U183 pin 10 (zone 11-2C).

The output of U122-1 (zone 12-6E) is applied to the Lower Electronic Sector Programming array for purposes of determining the value loaded into the Sector Countdown Counter.

As previously discussed, the output of U122 pin 4 (zone 12-2F) is the raw sector pulse which is utilized by the Sector Number Counter, Count Control, and the Sector Pulse Former.

5.6 MOTOR CONTROL PCBA

The following paragraphs describe the Motor Control PCBA installed in the D3000 Series Disk Drives. Refer to Schematic No. 103570 and Assembly No. 103571.

The Motor Control PCBA is approximately 101.6 mm (4 inches) square and is physically located on top of the power transformer. This PCBA is one of the subassemblies which comprise the Power Supply Chassis. The circuitry contained on the Motor Control PCBA performs a ground isolation function and provides the drive current necessary for controlling a triac, which, in turn, switches power to the drive motor. This PCBA is one of the functional elements in the spindle speed control.

Figure 5-8 illustrates the placement of the six molex connectors located on the face of the PCBA. These connectors are used to provide inputs to the circuit board consisting of the line voltage, the line voltage common, a reference voltage derived from a secondary winding on the main power transformer, and a trigger from the speed control circuitry on the Servo PCBA.

Additionally, the connectors and jumpers on the face of the Motor Control PCBA are used to provide an alterable interconnection scheme for selecting different connections to the motor capacitors and the drive motor depending upon the type of line voltage operation desired. Therefore, the connectors which connect to the Motor Control PCBA, plus the jumpers on the face of the board, provide a switchable junction box to allow alternation of the connections of the drive motor windings and the motor capacitors. This can be visualized by referring to the Power Supply Schematic, Drawing No. 103580.

Note that there are two classes of line voltage operation, i.e., 110v and 220v. When a particular drive is configured for operation on nominal line voltages between 95v and 125v, P403 is connected to J403 on the Motor Control PCBA and jumpers W1, W3, W4, and W5 are installed. P403 is the plug from the motor capacitors and P405, P406 are the plugs from the drive motor. For operation on nominal line voltages of 190v to 250v, P403 connects to J404, and jumpers W2 and W6 are installed. Nominal line voltage of 95v to 125v is defined as 110v operation classification; nominal line voltage of 190v to 250v is defined as 220v operation classification. Refer to Paragraph 4.8 for the functional details of 110v and 220v operation of the drive motor.

Other than the interconnection arrangement previously described, all circuitry on the Motor Control PCBA is dedicated to switching the triac and suppressing any transients that result from this switching. A dc power supply voltage is required to provide current to the gate of the triac and must be developed with respect to the line voltage common. This is a function which is performed by a special power supply made up of CR1, R8, and C1 (zone D6,7). The voltage is negative dc with respect to the ac common (pin 3 of J402). An ac signal of approximately 8v rms is provided to pin 5 of J402 from a separate secondary winding of the main transformer mounted on the power supply chassis. The voltage provided by this winding is rectified by CR1 and charges C1 to provide a relatively steady dc voltage; current limiting is provided by R8.

The trigger from the Servo PCBA is supplied to the Motor Control PCBA at J401 (zone E7). This trigger is the output of the Motor Speed Control circuitry on the Servo PCBA and is, in essence, a transistor switch closure to ground when the trigger is asserted.

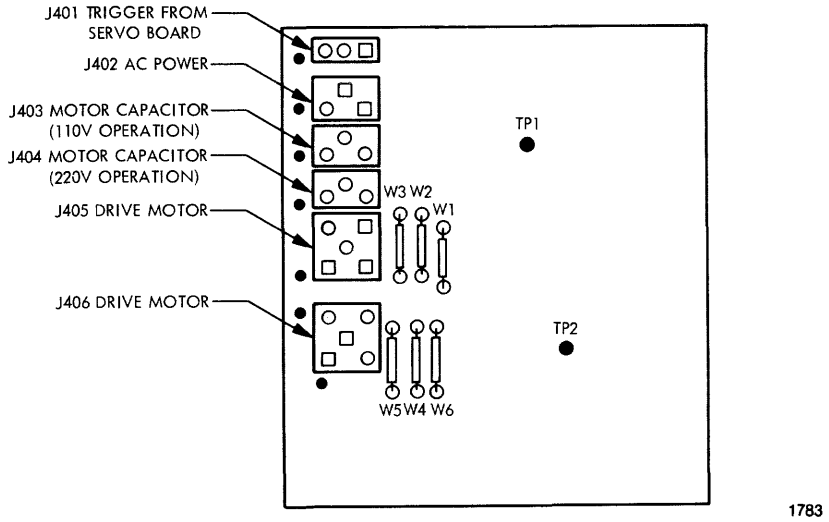

Figure 5-8. Motor Control PCBA Test Point and Connector Placement

When the transistor switch on the Servo PCBA is conducting and the trigger is asserted, current from the +5v supply flows through R1 (zone E7) and a Light Emitting Diode (LED), which is part of U1. U1 is an optical isolator consisting of a LED optically coupled to a phototransistor. When current passes through the LED, it causes the LED to emit light; this light is coupled to the phototransistor causing it to conduct. Conduction of the phototransistor in U1 causes a base current to flow in Q1 (zone E6) which, in turn, causes a base current in Q2. Q2 conducts and provides the current to triac SCR1 (zone E5). Gate current flowing in SCR1 results in the triac conducting current through the motor winding. Conversely, when the trigger signal is absent, there is no current flow through the LED in U1; therefore, the voltage across R2 causes Q1 to turn off and the voltge across R7 causes Q2 to turn off. Therefore, there is no current into the gate of the triac and conduction will stop as soon as the current through the triac passes below the holding current value, a characteristic of the device.

Resistors R3, R6, R4, and R5 provide the proper values of current in the collectors of transistors Q1 and Q2, and into the gate of the triac. R9 ensures that the gate current is sufficiently low that the triac will stop conducting. C2 and R10 (zone D5) provide a network for compensating for the fact that the drive motor is an inductive load. This means that at the time the current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with such an inductive load, the rate of rise in voltage (dc/dt) must be limited by a series R-C network across the triac. The capacitor will then limit the rate of change of voltage across the triac. The resistor is necessary to limit the surge of current from the capacitor when the triac fires and to damp the resonance of the capacitor with the load and circuit inductance.

5.7 TEMPERATURE COMPENSATION PCBA

5.7.1 TEMPERATURE COMPENSATION CIRCUITRY

The Temperature Compensation PCBA is located adjacent to the Read/Write PCBA and is approximately 203.2 mm (8 inches) long by 101.6 mm (4 inches) high. The Temperature Compensation PCBA operates in conjunction with two externally mounted thermistors to provide thermal compensation. Control circuitry for the Emergency Unload mode is also included in this PCBA to protect the heads and media from possible damage during an emergency unload condition. Refer to Schematic No. 108175 and Assembly No. 108176.

The switched current resistors (R24, R26, R28) receive their commands from the Current Address Counter on the Logic PCBA via J503 (zone D-C8). The three most significant bits are employed to provide off-track compensation and are comprised of LCA E1, LCA 71, and LCA 61 (zone C,D8), in order of declining bit weight.

Figure 5-9 illustrates the placement of the five connectors on the Temperature Compensation PCBA. These connectors provide power to the PCBA in addition to providing input and output signal paths between this PCBA and the Logic PCBA, the Servo PCBA, and the two externally mounted thermistors.

There are two temperature sensing thermistors, one for the removable cartridge, the other for the fixed disk(s) ambient surface temperature. On top load drives, RT2 is mounted on the rear right side of the adapter bowl and protrudes through a port into the interior of the bowl. On front load drives, RT2 is mounted so that it extends through the rear flapped opening of the cartridge and extends above the surface of the disk when the cartridge is fully seated in position.

The fixed disk(s) sensor, RT1, for both top and front load models, is mounted on the positioner base as part of the head ramp. The thermistor extends into the fixed disk area immediately adjacent to the heads and is positioned above the outer surface of the disk.

RT1 is connected to the input of amplifier U1 (zone F7) via pin 1 of J505. RT2 is connected to the input of amplifier U3 via pin 6 of J505. The outputs of U1 and U3 are applied simultaneously to pins 2 and 6 of U7.

The output of U7 pin 7 (zone F5) drives a multiplexer digital-to-analog converter which consists of three FETs in U6 pins 3, 11, and 14 (zone G,E6). The fourth FET (at U6 pin 6) is driven by the output of U7 pin 1 when the Transient Compensation signal (NLTPCG) is active.

The NLTPCG signal from the Transient Compensation circuitry (sheet 3, zone D1) drives FET U6 pin 6 (zone D6) whose output is applied to the summing junction of U4 pin 6 along with three outputs of FET U6 at pins 1, 9 and 16. The output of the summing amplifier is the Servo Compensation signal which is sent to the Servo PCBA via J504 pin 2 (zone C3).

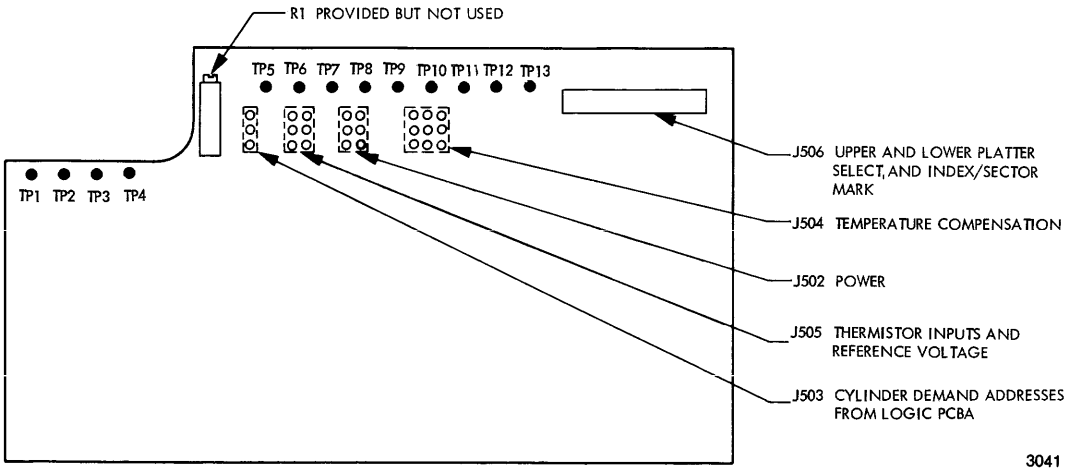

Figure 5-9. Temperature Compensation PCBA Test Point and Connector Placement

Sheet 4 shows the Emergency Unload circuitry which, although physically located on the Temperature Compensation PCBA, is electrically associated with the Servo PCBA.

The voltage drop across R164 (sheet 3, zone F5) on the Servo PCBA (drawing 108130) appears on J504 pin 4 which is the input to U16 (zone F5). This input is compared with the voltage divider network consisting of R56 and R55.

The output of U16 drives the base of Q1 which uses VR5 in its emitter circuit to limit the voltage at the base of Q2. When Q2 is on, current is applied to the positioner coil via J504 pin 1, and Relay K1 on the Servo PCBA.

Addressing of the removable cartridge is detected in U12 from the Lower Platter Select (NLLPSG) and Upper Platter Select (NLUPSG) signals. Immediately after the removable cartridge is either selected or deselected, U13 (sheet 3, zone F5) serves a a *one shot* to mask index and sector signals and also read signals (for soft-sectored formats) for approximately 10 msec. This allows the positioner to recover from the position transient caused by the change in the temperature compensation signals.

The Delayed Index And Sensor (NLDISG) signal (sheet 3, zone F1) is sent to the Logic PCBA to mask the Index and Sector Count signals.

The Temperature Compensation Read Enable (NTTREG) signal (sheet 3, zone E1) is sent to the Read/Write PCBA to disable the Read Enable circuitry.

In addition to the Temperature Compensation electronics, the Temperature Compensation PCBA contains a time delay circuit. This circuit consists of a monolithic timer, U8, a 4-bit binary counter, U10, and associated components. A low on U8 pin 4 (zone C4) resets the timer. The timer will *free run,* generating one pulse per 2 minutes as determined by R52, R53, and C7. The binary counter is clocked by each pulse and counts eight of these pulses before an output is delivered at J506 pin 10. This 16-minute timer circuit allows the internal temperature of the drive to stabilize before disabling the differential temperature compensation and the index and sector *mask* of U13. The timer circuit operates after the RUN indicator illuminates on the drive control panel.

Jumper W2 (zone C4) is used for test purposes only.

5.7.2 EMERGENCY UNLOAD CONTROL CIRCUITRY

During an unload condition, the sudden acceleration of the positioner assembly sometimes causes the heads to torque and thereby gouge the media. Sheet 4 of the Temperature Compensation schematic, 108175, shows the circuitry that controls the speed of the positioner during the unload mode.

Controlling positioner speed means applying sufficient current to the voice coil to limit the speed of the positioner as it reaches the unload ramp and then to apply a higher level of current to the voice coil to allow the heads to fully unload.

During an unload condition, positioner current is sensed at U16-3 via the line on J504 pin 4 (zone F7). A current threshold is established by the divider network, R55 and R56. When the positioner current is below threshold, U16-6 will be positive, Q1 will turn on and VR5 will conduct. Q2 will open and the limit current will be transmitted to the emergency unload driver via J504 pin 1 (zone E2).

If the positioner current reaches the threshold current, U1 will be negative at U1-6, VR5 will cease to conduct and R59 will bias Q4 to saturation and establish the high limit of the current to the emergency unload driver via J504 pin 1 (zone E2).

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation of components and circuits for reference.

6.2 FUSE REPLACEMENT

The four fuses which protect the disk drive electrical components are located under the left rear corner of the base casting. Fuse identification and types are listed in Table 6-1.

6.3 SCHEDULED MAINTENANCE

The disk drive is designed to operate with a minimum of maintenance and adjustments. Part replacement is planned to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of hand tools required to service the drive is given in Paragraph 6.30.

6.3.1 MAINTENANCE PHILOSOPHY

To ensure reliable operation of the disk drive at its optimum design potential a scheduled preventive maintenance program is recommended.

The objective of any maintenance program is to provide maximum machine readiness with a minimum of downtime. To provide this type of reliability, it is necessary to perform preventive maintenance at the specified intervals. This schedule is given in Table 6-2.

In general, it is not necessary to alter any adjustment on equipment that is performing in a satisfactory manner.

6.3.2 GENERAL MAINTENANCE

Perform a visual inspection of the disk drive for loose electrical connections, dirt, cracks, binding, excessive wear, and loose hardware while conducting any maintenance function.

Cleanliness is essential for proper operation. Minute particles of dirt trapped between the flying heads and the disk causes the disk surface to become scored. This condition may result in an unusable disk or head damage, or both.

Table 6-1

Fuse Requirements

	Function	Type
F1	Line Fuse	10 Amp, 3AG, SB, 125v and below 5 Amp, 3AG, SB, 190v and above
F2	+ 25v dc (Unregulated)	10 Amp, 3AG, FB
F3	– 25v dc (Unregulated)	10 Amp, 3AG, FB
F4	+ 10v dc (Unregulated)	10 Amp, 3AG, FB

Table 6-2
Preventive Maintenance Schedule

Interval*	Item	Paragraph Reference
1000 Hours**	Clean Heads and Disks	6.4.1, 6.4.2
1000 Hours**	Clean Pre-filter	6.26.1
2000 Hours	Check Belt for Wear and Proper Tension	6.19
2000 Hours or 6 Months**	Replace Air Filter	6.26
2000 Hours	Lubricate Catch Assembly Ball Studs in Bezel	6.17.2
2000 Hours or 6 Months	Clean Spindle Magnetic Chuck and Cone	6.4.4
4000 Hours or 12 Months	Clean Positioner	6.4.5
1000 Hours or 3 Months, and when Unit is moved	Check CE Alignment	6.14
4000 Hours or 12 Months	Clean Base Casting and Inspect Machine	6.4.6
24,000 Hours	Replace Drive Motor, Replace Spindle	6.29

*The listed preventive maintenance frequency is based on operating hours. Typically, about 200 hours operating time per month will be accumulated for the average installation. When operating hours are less than the specified time interval, perform the maintenance on the basis of time interval only if stated in the table above.

**More frequent servicing may be required if operating in an abnormally dirty environment or if a high rate of cartridge loading is encountered.

Accumulated foreign matter can also cause the heads to fly at an excessive distance from the disk surface. This will severely impair the retrieval of data and result in writing errors.

6.3.3 GENERAL PRECAUTIONS

Any work performed on the drive should be accomplished with the power off and preferably, with the power cord disconnected from the power line unless otherwise necessary.

CAUTION

THE DISK DRIVE POSITIONER ASSEMBLY CONTAINS A PERMANENT MAGNET; KEEP ALL ITEMS MADE OF FERROUS MATERIALS (TOOLS, WRIST WATCHES, RINGS, ETC.) AWAY FROM THIS AREA.

WARNING

AVOID PLACING HANDS IN VICINITY OF CARTRIDGE OR VOICE COIL WHEN DRIVE IS OPERATING. AN EMERGENCY UNLOAD OF MAGNETIC HEADS COULD CAUSE SERIOUS INJURY TO MAINTENANCE OR OPERATING PERSONNEL.

CAUTION

CIGARETTE SMOKE AND TOBACCO ASHES ARE A COMMON CAUSE OF PROBLEMS INDUCED DURING SERVICING. AVOID SMOKING WHEN SERVICING THE DRIVE WITH THE COVER OFF OR AIR FILTER REMOVED.

NOTE

Avoid operating the drive with top cover removed unless maintenance cannot be performed otherwise. If the drive must be operated with dust cover off, use a work cartridge.

6.4 CLEANING THE DISK DRIVE

The disk drive requires cleaning in these major areas: heads, disks, spindle, positioner, base casting, dust cover, and filters. Details are given in Paragraphs 6.4.1 through 6.4.5, and 6.26.

The following cleaning materials are recommended for use when cleaning the disk drive.

(1) Lint-free wipes such as Absorband TX404* or Kaydry Disposable Wipes 34720**.

(2) Isopropyl alcohol, 91 percent by volume.

CAUTION

DO NOT USE ISOPROPYL ALCOHOL, OR ITS EQUIVALENT, ON ANY PART OF THE DRIVE OR ITS CARTRIDGE UNLESS SPECIFICALLY INSTRUCTED TO DO SO IN THIS MANUAL.

CAUTION

USE ONLY 91 PERCENT ISOPROPYL ALCOHOL TO CLEAN DISK AND HEADS. USE OF ANY OTHER TYPE OF CLEANER OR SOLVENT, SUCH AS CARBON TETRACHLORIDE OR TRICHLORETHYLENE MAY RESULT IN DAMAGE TO THE DISKS OR HEADS. DO NOT USE CONTAMINATED ALCOHOL WHICH COULD CONTAIN ANY FORM OF RESIDUE.

WARNING

THE 91 PERCENT ISOPROPYL ALCOHOL SOLUTION IS A FLAMMABLE LIQUID. KEEP THE BOTTLE CONTAINING ISOPROPYL ALCOHOL STORED IN A SEALED METAL CONTAINER EXCEPT WHEN IN USE.

WARNING

WHEN SHIPPING 91 PERCENT ISOPROPYL ALCOHOL, COMPLY WITH THE APPROPRIATE REGULATIONS FOR SHIPMENT OF FLAMMABLE LIQUIDS.

(3) Two disk cleaning wands, Texwipe Part No. TX800*, PCC PD Part No. 623-0002.

(4) Cotton swabs such as Q-Tips***.

(5) Masking tape ½-inch or ¾-inch wide.

6.4.1 CLEANING THE HEADS

Remove the cover from the drive and raise the Logic PCBA to the extended position. Instructions for removal of the drive cover are contained in Paragraph 2.2.

NOTE

The Read/Write PCBA should be removed prior to performing the head cleaning operation.

Use a dental mirror and a suitable light source (such as a penlight) to inspect each head before and after cleaning. It is important that all debris be removed from the head.

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*Available from Texwipe Co., Hillsdale, New Jersey 07642

**Available from Kimberly-Clark

***Chesebrough-Ponds, Inc., Greenwich, CT 06830

Examples of slider defects and head contamination are shown in Figures 6-1 and 6-2 with explanations for each example. If the contamination shown in Figure 6-1 cannot be removed with alcohol without scratching slider surface, affected heads must be replaced.

Any physical damage to the gimbal spring, load spring, slider, or the load pin will necessitate replacement of the head assembly.

Use the following procedure for cleaning each head.

(1) Remove a cleaning Q-tip from its container, without touching the cotton swab.

(2) Saturate the Q-tip cotton swab with 91 percent isopropyl alcohol.

NOTE

Do not dip the swab into the isopropyl alcohol, but pour it over the swab so as not to contaminate the alcohol.

CAUTION

DO NOT TOUCH THE FACE OF THE MAGNETIC HEADS WITH YOUR FINGERS. ACIDS EMITTED FROM THE SKIN CAN CAUSE PERMANENT DAMAGE TO THE HEAD. DO NOT BLOW ON THE HEADS AS MOISTURE WILL CONTAMINATE THE HEADS.

(3) Carefully clean the slider surface and edges of the heads.

NOTE

To facilitate cleaning the heads, the positioner may be moved forward from its fully retracted position about ½ to ¾-inch. This will cause the head pairs to separate, thus allowing more space between the heads.

(4) Clean the two bleed holes in the head by rotating the cotton swab at each hole opening (this will clear any loose oxide or contamination that may be trapped at the edge of the holes) — make sure you do this from the slider face of the head — not from the back.

(5) Wipe the slider face dry using a second cotton swab before the alcohol has evaporated.

(6) Inspect each head after all have been cleaned. Repeat the cleaning process if necessary.

6.4.2 INSPECTING AND CLEANING THE FIXED DISK

Remove the cover from the drive and raise the Logic PCBA to the extended position. Instructions for removal of the drive cover are contained in Paragraph 2.2. Also remove the disk cartridge, if necessary.

Use a dental mirror and a suitable light source (such as a penlight) to inspect each disk surface before and after cleaning. It is important that all debris be removed from the disk surface.

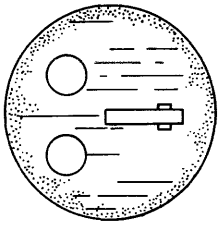
Use the following procedure for cleaning each disk surface.

(1) For front load models only, gain access to the lower fixed disk(s) by removing the access cover plate on the side of the lower disk cover.

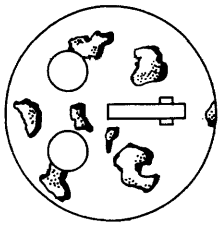
(2) Prepare two cleaning wands as follows.

- Insert a lint-free pad* into the barbed slot of wand.

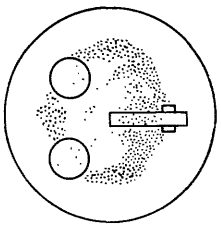
*Some pads, such as Texpads (from the Texwipe Co., Hillsdale, NJ 07642) come packaged in a sealed container already saturated with 90% isopropyl alcohol.



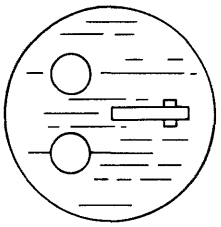
SLIGHT OXIDE ACCUMULATION
ON SLIDER SURFACE



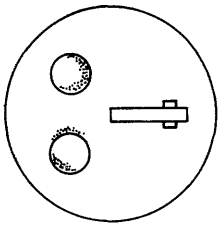
ALCOHOL RESIDUE DRIED ON
SLIDER SURFACE



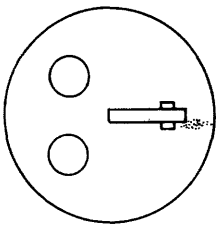
FINGERPRINTS ON SLIDER SURFACE



LIGHT SCRATCHES ON SLIDER
SURFACE WITHOUT OXIDE
ACCUMULATION



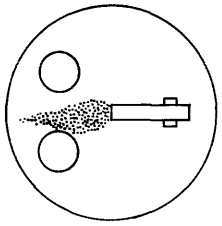
EXCESSIVE LOOSE OXIDE PARTICLE
BUILD UP IN BLEED HOLES



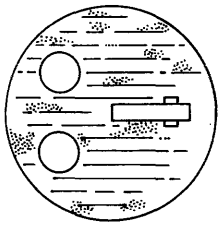
MINOR OXIDE STREAK

DIRECTION OF DISK ROTATION

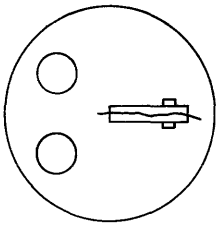
Figure 6-1. Slider Defects and Head Contamination which Require Cleaning Action



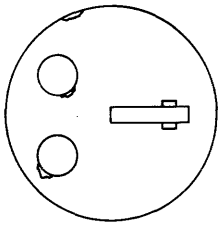
SLIDER SURFACE HAS A HEAVY OXIDE ACCUMULATION IN POLE TIP AREA WHICH CANNOT BE REMOVED



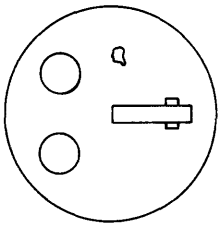
SLIDER SURFACE HAS DEEP SCRATCHES WITH OXIDE ACCUMULATION



DEEP SCRATCH OR SCRATCHES THRU CORE FACE OR POLE TIPS



CHIPPED EDGE OF SLIDER SURFACE PERIPHERY OR CHIPS AT EDGE OF BLEED HOLES



LARGE PIT OR VOID IN SLIDER SURFACE

DIRECTION OF DISK ROTATION

Figure 6-2. Slider Defects and Head Contamination which Require Head Replacement

- It is important to rotate the wand counterclockwise, thereby wrapping the pad completely around the wand. Take care not to contaminate the pad.

(3) Saturate the pad with 91 percent isopropyl alcohol.

NOTE

Do not dip the lint-free pad into the alcohol but pour the liquid over the pad so as not to contaminate the alcohol.

(4) While rotating the spindle chuck CCW, insert the cleaning wand parallel to the disk far enough to cover the innermost track. The lint-free pad should lightly contact the surface of the disk and should point directly at its center.

(5) After the disk surface has been subjected to the alcohol treatment, and with the disk still spinning, quickly withdraw the wand with a steady motion lifting it gently from the disk surface.

(6) Using the procedure in Step (4), wipe the disk surface dry with the second cleaning wand. Remember that you are gently drying the disk — not polishing it. This operation must be done before the alcohol evaporates to prevent puddles and solvent spots from forming on the disk surface.

CAUTION

EXCESSIVE WAND PRESSURE CAN CAUSE DRY FRICTION HEAT WHICH CAN DESTROY RECORDED DATA.

CAUTION

DO NOT ALLOW ALCOHOL TO DRY ON DISK SURFACE. DO NOT TOUCH DISK WITH FINGERS. ACIDS EMITTED FROM SKIN CAN CAUSE PERMANENT DAMAGE TO DISK SURFACE.

(7) As the disk continues to spin, withdraw the cleaning wand with a steady motion, lifting it gently from the disk surface.

(8) Inspect each disk surface after cleaning; repeat the cleaning process if necessary.

(9) Reinstall the plate and hardware removed in Step (1).

6.4.3 REMOVABLE DISK CARTRIDGE CLEANING

The 2315 and 5440-type removable disk cartridges must be cleaned periodically. PCC PD recommends the use of a mechanical disk cartridge cleaner; there are several of these cleaners available on the commercial market. Additionally, there may be media cleaning and refurbishment services available locally.

6.4.4 CLEANING THE SPINDLE

Wipe the spindle cone and the magnetic chuck with a dry lint-free wiper. Metal particles that have become attracted to the magnetic chuck may be removed using masking tape.

6.4.5 CLEANING THE POSITIONER

The positioner shaft and scale can be cleaned with a lint-free wiper slightly moistened with isopropyl alcohol. Carefully wipe the surfaces to remove any accumulated matter.

CAUTION

DO NOT WET THE SHAFT, SCALE, OR WIPER WITH AN EXCESSIVE AMOUNT OF ISOPROPYL ALCOHOL AS IT COULD SEEP INTO CARRIAGE BEARINGS CAUSING BREAKDOWN OF THE BEARING LUBRICANT.

CAUTION

DO NOT DISASSEMBLE POSITIONER FOR CLEANING.

6.4.6 CLEANING THE BASE CASTING, DUST COVER AND FILTERS

The base casting and associated areas, including the dust cover, should be cleaned using a vacuum cleaner. (The procedure for cleaning the filters is described in Paragraph 6.26.)

CAUTION

DO NOT USE COMPRESSED AIR AS THIS WILL BLOW DIRT INTO THE DISK CHAMBERS AND AIR SYSTEM.

6.5 PART REPLACEMENT ADJUSTMENTS

Table 6-3 defines the adjustments that may be necessary when a part is replaced in the disk drive; details are given in Paragraphs 6.6 and 6.7.

6.6 ELECTRICAL ADJUSTMENTS

In addition to the tools listed in Paragraph 6.30, the following equipment (or equivalent) will be required for electrical adjustments.

(1) Oscilloscope, dual trace, having at least a 50 MHz bandwidth. Vertical and horizontal sensitivity specified to ±3 percent accuracy.

(2) Three calibrated X10 test probes with ground clips.

(3) One X1 test probe with ground clip.

(4) Digital Volt Meter, Fairchild 7050 (±0.1 percent specified accuracy) or equivalent, with test leads.

(5) Disk Exerciser and 6-foot extender cable.

(6) Counter Timer, Monsanto Model 100B (±0.1 percent specified accuracy) or equivalent.

(7) Jumper, not to exceed 6 inches in length, with alligator clips on each end.

(8) Reticle Adjustment Tool, PCC PD Part No. 103659.

(9) Emergency Unload Bypass Jumper Plug, PCC PD Part No. 103608.

(10) Voice Coil Polarity Tester, PCC PD Part No. 103607.

(11) Circumferential Adjustment Tool, PCC PD Part No. 103609, or equivalent (required for front load models only).

(12) Head Installation Tool, PCC PD Part No. 108231-01.

6.6.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.6. When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustments should be made in accordance with the relevant procedure.

NOTE

Some adjustments may require corresponding adjustments in other parameters; ensure these adjustments are made as specified in the individual procedures. The +5v, −5v, +12v, and −12v voltages must be checked prior to attempting any electrical adjustments.

Table 6-3
Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	Time Required (Hrs)	Paragraph Reference
Spindle	Sector PLL Adjustment, Circumference Alignment, Radial Alignment	2:00	6.11, 6.14, 6.14.5 or 6.14.7
Servo PCBA	Servo, Power Supplies, and Spindle Speed Control	1:00	6.6.2, 6.6.3, 6.7, 6.9
Position Transducer Assy	Servo Readjustment, CE Alignment	1:00	6.7, 6.9, 6.14
Logic PCBA	Sector PLL Adjustment .	0:45	6.11
Read/Write PCBA	RPN Pulsewidth Adj., One-shot Adj., Read Asymmetry Adjustment	1:00	6.12
Magnetic Transducer, Upper	Magnetic Transducer Gap, CE	0:35	6.18.1, 6.14
Magnetic Transducer, Lower	Magnetic Transducer Gap	0:35	6.18.2 or 6.18.3
Photoelectric Sensor, Upper (Front Load Only)	Circumferential Alignment	0:30	6.14
Cartridge Interlock Switch	Interlock Adjustment	0:30	6.15, 6.16
Cartridge Interlock Solenoid	Solenoid and Interlock Adjustment	0:30	6.15, 6.16
Head	CE Alignment*, Data Reliability	1:00	6.14
Fixed Disk	Check Data Reliability	1:00	—
Power Supply	Power Supply Adjustment	1:00	6.6.2
Bezel Assembly (Front Load Only)	Solenoid and Interlock Adjustment	0:30	6.15

*Applies to removable media heads only.

When adjustments are made, the value set should be the exact value specified, to the best of the operator's ability.

CAUTION

PRIMARY POWER SHOULD BE REMOVED FROM THE DRIVE WHEN ACCESS IS REQUIRED EXCEPT IN CASES OF ELECTRICAL TESTING AND ADJUSTMENTS.

Allowable line voltage variation is ± 10 percent of nominal. See Figure 4-14 for transformer primary connections. Allowable line frequency variations are:

- ☐ 50 Hz line
  - 48 Hz minimum
  - 52 Hz maximum
- ☐ 60 Hz line
  - 58 Hz minimum
  - 62 Hz maximum

6.6.2 12V AND 5V REGULATORS

The 12v and 5v regulator circuitry is located on the Servo PCBA. The 12v sources are established by 12v regulators and cannot be adjusted. The + 5v source is adjustable by means of potentiometer R30 on the Servo PCBA. However, the – 5v source is established by the – 5v regulator and is not adjustable.

NOTE

When a new Servo PCBA is installed, or any change is made to the power supply circuitry, do not perform the following tests, but go directly to the adjustment procedure, Paragraph 6.6.2.4.

6.6.2.1 Test Configuration

(1) Connect the drive to appropriate ac power source and set ON/OFF switch to the ON position.

(2) All test points mentioned in Paragraphs 6.6 through 6.11 are located on the Servo PCBA unless otherwise noted.

6.6.2.2 Test Procedure, 12v

(1) Using a DVM (Fairchild 7050 or equivalent), connect the positive test lead to TP20 and the common test lead to TP26.

(2) Acceptable limits (+ 12v)

- + 12.8v maximum
- + 11.2v minimum

(3) Change the positive DVM test lead connection to TP17.

(4) Acceptable limits (– 12v)

- – 12.8v maximum
- – 11.2v minimum

NOTE

In the event the readings obtained in Steps (2) and (4) fall outside the acceptable limits, remove power from the drive and disconnect isolation plugs P209, P210, and P211 from the Servo PCBA. Apply power to the drive and proceed to troubleshoot using schematic contained in Section VII; the measurements will now be made with P209, P210, and P211 removed.

6.6.2.3 Test Procedure, 5v

(1) Establish test configuration described in Paragraph 6.6.2.1.

(2) Verify that isolation plugs P209, P210, and P211 are installed.

(3) Using a DVM, connect the positive test lead to TP30 and the common test lead to TP15, on the Logic PCBA

(4) Acceptable limits (+ 5v) at TP30

- + 5.10v maximum
- + 4.90v minimum

(5) Change the positive DVM test lead connection to TP24 on the Servo PCBA.

(6) Acceptable limits (+ 5v) at TP24

- + 5.25v maximum
- + 4.75v minimum

(7) Change the positive DVM test lead connection to TP7 on the Servo PCBA.

(8) Acceptable limits (– 5v)
- – 5.30v maximum
- – 4.70v minimum

6.6.2.4 Adjustment Procedure

When the acceptable limits are exceeded or a new Servo PCBA is installed, the following adjustments are performed.

(1) Remove power from the drive and remove isolation plugs P209, P210, and P211 from the Servo PCBA.
(2) Apply power to the drive.
(3) Connect positive test lead of the DVM to TP24 and the common test lead to TP26, both on the Servo PCBA
(4) Adjust potentiometer R30 to + 5v as observed at TP24.
(5) Remove power from the drive and replace isolation plugs P209, P210, and P211.
(6) Apply power to the drive and recheck the + 12v and – 12v measurements (see Paragraph 6.6.2.2).
(7) Perform recheck of + 5v and – 5v power supply under load, i.e., jumper plugs P209, P210, and P211 re-installed.
   - ☐ Acceptable limits at TP24 on the Servo PCBA
     - + 5.25v maximum
     - + 4.75v minimum
   - ☐ Acceptable limits at TP7 on the Servo PCBA
     - – 5.30v maximum
     - – 4.70v minimum
(8) If the limits established in Step (7) are exceeded, readjust R30 to obtain + 5v at TP30 on the Logic PCBA. Since no adjustment can be made to the – 5v supply, remove power from the drive and disconnect isolation plugs P209, P210, and P211. Apply power to the drive and proceed to troubleshoot using the schematic contained in Section VII; the – 5v measurements will be made with P209, P210, and P211 removed.

6.6.2.5 Related Adjustments

When adjustment is made to the + 5v supply, tests and/or adjustments are required in the AC Motor Speed Control (Paragraph 6.6.3) and Static Positioner (Paragraph 6.8).

6.6.3 AC MOTOR SPEED CONTROL

The speed control adjustment for the ac drive motor is made to establish the correct spindle speed (1500 or 2400 rpm) within a ± 1 percent tolerance.

NOTE

The + 5v Regulator voltage must be checked and adjusted prior to adjusting the AC Motor Speed Control.

6.6.3.1 Test Configuration

(1) Remove power from the drive.
(2) Connect oscilloscope Channel 1 probe to TP2.
(3) Connect the ground clip of the oscilloscope probe to TP26.
(4) Set oscilloscope as follows.
   - Voltage sensitivity to 2v per division.
   - Select dc input mode.

- Sweep rate to 0.1 msec per division.
- Set to normal trigger mode.
- Use internal sync and set to trigger on negative slope.

6.6.3.2 Test Procedure

(1) Establish test configuration described in Paragraph 6.6.3.1.

(2) Select Channel 1 on the oscilloscope.

(3) Apply power to the drive.

6.6.3.3 Adjustment Procedure

(1) Establish test configuration described in Paragraph 6.6.3.1.

(2) Observing the waveform displayed on Channel 1 (TP2), adjust potentiometer R201 so that the hysteresis effect occurs between 0.20 msec and 0.70 msec as shown in Figure 6-3. Ensure the oscilloscope is still synced on the positive-going edge of the pulse. The hysteresis effect should be centered 0.45 msec from the positive-going sync pulse. Readjustment of R201 may be necessary to center the hysteresis effect at 0.45 msec.

(3) Remove power from the drive.

6.7 POSITIONER SERVO CALIBRATION

Paragraphs 6.8 and 6.9 describe the test configurations, test procedures, and adjustment procedures relevant to both static and dynamic operation of the D3000 Positioner Servo. It is important to note that if static positioner adjustments are performed, the dynamic positioner adjustments must also be performed.

To ensure accurate calibration of the positioner, the preliminary tests and adjustments described in Paragraph 6.7.1 must be performed prior to calibration of the positioner.

NOTE

The only ground reference test point to be used for measurement purposes is TP26. All test points referred to are located on the Servo PCBA unless otherwise noted.

6.7.1 POSITIONER PREPARATION FOR STATIC TESTS

The following functions are required to prepare the positioner for calibration.

(1) Remove power from the drive.

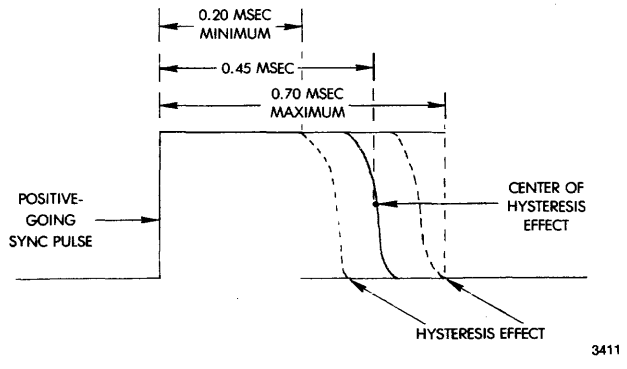


Figure 6-3. AC Motor Speed Control Signal Pulsewidth

(2) Disconnect connector P205 from the Servo PCBA.

WARNING

TO PREVENT INJURY TO SERVICE ENGINEER DUE TO INADVERTENT ACTIVATION OF POSITIONER DRIVE, CONNECTOR P205 MUST BE REMOVED FROM SERVO PCBA PRIOR TO ANY SERVO TESTS OR ADJUSTMENTS.

(3) Install Emergency Unload Bypass Jumper plug at connector J128 on Logic PCBA.

(4) Apply power to the drive. Observe that the SAFE indicator is illuminated, and that the bulb in the lamp/lens assembly (see Figure 7-7 and Table 7-7) is illuminated.

(5) Insert a disk cartridge into the drive.

(6) Measure +12.0 ±0.8v between TP20 and TP26.

(7) Measure −12.0 ±0.8v between TP17 and TP26.

(8) Measure regulated +5.0v ±0.25v between TP24 and TP26.

(9) Measure regulated −5.0v ±0.30v between TP7 and TP26.

(10) Voltages in Steps (6) through (9) must fall within the limits specified. In the case where voltages fall outside these limits, perform the test and adjustment procedures described in Paragraph 6.6.2.

(11) Manually move the positioner carriage back and forth and check that the reticle-to-scale gap across the full length of the scale is 0.127 ±0.025 mm (0.005 ±0.001 inch). A mylar shim (Pertec Part No. 104476-02) can be used for this measurement. The SAFE indicator will extinguish when the shim is in place between the reticle and scale. Do not load heads onto the disk at this time. If scale-to-reticle spacing is within tolerance, continue with Step (16).

NOTE

The Read/Write PCBA may be removed, if power is OFF, to facilitate access to the scale. Perform Steps (12) through (14) only if gap is not within tolerance.

(12) Loosen the horizontal hex-head screw at the base of the receiver post. This will loosen the receiver post and allow it to be raised and lowered when the Allen-head screw located inside the hollow of the receiver post is rotated.

(13) Position the receiver post so that the reticle-to-scale gap is within 0.127 ±0.025 mm (0.005 ±0.001 inch).

(14) Partially tighten the horizontal Allen-head screws loosened in Step (12).

(15) Withdraw the mylar shim to the point where the SAFE light becomes illuminated. The shim can be left in this partially withdrawn position.

(16) Depress and release the RUN/STOP switch. Manually advance the carriage about one inch from its fully retracted position. The drive will come up to speed and after 2 minutes the READY indicator will be illuminated.

(17) Manually load the head onto the disk and check the reticle-to-scale gap, with the mylar shim, as the positioner carriage is manually moved through its full forward and return strokes.

NOTE

Perform Steps (18) through (20) only if the reticle-to-scale gap throughout the length of the scale is not approximately 0.005-inch when using the mylar shim.

(18) Loosen three Allen-head screws that hold the scale to the side of the carriage. The scale will pivot slightly around its locating pin. Position the angle of the scale so that the reticle-to-scale gap remains 0.127 ±0.025 mm (0.005 ±0.001 inch) as the positioner carriage travels through its full forward and return strokes.

(19) Partially tighten the Allen-head screws.

(20) Remove the mylar shim.

NOTE

The foregoing reticle-to-scale gap adjustments are preliminary. Additional adjustments will be required during static positioner adjustment (Paragraph 6.8).

6.7.1.1 Initial Potentiometer Settings, Servo PCBA

The following procedure defines the initial setting of potentiometers located on the Servo PCBA. It is important to note that the initial potentiometer settings are required only when the Servo PCBA, Positioner, or Position Transducer have been replaced, or when repairs have been made (parts replaced) in the 12v power supplies or the Positioner Servo circuit.

(1) Velocity Feedback Potentiometer. Rotate potentiometer R136 fully CCW, then adjust 7 turns in the CW direction.

(2) Current Feedback Potentiometer. Adjust potentiometer R163 to the center of its range, i.e., approximately 10 turns from full CCW or CW position.

(3) X + 0 Offset Potentiometer. Adjust potentiometer R57 to the center of its range, i.e., approximately 10 turns from full CCW or CW position.

(4) Velocity Offset Potentiometer. Adjust potentiometer R145 to the center of its range, i.e., approximately 10 turns from full CCW or CW position.

6.8 STATIC POSITIONER ADJUSTMENTS

The following static measurements and adjustments are required to check the integrity of the position transducer signals (amplitude and polarity), and the voice-coil polarity. The test and adjustment procedures given in Paragraphs 6.8.1 through 6.8.8 should be performed in the order presented.

NOTE

The +5v Regulator voltage must be checked and adjusted prior to making Static Positioner adjustments.

6.8.1 X + 0 GAIN AND BALANCE

6.8.1.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.1, Steps (1)—(5), and (16).

(2) Remove J215 from the Servo PCBA.

(3) Set oscilloscope Channel 1 sensitivity to 2v per division.

(4) Connect oscilloscope Channel 1 X10 probe to TP21. Connect ground lead to TP26.

(5) Set oscilloscope horizontal sweep rate to 2 msec per division.

(6) Set oscilloscope trigger control to Line and Auto.

(7) Manually load the heads onto the disk.

NOTE

A ground reference sweep trace is obtained by centering the trace on a particular graticule line with vertical input mode switch of oscilloscope set to ground position.

6.8.1.2 Test Procedure

(1) Manually move the positioner carriage slowly, and at a constant rate, back and forth through its full stroke. Do not unload the heads from the disk.

(2) Monitor TP21 on oscilloscope Channel 1 and observe the Position Reference (X + 0) waveform shown in Figure 6-4 as the positioner is being moved. The peak-to-peak voltage observed throughout the full stroke of the positioner must fall within the acceptable limits listed in Step (3) and balanced about ground within ± 0.25v. If the acceptable limits are exceeded, perform the adjustment procedures in Paragraph 6.8.1.3 before continuing this procedure.

(3) Acceptable limits:

- 4.25v (maximum) peak-to-peak
- 3.75v (minimum) peak-to-peak

(4) Monitor TP21 and observe that the peak-to-peak envelope variations should be less than 0.5v throughout the full stroke of the positioner. If the voltage variation envelope is greater than 0.5v, perform the scale-flatness adjustment in Paragraph 6.8.1.4.

6.8.1.3 Adjustment Procedure

(1) Adjust potentiometer R60 (X + 0 Gain) to attain a 4v peak-to-peak sine wave at TP21 on the oscilloscope screen while the positioner carriage is being slowly moved back and forth through its full stroke by hand.

NOTE

Clockwise rotation of R60 will increase amplitude.

(2) If the 4v peak-to-peak sine wave cannot be attained, perform the signal polarity and quadrature checks in Paragraph 6.8.3.

(3) Adjust potentiometer R57 (X + 0 Balance) to center the waveform equally about ground within ± 0.25v.

(4) Perform the X + 90 Gain and Balance procedure detailed in Paragraph 6.8.2.

6.8.1.4 Scale-Flatness Adjustment

(1) Loosen the three Allen-head screws that hold the scale assembly to the side of the carriage. The scale will pivot slightly around its locating pin.

(2) Manually move the positioner carriage back and forth slowly (at a constant rate) through its full stroke while monitoring the waveform at TP21 (X + 0) (refer to Figure 6-4).

(3) Adjust the horizontal angle of the scale so that the amplitude of the waveform at TP21 remains constant throughout each full stroke of the positioner carriage.

(4) Tighten the Allen-head screws loosened in Step (1).

(5) Perform the adjustment procedure detailed in Paragraph 6.8.1.3.

6.8.2 X + 90 GAIN AND BALANCE

The X + 0 Gain and Balance checks and adjustments in Paragraph 6.8.1 must be performed before the X + 90 Gain and Balance tests.

6.8.2.1 Test Configuration

(1) Prepare the positioner and oscilloscope as described in Paragraph 6.7.1, Steps (1)—(5), and (16).

(2) Remove connector P215 from the Servo PCBA.

(3) Connect oscillosope Channel 1 X10 test probe to TP15 and ground lead to TP26.

(4) Set oscilloscope Channel 1 sensitivity to 2v per division.

(5) Set horizontal sweep rate to 2 msec per division.

(6) Set oscilloscope trigger control to Line and Auto.

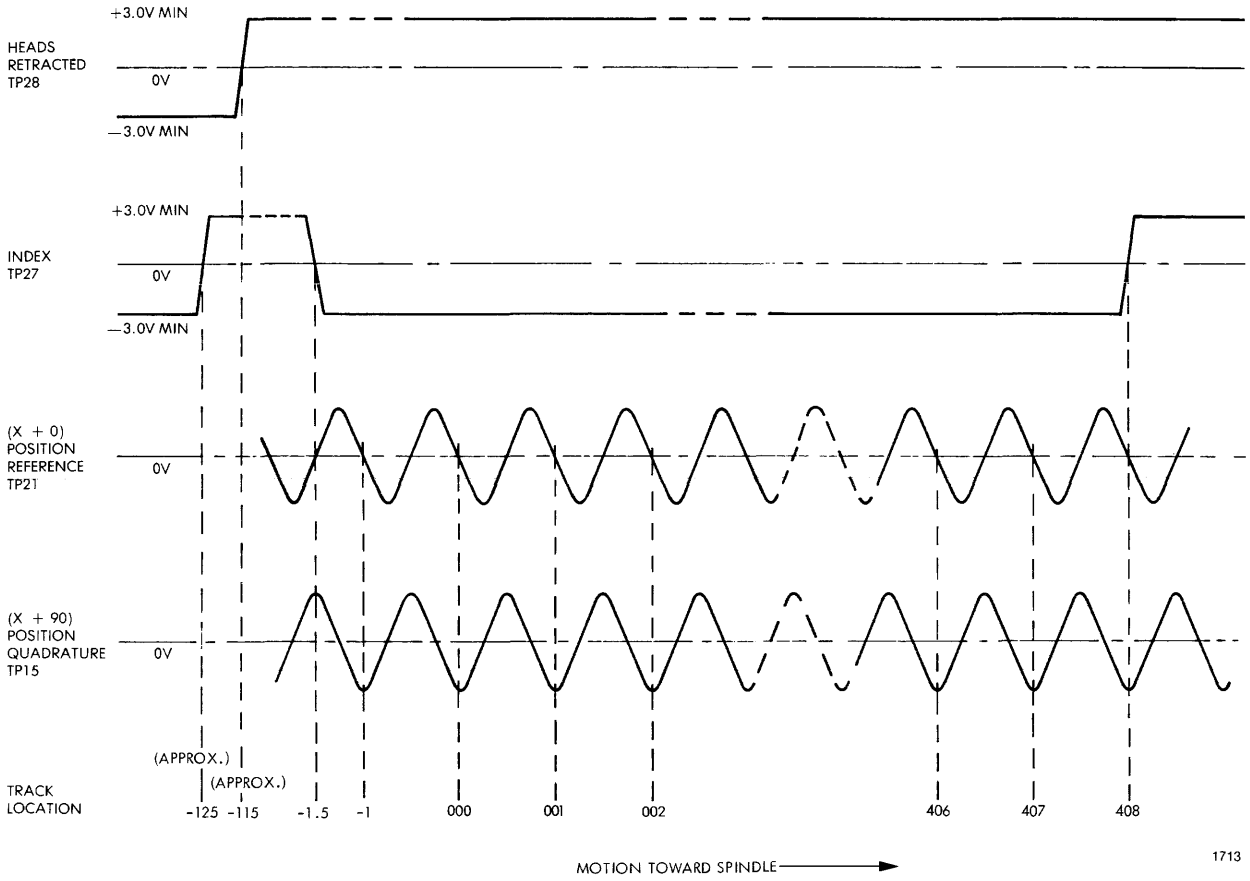


Figure 6-4. Position Transducer Signal Amplifier Outputs

(7) Manually load the heads onto the disk.

NOTE

A ground reference sweep trace is obtained by centering the trace on a particular graticule line with vertical input mode switch of oscilloscope set to ground position.

6.8.2.2 Test Procedure

(1) Manually move the positioner carriage slowly, and at a constant rate, back and forth through its full stroke, i.e., cylinder 000 to cylinder 405. Do not unload the heads from the disk.

(2) Monitor TP15 on oscilloscope Channel 1 and observe the X + 90 Position Quadrature waveform shown in Figure 6-4 as the positioner is being moved. The peak-to-peak voltage observed throughout the full stroke must fall within the acceptable limits listed in Step (3) and balanced about ground within ± 0.25v. If the acceptable limits are exceeded, perform the adjustment procedure detailed in Paragraph 6.8.2.3.

(3) Acceptable limits:

- 4.25v (maximum) peak-to-peak
- 3.75v (minimum) peak-to-peak

6.8.2.3 Adjustment Procedure

(1) Adjust potentiometer R69 (X + 90 Gain) to attain a 4v peak-to-peak sine wave at TP15 on the oscilloscope screen while the positioner carriage is being slowly moved back and forth through its full stroke by hand.

NOTE

Clockwise rotation of R69 will increase amplitude.

(2) Adjust potentiometer R66 (X + 90 Balance) to center the sine wave equally about ground within ±0.25v. If required, reposition the ground-referenced sweep trace to the center graticule line.

(3) Perform X + 0 and X + 90 Signal Polarity and Quadrature check detailed in Paragraph 6.8.3.

6.8.3 X + 0 AND X + 90 SIGNAL POLARITY AND QUADRATURE CHECK

The following procedure will verify the correct polarity of the X + 0 and X + 90 signals and their correct phase relationship.

6.8.3.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.1, Steps (1)—(5), and (16).

(2) Set the oscilloscope to the chopped mode.

(3) Connect Channel 2 X10 test probe to TP19.

(4) Connect Channel 1 X10 test probe to TP21.

(5) Set Channel 1 sensitivity to 2v per division.

(6) Set Channel 2 sensitivity to 2v per division.

(7) Position the ground-referenced sweep trace of both channels to the center graticule line.

(8) Manually load the heads onto the disk.

6.8.3.2 Test Procedure

(1) Observe the signal at TP19 on Channel 2 while manually moving the positioner carriage through its full stroke.

NOTE

Channel 2 output should be a digital signal of approximately 0v to 5v. If the digital signal cannot be observed, repeat X + 90 Balance procedure (Paragraph 6.8.2).

(2) Readjust the sensitivity of Channel 2 to 5v per division.

(3) Set Channel Select switch to Add mode (Channel 1 plus Channel 2).

(4) Sync internally off of Channel 1 on the positive portion of the analog signal.

(5) Manually move the positioner carriage back and forth, at a constant rate, through its full stroke.

(6) Observe that the X + 90 digital signal, added to the X + 0 analog signal, appears on the positive and negative peak of the sine wave as illustrated in Figure 6-5.

(7) While moving the positioner carriage forward (toward the spindle) verify that the added digital signal (X + 90) has its trailing edge on the positive peak of the sine wave (see Figure 6-5).

NOTE

The signal observed might not be balanced about ground due to adding the two signals together.

(8) If the trailing edge of the digital signal is not on the positive peak of the sine wave, or the oscilloscope pattern does not correlate with Figure 6-5, perform the adjustment procedure detailed in Paragraph 6.8.3.3.

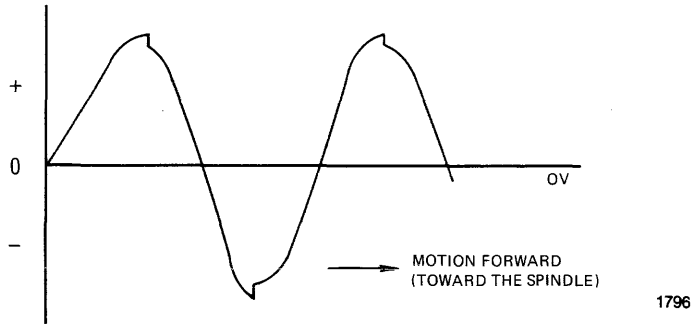


Figure 6-5. X + 0 Analog Signal Added to X + 90 Digital Signal

6.8.3.3 Adjustment Procedure

CAUTION

IN PERFORMING THIS PROCEDURE, DO NOT LOOSEN ALLEN-HEAD SCREW THAT CLAMPS THE THERMAL BLOCK TO THE BASE CASTING.

(1) Loosen the horizontal hex-head screw on the thermal block. This will loosen the receiver post upon which the reticle is mounted.

(2) Check that the reticle arm is approximately at right angles to the scale.

(3) Manually move the positioner carriage back and forth through its full stroke, while monitoring the waveform at TP19 and TP21. At the same time (using a wide-edge screwdriver in the grooves provided at the top of the receiver post) rotate the reticle CW or CCW until the waveform of Figure 6-5 is achieved. Observe that this waveform will occur at more than one angular position of the reticle. Set the reticle at the position which results in the waveform as shown in Figure 6-5 and with maximum amplitude.

(4) Partially tighten the hex-head screw, loosened in Step (1), to the point where self-rotation of the receiver is inhibited.

NOTE

This prepares the receiver post for the Dynamic Reticle-to-Scale Adjustment contained in Paragraph 6.9.3.

(5) Perform the Heads Retracted Signal Check described in Paragraph 6.8.4.

6.8.4 HEADS RETRACTED SIGNAL CHECK

The Heads Retracted Signal Check is made to ascertain the approximate position at which the signal occurs and to determine if the voltages generated are within acceptable limits and have the correct polarity.

6.8.4.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.1, Steps (1)—(5), and (16).

(2) Connect Channel 1 test probe to TP28.

(3) Connect Channel 2 test probe to TP13.

(4) Set Channel 1 sensitivity to 2v per division.

(5) Set Channel 2 sensitivity to 2v per division.

(6) Use automatic or normal sync, internal trigger mode, and trigger on positive slope.

(7) Set sweep rate to 20 msec per division.

(8) Manually load the heads onto the disk.

6.8.4.2 Test Procedure

(1) Move the positioner carriage to its fully retracted position. Note that the spindle speed decreases as the heads are unloaded.

(2) Select Channel 1.

- Check that the dc level of the signal at TP28 is equal to or more negative than – 3v (refer to Figure 6-4).
- Slowly move the positioner carriage approximately ½-inch toward the spindle and at the same time observe that the signal at TP28 changes in dc level from – 3v or more negative to + 3v or more positive.
- Continue to move the positioner carriage slowly toward the spindle all the way to the front stop. Check that the signal voltage remains at + 3v as shown in Figure 6-4.

NOTE

There may be some crosstalk present on the signal; however, voltage tolerances specified above must be met.

(3) Select Channel 2.

- Return the positioner carriage to its fully retracted position.
- Observe that the digital signal at TP13 is a high state.
- Slowly move the positioner carriage approximately ½-inch toward the spindle and at the same time observe that the digital signal at TP13 changes from a high to a low state.
- Continue to move the positioner carriage slowly toward the spindle, all the way to the stop. Note that the signal always remains in the low state.

NOTE

If the limits of Steps (2) and (3) are exceeded, refer to Adjustment Procedure in Paragraph 6.8.4.3.

(4) Perform the Index Balance procedure detailed in Paragraph 6.8.5.

6.8.4.3 Adjustment Procedure

Repeat the tests and adjustment procedures contained in Paragraphs 6.7.1 through 6.8.4.2. In the event that test limits given in Paragraph 6.8.4.2 are exceeded after repeating these tests, replacement of the positioner carriage or the Servo PCBA may be required.

6.8.5 INDEX BALANCE

The index area is located very close to where the heads are either loaded or unloaded from the ramp. This load/unload position is within ¼-inch from the outside rim of the disk.

6.8.5.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.1, Steps (1)—(5) and (16).

(2) Connect Channel 1 probe to TP27.

(3) Position Channel 1 ground-referenced sweep trace to the center line of graticule.

(4) Connect Channel 2 probe to TP16.

(5) Set Channel 1 sensitivity to 2v per division.

(6) Set Channel 2 sensitivity to 2v per division.

(7) Use automatic or normal sync, internal trigger mode, and trigger on positive slope.

(8) Set sweep rate to 20 msec per division.

6.8.5.2 Test Procedure — Channel 1

(1) Select Channel 1.

(2) Manually move the positioner carriage back and forth within the index area (within the first ¼-inch after the heads are loaded onto the disk).

(3) Check that the signal at TP27 changes from + 3v to − 3v or more negative (refer to Figure 6-4). Adjust potentiometer R75 (Index Balance) to obtain an equal balance of the + and − dc levels with respect to ground.

NOTE

Clockwise adjustment of R75 will shift signal more positive.

(4) Continue to adjust R75 until the transition region is approximately centered about ground.

NOTE

If crosstalk is observed, R75 must be adjusted to ensure that it does not exceed the limits specified in Step (3).

(5) Fully retract the positioner carriage.

(6) Slowly move the positioner carriage approximately ½-inch closer to the spindle.

(7) Observe on Channel 1 at TP27 a signal change from − 3v or more negative to + 3v (refer to Figure 6-4).

(8) Moving the positioner carriage further forward toward the spindle through the index area (heads now loaded) will again reverse the signal from + 3v to − 3v or more negative.

(9) Check that the signal remains at − 3v or more negative as the positioner carriage is moved through the full stroke and that this condition is maintained to a point just prior to touching the front end of the positioner assembly at approximately cylinder 406.

(10) Note that at approximately the point where the positioner carriage touches the front end of the positioner, which is approximately cylinder 408, the signal reverses once again from − 3v to + 3v. Also observe that at each transition point only a single transition from high to low or low to high occurs.

NOTE

If a transition does not occur, adjustment of the transducer assembly position is required. Refer to Paragraph 6.8.5.4 for adjustment procedure.

6.8.5.3 Test Procedure — Channel 2

(1) Select Channel 2.

(2) Fully retract positioner carriage to the back stop.

(3) Slowly move the positioner carriage ½-inch toward the spindle.

(4) Observe on Channel 2 that the digital signal at TP16 changes from a low to a high state.

(5) Observe, as the positioner carriage is moved forward through the index area (head now loaded), the signal changes from a high to a low state.

(6) Observe that the signal remains low as the positioner carriage is moved further toward the spindle. Ensure that this condition is maintained to a point just prior to touching the front end of the positioner assembly.

(7) At approximately the end of the forward stroke of the positioner, the signal reverses again from a low to a high state. Also note that at each transition point, only a single transition of the logic state (from low to high or high to low) occurs.

6.8.5.4 Adjustment Procedure

In the event that the voltage transitions do not occur according to the tests performed in Paragraphs 6.8.5.2 and 6.8.5.3, repeat the test and adjustment procedures detailed in Paragraphs 6.7 through 6.8.5.4.

6.8.6 POSITIONER VOICE COIL POLARITY CHECK

This test will establish that the electrical connections to the positioner voice coil have the correct polarity.

6.8.6.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.1.

(2) Connect the Voice Coil Polarity tester (Pertec Part No. 103607) onto connector P205.

(3) Maintain the drive in the operating mode with the heads loaded onto the disk.

6.8.6.2 Test Procedure

(1) Manually move the positioner carriage forward toward the spindle in a brisk manner. Observe that the red indicator on the voice coil polarity tester becomes illuminated. Also note that the red indicator becomes extinguished and remains extinguished as the positioner carriage is moved away from the spindle.

NOTE

If the red indicator on the voice coil polarity tester remains extinguished when the positioner carriage is moved toward the spindle and becomes illuminated when the positioner carriage is moved away from the spindle, perform the adjustment procedure in Paragraph 6.8.6.3.

(2) Return the carriage to the retracted position.

(3) Remove power from the drive.

(4) Disconnect the voice coil polarity tester from connector P205.

6.8.6.3 Adjustment Procedure

(1) Reverse the wiring at P205 between pins 1 and 4, and between pins 2 and 5.

(2) Check operation by repeating the test procedure in Paragraph 6.8.6.2.

(3) Perform the Power-Down procedure detailed in Paragraph 6.8.7.

6.8.7 POWER-DOWN PROCEDURE

It is important that the Dynamic Positioner Adjustments detailed in Paragraph 6.9 and the Performance Checks detailed in Paragraph 6.10 be performed subsequent to performing the Static Positioner Adjustments specified in Paragraph 6.8.

(1) Manually return the positioner carriage to its fully retracted position.

(2) Place the power ON/OFF switch to the OFF position.

(3) Replace the Read/Write PCBA.

(4) Remove the emergency unload connector P128 from the Logic PCBA.

(5) Replace connector P205 and connector P215 on the Servo PCBA.

(6) Complete the Dynamic Positioner adjustments detailed in Paragraph 6.9.

6.9 DYNAMIC POSITIONER ADJUSTMENTS

The dynamic tests and adjustments required to ensure proper operation of the Positioner Servo are contained in the following paragraphs. Although these tests and adjustments may be performed independent of the static tests and adjustments, they must be performed when the procedures contained in Paragraph 6.8 are performed.

6.9.1 POSITIONER PREPARATION, DYNAMIC TESTS

The following functions are required to prepare the positioner for calibration.

(1) Remove power from the drive.
(2) Verify that connector P205 is connected to the Servo PCBA.
(3) Remove Emergency Unload jumper plug P128 from the Logic PCBA.
(4) Remove the interface connector and terminator board from connectors J101 and J102 located on the Logic PCBA.
(5) Install PCC PD Hand-Held Exerciser Model TE-D02 (or equivalent) into interface connector J101.
(6) Disconnect connector P215 from the Servo PCBA.
(7) Apply power to the drive and allow it to come SAFE.
(8) Insert a disk cartridge into the drive.
(9) Depress the RUN/STOP switch once and observe that the positioner loads the heads after approximately 65 seconds.
(10) Observe that the drive comes to READY in approximately 110 seconds.

CAUTION

ALL DYNAMIC CALIBRATION TESTS REQUIRE THAT THE DRIVE ROTATE THE DISKS AT THEIR DESIGN SPEED; OPERATION AT ANY OTHER SPEED CAN CAUSE DAMAGE TO DISK RECORDING SURFACES AND HEADS.

6.9.2 DYNAMIC ADJUSTMENTS

6.9.2.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.
(2) Set the oscilloscope as follows.
- Position ground reference sweep trace of Channels 1 and 2 to center graticule line.
- Set Channel 1 sensitivity to 1v per division.
- Connect Channel 1 X10 test probe to TP21.
- Set Channel 2 sensitivity to 1v per division.
- Set vertical input (Channels 1 and 2) to dc.
- Connect Channel 2 X10 test probe to TP15.
- Using a X10 probe, connect External Trigger Input to TP11 on the Logic PCBA.
- Set the horizontal sweep rate to 2 msec per division.
- Use normal sync, external trigger mode, and trigger slope negative.

(3) Set the disk exerciser to perform a one-track repetitive seek from cylinder 000 to cylinder 001.
(4) Set the disk exerciser to the DN or SEEK mode.

6.9.2.2 Test Procedure

(1) Select Channel 1.

(2) Observe the amplitude of the waveform at TP21 as shown in Figure 6-6 while performing a one-track repetitive seek.

NOTE

Careful observation of the X + 0 signal at TP21 will show a small disturbance near the forward and reverse waveform peaks. This disturbance is normal and occurs at the point where the Servo switches into the Position mode.

(3) Acceptable limits:
- 4.25v (maximum) peak-to-peak
- 3.75v (minimum) peak-to-peak

(4) If the acceptable limits are not met, perform the adjustment given in Paragraph 6.9.2.3, Step (1), before continuing this procedure.

(5) Check that the waveform at TP21 is balanced about ground as shown in Figure 6-6.

(6) If the waveform is not balanced about ground within ±0.25v, perform the adjustment given in Paragraph 6.9.2.3, Step (2), before continuing this procedure.

(7) Check that the start of the waveform is balanced about ground (Figure 6-6).

(8) If the start of the waveform is not balanced about ground, perform the adjustment given in Paragraph 6.9.2.3, Step (3), before continuing this procedure.

(9) Select Channel 2 (probe to TP15).

(10) Observe the amplitude of the waveform at TP15 (Figure 6-7) while performing a one-track repetitive seek.

(11) Acceptable limits:
- 4.25v (maximum) peak-to-peak
- 3.75v (minimum) peak-to-peak

(12) If the acceptable limits are not met, perform the adjustment given in Paragraph 6.9.2.3, Step (4), before continuing this procedure.

(13) Check that the waveform is balanced about ground as shown in Figure 6-7.

(14) If the waveform is not balanced about ground, perform the adjustment given in Paragraph 6.9.2.3, Step (5), before continuing this procedure.

(15) Select Channel 1 (probe to TP21).

(16) Observe that the waveform at TP21 is symmetrical about ground as shown in Figure 6-8; Figure 6-9 is given as an example of unbalanced crossover points.

(17) If the crossover point does not occur at ground within ±0.25v, perform the Dynamic Reticle-to-Scale Phase Adjustment procedure given in Paragraph 6.9.3 before continuing this procedure.

(18) Check that the X + 0 waveform at TP21 meets all requirements shown in Figure 6-6, i.e., waveform amplitude, symmetrical start, waveform balanced about ground, correct crossover point. If the waveform does not meet these requirements, repeat Steps (1) through (17) of this procedure.

(19) If the Static Positioner Adjustments (Paragraph 6.8) were performed prior to performing the Dynamic Positioner Adjustments, tighten the hex-head screw on the thermal block loosened in Paragraph 6.8.3.3, Step (1).

NOTE

Ensure, by observing the waveform on TP21, that tightening the hex-head screw on the thermal block has not disturbed or altered the crossover point.

(20) Proceed with the Current Adjustment in Paragraph 6.9.4.

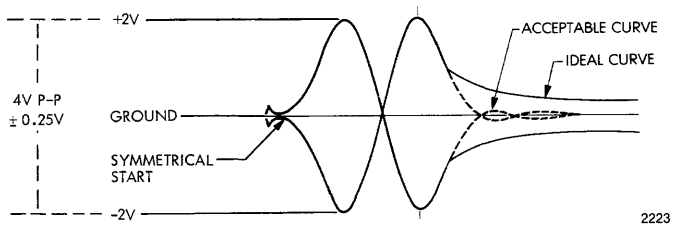


Figure 6-6. X + 0 Waveform, One-Track Repetitive Seek (TP21)

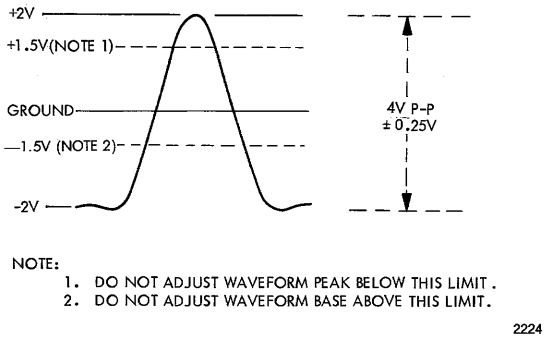


Figure 6-7. Analog Waveform Limits, One-Track Repetitive Seek (TP15)

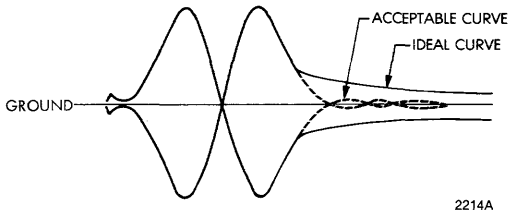


Figure 6-8. X + 0 Crossover Correctly Occurring at Ground

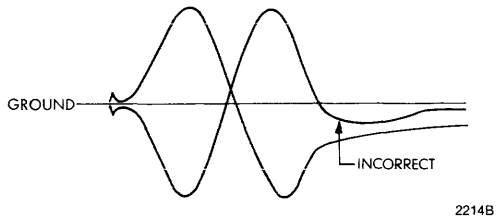


Figure 6-9. X + 0 Crossover Incorrectly Occurring Below Ground

6.9.2.3 Adjustment Procedure

The following adjustments are directly referenced in Paragraph 6.9.2.2 and should be performed only as specified.

(1) Observe TP21 and set R60 to attain a 4v peak-to-peak envelope.

(2) Observe TP21 and set R57 so that the waveform is balanced about ground (Figure 6-6).

(3) Observe TP21 and set R145 so that the start of the waveform is balanced about ground (Figure 6-6).

(4) Observe TP15 and set R69 so that amplitude of the waveform is 4v peak-to-peak.

(5) Observe TP15 and set R66 so that the waveform is balanced about ground (Figure 6-7).

6.9.3 DYNAMIC RETICLE-TO-SCALE PHASE ADJUSTMENTS

Adjustment of the reticle is required when the position mode waveform does not have the crossover point at ground (Figure 6-9).

CAUTION

ONLY SLIGHT ADJUSTMENT OF THE ANGLE BETWEEN THE RETICLE AND THE POSITION TRANSDUCER SCALE IS REQUIRED. OVER-ADJUSTMENT WILL CAUSE A LOSS OF TRANSDUCER SIGNALS AND THE POSITIONER TO GO UNCONTROLLED; PERFORM SIGNAL POLARITY AND QUADRATURE CHECKS IN PARAGRAPH 6.8.3.

6.9.3.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Establish oscilloscope settings as described in Paragraph 6.9.2.1, Step (2).

6.9.3.2 Test Procedure

(1) Set exerciser for a 000 to 001 track seek.

(2) Set exerciser to DN or SEEK mode.

(3) Slightly loosen the horizontal hex-head screw at the base of the receiver post; this will allow the receiver post to be rotated horizontally.

6.9.3.3 Adjustment Procedure

(1) Insert a screwdriver blade into the slot at the top of the receiver post and adjust the reticle so that the waveform observed at TP21 is positioned with its crossover point at ground as shown in Figure 6-9(A).

(2) Tighten the hex-head screw loosened in Paragraph 6.9.3.2, Step (3). Check the waveform at TP21 to ensure that tightening the screw has not disturbed or altered the crossover point.

(3) Observe the amplitude of the waveform at TP21 (Figure 6-6).

(4) Acceptable limits:

- 4.25v (maximum)
- 3.75v (minimum)

(5) If the acceptable limits are not met, adjust R69 to obtain a 4v peak-to-peak envelope at TP21.

(6) Check that the waveform at TP21 is balanced about ground as shown in Figure 6-6.

(7) If the waveform at TP21 is not balanced about ground, adjust R57 until the waveform is balanced.

(8) Check that the start of the waveform at TP21 is symmetrical about ground as shown in Figure 6-6.

(9) If the start of the waveform is not symmetrical, adjust R145 to obtain the correct waveform.

(10) Select Channel 2 and check that the amplitude of the waveform at TP15 is 4.0v ± 0.25v peak-to-peak as shown in Figure 6.7. Adjust R69 if necessary to obtain the peak-to-peak amplitude.

(11) Check that the waveform at TP15 is balanced about ground as shown in Figure 6-7. Adjust R66 if necessary to balance the waveform about ground.

6.9.4 CURRENT ADJUSTMENT

The following current adjustment procedure is made to ensure that the positioner carriage will perform a 134-track seek within an average time interval of 38.5 msec.

6.9.4.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Set the oscilloscope as follows.

- Set the Channel 1 sensitivity to 0.2v per division.
- Set the sweep rate to 1 msec per division.
- Connect Channel 1 X10 test probe to TP30.

(3) Set the disk exerciser to produce a 134-track repetitive seek from cylinder 000 to cylinder 134.

(4) Set the disk exerciser to DN or SEEK mode.

6.9.4.2 Test Procedure

(1) Select Channel 1.

(2) Observe the current waveform at TP30 as shown in Figure 6-10.

(3) Acceptable limits:

- 1.54v (maximum)
- 1.26v (minimum)

(4) If the acceptable limits of the waveform at TP30 are not met, the adjustment procedure detailed in Paragraph 6.9.4.3 must be performed.

6.9.4.3 Adjustment Procedure

(1) Observe the current waveform at TP30.

(2) Adjust potentiometer R163 until the waveform observed has a peak-to-peak amplitude of 1.4v (Figure 6-10).

6.9.5 SEEK-TIME ADJUSTMENT

6.9.5.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Set the oscilloscope as follows.

- Set Channel 1 sensitivity to 1v per division.
- Set sweep rate to 5 msec per division.
- Connect Channel 1 X10 test probe to TP12 on the Servo PCBA.

6.9.5.2 Test Procedure

(1) Using the oscilloscope Channel 1 test probe, observe that the waveform at TP12 appears as shown in Figure 6-11.

(2) If the waveform and timing at TP12 does not appear correctly, perform the adjustments in Paragraph 6.9.5.3; otherwise, proceed with the Overshoot and Settling Response Tests in Paragraph 6.9.6.

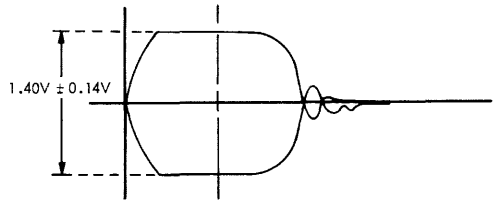


Figure 6-10. Current Waveform After Adjustment of R163 (TP30)

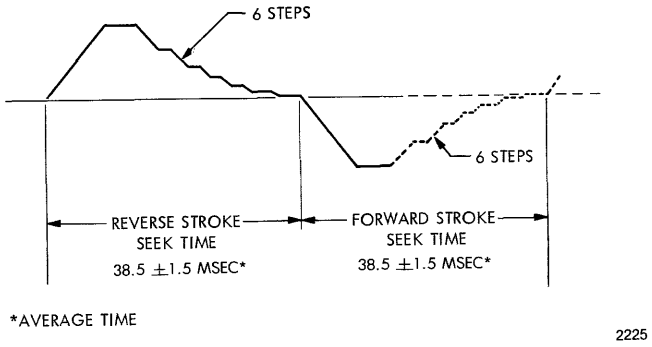


Figure 6-11. Velocity Feedback Waveform, TP12

6.9.5.3 Adjustment Procedure

(1) Observe the waveform at TP12.

(2) Adjust potentiometer R136 to obtain both forward-and-reverse seek times of 38.5 ± 1.5 msec.

NOTE

Average seek time is the average between the forward and reverse strokes; see Figure 6-11.

(3) If the average seek time cannot be attained, perform the Current Adjustment procedure in Paragraph 6.9.4.

6.9.6 OVERSHOOT PROCEDURE

The following steps are used to measure the overshoot of the positioner.

6.9.6.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Set the oscilloscope as follows.

- Set Channel 1 sensitivity to 0.5v per division.
- Connect Channel 1 test probe to TP21.
- Set Channel 2 sensitivity to 2v per division.
- Connect Channel 2 X10 test probe to TP10 on the Logic PCBA (Busy Time Signal NLBTFF).
- Set sweep rate to 2 msec per division.
- Set Channel Select switch to Chopped mode.
- Set internal sync to Channel 2 and trigger on negative slope.

(3) Set the disk exerciser as follows.
- Set exerciser for a repetitive one-track seek (000—001).
- Set Data mode switch to DN or SEEK.
- Set exerciser to Auto.

6.9.6.2 Test Procedure

(1) Observe the waveform at TP11 (on the Logic PCBA) and TP21 (on the Servo PCBA); refer to Figure 6-12.

(2) If overshoot exceeds ±0.5v, or excessive undershoot is evident, perform Overshoot Adjustment in Paragraph 6.9.7.

6.9.7 OVERSHOOT ADJUSTMENT PROCEDURE

The following steps are used to adjust the overshoot of the positioner.

6.9.7.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Set the oscilloscope as follows.
- Set Channel 1 sensitivity to 0.5v per division.
- Connect Channel 1 X10 test probe to TP21.
- Set Channel 2 sensitivity to 1v per division.
- Connect Channel 2 X10 test probe to TP15.

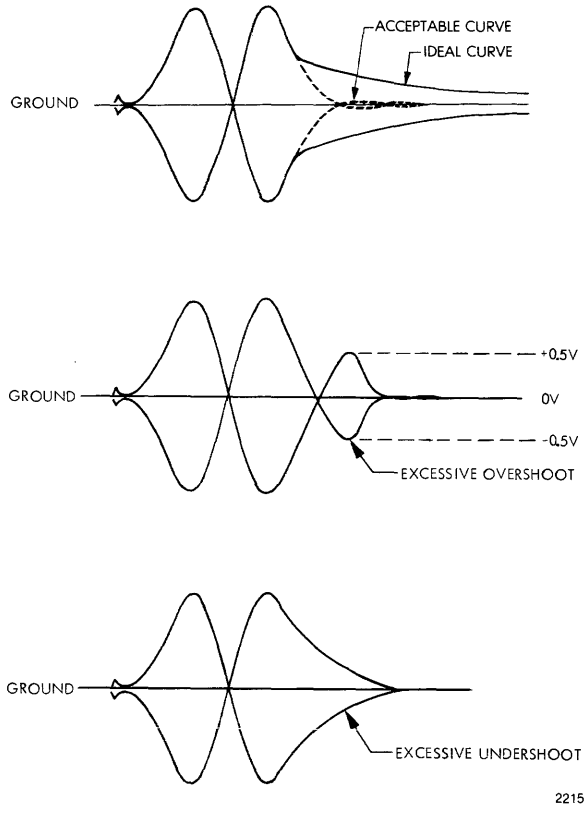


Figure 6-12. X + 0 Waveforms 000-001 Repetitive Track Seek

- Using an X10 test probe, connect external trigger input to TP10 on Logic PCBA.
- Set sweep rate to 2 msec per division.
- Use normal sync, external trigger mode, and trigger slope negative.

(3) Set the disk exerciser to perform a one-track repetitive seek from cylinder 000 to cylinder 001.

6.9.7.2 Adjustment Procedure

(1) Select Chopped mode on the oscilloscope.

(2) Observe waveforms at TP21 (Figure 6-12) and TP15 (Figure 6-7) while performing one-track seek.

(3) While adjusting R66 for minimum overshoot (Figure 6-12), ensure that the positive peak of the waveform at TP15 is > + 1.5v and that the negative excursion is more negative than – 1.5v (Figure 6-7).

6.9.8 INDEX TO QUADRATURE CLOCK RELATIONSHIP

This adjustment is used to correctly establish the relationship between the trailing edge of the Quadrature Clock (SPQCG) with respect to the trailing edge of the Index Logic Signal (SPTIG) as shown in Figure 6-13.

6.9.8.1 Test Configuration — Step 1

(1) Set the oscilloscope as follows.

- Set sensitivity of both channels to 2v per division.
- Connect Channel 1 test probe to TP16.
- Connect Channel 2 test probe to TP19.
- Sync internal on Channel 1, use positive trigger slope.
- Set sweep rate to 0.5 msec per division.
- Set channel select switch to Chopped mode.

(2) Set exerciser to operate in the repetitive Restore mode.

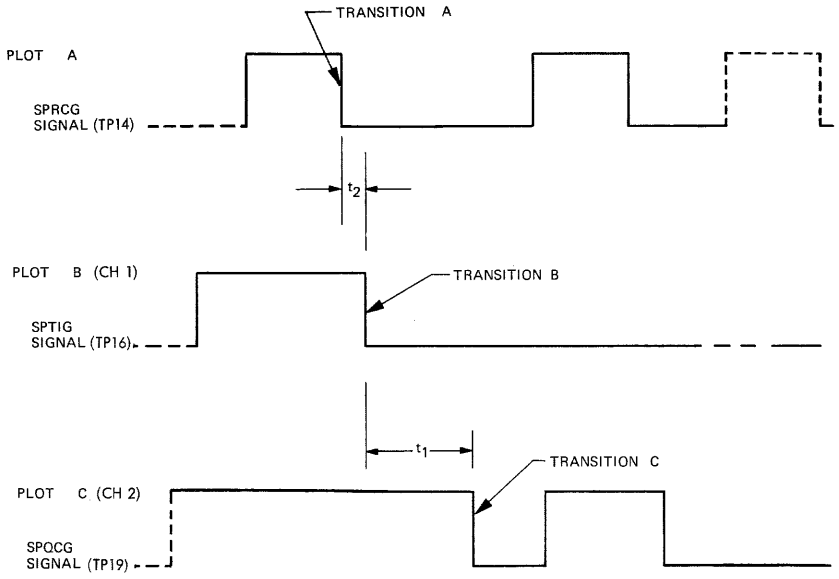


Figure 6-13. SPRCG, SPTIG, SPQCG Signals, Repetitive Restore Mode

6.9.8.2 Test Procedure — Step 1

(1) Observe the relative position of the high-to-low transition of signal SPQCG on Channel 2 (TP19) in relation to the high-to-low transition of signal SPTIG on Channel 1 (TP16). The waveform relationship must be approximately as shown in Figure 6-13, Plots B and C.

NOTE

There must be exactly two high-to-low transitions and one low-to-high transition of SPQCG after the high-to-low transition of SPTIG.

(2) Connect Channel 2 test probe to TP14. Observe SPRCG on Channel 2 in relation to the high-to-low transition of SPTIG (see Figure 6-13, Plots A and B).

NOTE

After the high-to-low transition of SPTIG, there must be either one or two low-to-high transitions and either one or two high-to-low transitions of SPRCG.

NOTE

Stable nulls for either of two distinct tracks may occur as a result of this procedure. A CE check should be made after an index adjustment. If the CE track has shifted and fixed disk information is not required, readjust the heads; if fixed disk information is required, readjust the index.

(3) The high-to-low transition of SPTIG (Transition B of Figure 6-13) should occur at or after the low-to-high transition of SPRCG (Transition A of Figure 6-13), i.e., time t_2 should be greater than or equal to zero seconds.

(4) If the requirements of Steps (1), (2) and (3) are not satisfied, perform the adjustment procedure outlined in Paragraph 6.9.8.3, then repeat the foregoing steps prior to continuing this procedure. If adjustments to satisfy the above requirements cannot be made, replacement of position transducer scale may be necessary.

(5) Change the oscilloscope settings established in Paragraph 6.9.8.1, as follows.

- Connect Channel 2 test probe to TP19.
- Sync internal on Channel 1, use negative trigger slope.

NOTE

It may be necessary to change the sweep rate to a more desirable setting.

(6) Observe the first high-to-low transition of SPQCG (TP19) with respect to the high-to-low transition of SPTIG (TP7); see Figure 6-14.

NOTE

The high-to-low transition of SPQCG (Transition C of Figure 6-14) should occur after a time delay (t_1 of 300 ± 100 μsec after the occurrence of the high-to-low transition of SPTIG (Transition B of Figure 6-14). See Figure 6-13, Plots B and C, and Figure 6-14.

6.9.8.3 Adjustment Procedure — Step 1

(1) Adjust Index Balance potentiometer R75 to position the trailing edge of SPTIG (TP16) to occur prior to the trailing edge of SPQCG (TP13) as shown in Figure 6-13.

(2) Change the oscilloscope settings established in Paragraph 6.9.8.2, as follows.

- Set sweep rate to 50 μsec per division.
- Sync internal on Channel 1, use negative trigger slope.

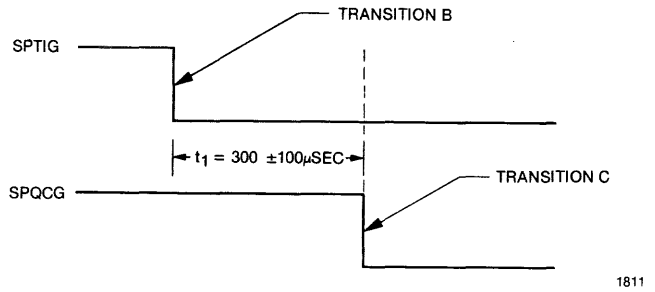


Figure 6-14. Correct Relationship Between SPQCG and SPTIG Signals, Expanded

(3) Continue to adjust potentiometer R75 so that the high-to-low transition of SPTIG occurs approximately 300 ± 100 μsec before the high-to-low transition of SPQCG as shown in Figure 6-14.

6.9.8.4 Test Configuration — Step 2

(1) Set oscilloscope as follows.
- Set Channel 1 sensitivity to 1v per division.
- Connect Channel 1 test probe to TP27.
- Set sweep rate to 1 msec per division.
- Sync internal on Channel 1, use positive trigger slope.
- Set Channel 1 ground-referenced sweep trace to the center line of graticule.

(2) The exerciser remains operating in the repetitive Restore mode.

6.9.8.5 Test Procedure — Step 2

(1) Select Channel 1.

(2) Observe that the Index signal at TP27 makes a transition from a point more negative than −3v to a value greater than 0v as shown in Figure 6-15.

(3) If the waveform observed at TP27 is within limits, perform the Overshoot and Settling Response procedure detailed in Paragraph 6.9.9. If the observed waveform does not fall within the specified limits, perform the adjustments in Paragraph 6.9.8.6.

6.9.8.6 Adjustment Procedure — Step 2

(1) Adjust the Index Balance potentiometer R75 to obtain a minimum of −3v transition of the index waveform from ground as shown in Figure 6-15.

(2) Ensure that the relationship between SPQCG and SPTIG established in Paragraph 6.9.8.3, Step (3), is maintained.

(3) Repeat the SPOCG and SPRCG Test Procedures, Paragraph 6.9.8.2

(4) Repeat the Analog Index Balance Test Procedure, Paragraph 6.9.8.5.

(5) If the waveform at TP27 still does not fall within the specified limits, replacement of the transducer assembly may be required.

NOTE

If crosstalk is observed, it must not appear within the +3v, −3v area shown in Figure 6-15. If the limits of Step (6) are exceeded and crosstalk appears in this area, repeat the adjustment procedure in Paragraph 6.9.8.6.

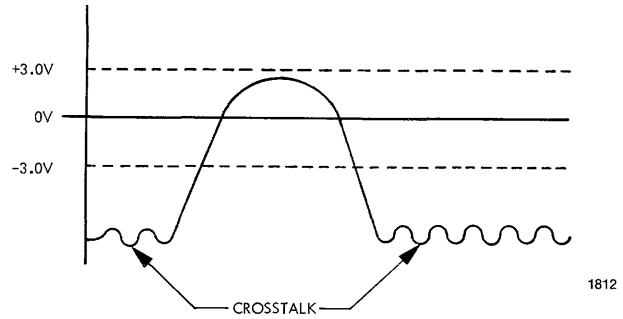


Figure 6-15. Index Signal, TP27, Repetitive Restore Mode

6.9.9 OVERSHOOT AND SETTLING RESPONSE OFFSET PROCEDURE

The following steps are used to measure the overshoot and settling response of the positioner.

6.9.9.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.1.

(2) Set the oscilloscope as follows.

- Set Channel 1 sensitivity to 0.5v per division.
- Connect Channel 1 X10 test probe to TP21.
- Set Channel 2 sensitivity to 2v per division.
- Connect Channel 2 X10 test probe to TP10 on the Logic PCBA (Busy Signal NLBSXG).
- Set sweep rate; refer to Table 6-4, Step 1.
- Set channel select switch to Chopped mode.
- Set internal sync to Channel 2.

(3) Set disk exerciser as follows.

- Set exerciser to perform a repetitive one-track seek; refer to Table 6-4, Step 1.
- Set Data mode switch to R/W.
- Set exerciser to Auto.

6.9.9.2 Test Procedure

(1) With the exerciser set to the appropriate track seek, observe both the overshoot and settling response; refer to Figure 6-16.

(2) Check that the overshoot is less than ± 0.5v.

(3) Check that the X + 0 settling response offset in the settling band is less than 0.25v.

(4) If either the overshoot or the settling response observed is outside the limits specified, perform the adjustments in Paragraph 6.9.9.3.

6.9.9.3 Adjustment Procedure

(1) Move Channel 2 test probe to TP15.

(2) Set Channel 2 sensitivity to 1v per division.

(3) Using an X10 test probe, connect external trigger input to TP10 on the Logic PCBA.

(4) Use normal sync, external trigger mode, and trigger slope negative.

(5) Set sweep rate according to Table 6-4, Step 1.

(6) While observing waveforms at TP15 and TP21 simultaneously (TP15 in Figure 6-7 will be superimposed on TP21 in Figure 6-16), adjust R66 so that the overshoot at TP21 is less than 0.5v while waveforms at TP15 do not exceed established limits.

NOTE

For one-track seeks, use Figure 6-8 as a waveform reference to TP21; for longer than one-track seeks, use Figure 6-17. If R66 is readjusted, the index-to-quadrature relationship will be altered; therefore it will be necessary to repeat the Test Procedure in Paragraph 6.9.8.

(7) Repeat test procedure in Paragraph 6.9.9.2 using Steps 2 through 6 in Table 6-4.

NOTE

If the adjustment cannot be achieved, replacement of the Positioner Carriage or the Servo PCBA may be required.

Table 6-4

Repetitive Track Seek Settings for Overshoot and Settling Response Tests

Step	Exerciser Track-Seek Range	Oscilloscope Time Base	Seek-Time Limits
1	000—001	5 msec/div	10 msec
2	200—201	5 msec/div	10 msec
3	404—405	5 msec/div	10 msec
4	000—134	5 msec/div	40 msec
5	000—405	10 msec/div	65 msec
6	Increment	2 msec/div	10 msec

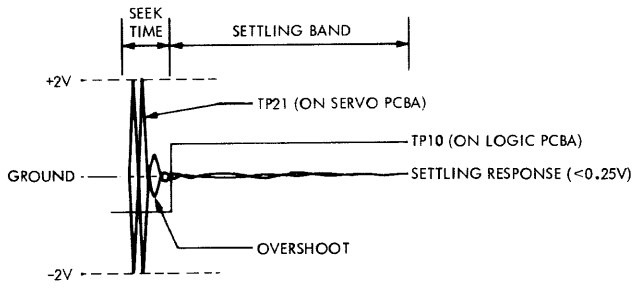


Figure 6-16. X + 0 Overshoot and Settling Response Waveforms

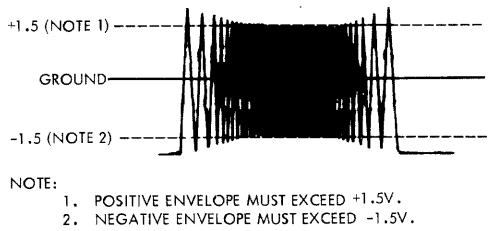


Figure 6-17. X + 90 Waveform for Long Track Seeks

6.10 PERFORMANCE CHECKS

The performance checks detailed in this section should be made after making any positioner adjustments. These checks ensure that the access and settling time of the drive meet the design specifications.

6.10.1 SERVO AND POSITIONER TEST

The tests used to verify the integrity of the position transducer signals, and to confirm the calibration adjustment of the Servo PCBA potentiometers are given in Paragraph 6.9.2, Dynamic Adjustments, and Paragraph 6.9.9, Overshoot and Settling Response. These procedures should be performed after making any mechanical or electrical adjustments or alterations to the Servo PCBA or positioner.

6.10.2 SPINDLE SPEED ACCURACY TEST

This test verifies the spindle speed control accuracy and is a functional integrity check of the control loop.

6.10.2.1 Test Configuration

(1) Apply power to the drive.
(2) After the SAFE indicator becomes illuminated, insert a disk cartridge.
(3) Actuate the RUN/STOP switch once and observe that the drive comes to READY in approximately 110 seconds.
(4) Connect an electronic counter to TP7 (IIPXD) on the Logic PCBA using an X10 oscilloscope probe.
(5) Use TP15 on the Logic PCBA as a ground reference.
(6) Set the counter as follows.
- Period measurement with 1 μsec (1 MHz) time base.
- Trigger at maximum readable sampling rate (use negative slope, if applicable).

6.10.2.2 Test Procedure

The minimum and maximum readings obtained during a 30-second observation should be within the spindle speed limits, as follows.

☐ 1500 rpm models
- 39,600 μsec (minimum)
- 40,400 μsec (maximum)

☐ 2400 rpm models
- 24,750 μsec (minimum)
- 25,250 μsec (maximum)

6.10.2.3 Adjustment Procedure

If the spindle speed requirements are not as specified, perform the ac motor speed control adjustment procedure detailed in Paragraph 6.6.3.

6.11 SECTOR PHASE-LOCK-LOOP ADJUSTMENT

The sector phase-lock-loop adjustment establishes the correct relationship between the phase-lock-pulse signal and the Voltage Controlled Oscillator (VCO) countdown signal. This relationship is shown in Figure 6-18.

NOTE

Each signal should be of the same frequency but 90° out of phase, and should correspond on a cycle-to-cycle basis.

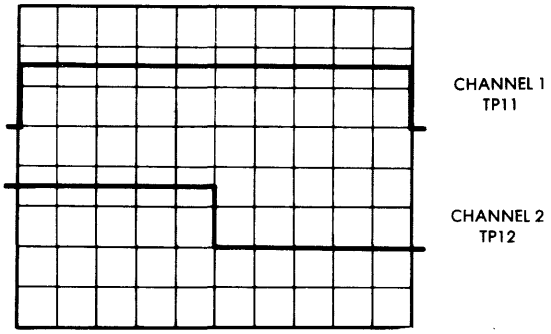


Figure 6-18. Quadrature Relationship Between Sector Phase-Lock-Loop Square Waves

6.11.1 TEST CONFIGURATION

(1) Set oscilloscope as follows.
- Set vertical sensitivity of both channels to 2v per division.
- Set channel select switch to the Chopped mode.
- Trigger internal from Channel 1; use positive trigger mode.
- For 1500 rpm drives, set the sweep at 0.5 msec per division, for 2400 rpm drives, set the sweep rate at 0.2 msec per division.

(2) Connect test probe ground clips to TP2 on the Logic PCBA.

(3) Connect Channel 1 test probe to TP11 on the Logic PCBA.

(4) Connect Channel 2 test probe to TP12 on the Logic PCBA.

(5) Apply power to the drive. When the SAFE indicator becomes illuminated, insert a disk cartridge. Depress the RUN/STOP switch once and allow the drive to come Ready as indicated by the READY indicator being illuminated.

NOTE

A square wave should be observed on Channels 1 and 2 as the drive comes up to speed.

6.11.2 TEST PROCEDURE

(1) Adjust Channel 1 trigger to display the low-to-high transition waveform. Adjust the sweep rate and horizontal position controls to position the leading and trailing edge of the waveform exactly 10 divisions apart. Refer to Figure 6-18.

(2) Observe the waveform on Channel 2. The transition edge should occur at the center vertical graticule line within ± 1/2 of a major division. Refer to Figure 6-18.

NOTE

This relationship is specified for an ambient (room) temperature of 23 ± 5° C (73.4 ± 9° F).

(3) If the relationship is not correct, and the spindle speed accuracy has been verified, perform the adjustment procedure detailed in Paragraph 6.11.3.

6.11.3 ADJUSTMENT PROCEDURE

(1) Adjust the Sector Phase Lock Loop centering potentiometer R47 on the Logic PCBA to position the transition edge of the waveform on Channel 2 (TP12) to the center vertical graticule line.

(2) Refer to Figure 6-18 for the correct positioning of the waveform.

NOTE

This adjustment should be made at a room temperature of 23 ± 5° C (73.4 ± 9° F).

6.12 READ DECODE CIRCUIT ADJUSTMENTS

Read decode test and adjustment procedures for 2200 bpi models (Read/Write Assembly No. 108141) are contained in Paragraphs 6.12.1 through 6.12.3; all test points are located on the Read/Write PCBA unless otherwise specified.

NOTE

The oscilloscope time base must be calibrated either via exterior calibration device or using the 10 MHz oscillator on the Logic PCBA.

6.12.1 RPN PULSEWIDTH ADJUSTMENT

6.12.1.1 Test Configuration

(1) Remove the interface connector and Terminator PCBA from connector J101 and J102 on the Logic PCBA.
(2) Connect a disk exerciser having read/write capability to J101 or J102 on the Logic PCBA.
(3) Apply power to the drive. Observe that the READY indicator is illuminated; allow a 5-minute warmup period.
(4) Write an all-zeros pattern via the disk exerciser.
(5) Connect oscilloscope Channel 1 probe to TP9. Connect the test probe ground clip to ground reference TP1.
(6) Position sweep trace 1 division below centerline of graticule.
(7) Set oscilloscope Channel 1 sensitivity to 1v per division.
(8) Set sync to internal, normal mode.
(9) Set oscilloscope to trigger on the positive slope of RPN.
(10) Set oscilloscope sweep to 0.1 μsec per division.

6.12.1.2 Test Procedure

(1) Establish test configuration described in Paragraph 6.12.1.1.
(2) Observe RPN waveform on oscilloscope Channel 1 (TP9) as shown in Figure 6-19.
(3) Adjust oscilloscope so that the leading edge of the RPN coincides with the center graticule line.
(4) Press the X10 MAG switch on oscilloscope to display 10 nsec per division.
(5) Measure RPN pulsewidth at the 1v level on oscilloscope centerline.

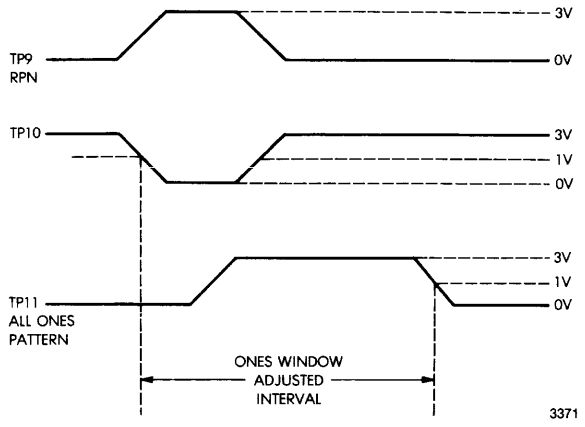


Figure 6-19. Read Pulse Narrow / 'Ones' Window

(6) Acceptable limits:

- ☐ 1500 rpm
  - 50 nsec (minimum)
  - 60 nsec (maximum)
- ☐ 2400 rpm
  - 40 nsec (minimum)
  - 50 nsec (maximum)

6.12.1.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustment is performed.

(1) Establish test configuration detailed in Paragraph 6.12.1.1.

(2) Adjust R69 on the Read/Write PCBA to 55 nsec (for 1500 rpm) or 45 nsec (for 2400 rpm).

6.12.2 'ONES' WINDOW SETTING

6.12.2.1 Test Configuration

(1) Remove the interface connector and Terminator PCBA from connector J101 on the Logic PCBA.

(2) Connect a disk exerciser having read/write capability to J101 on the Logic PCBA.

(3) Apply power to the exerciser and the drive. Observe that the READY indicator is illuminated; allow a 5-minute warmup period.

(4) Write an all-zeros pattern via the disk exerciser.

(5) Connect oscilloscope Channel 1 probe to TP10. Connect the test probe ground clip to ground reference TP1.

(6) Position sweep trace 1 division below centerline of graticule.

(7) Set oscilloscope Channel 1 sensitivity to 1v per division.

(8) Set sync to internal, normal mode, on Channel 1, and trigger on the negative slope.

(9) Set oscilloscope to trigger on the positive slope of RPN.

(10) Connect oscilloscope Channel 2 probe to TP11. Connect the test probe ground clip to ground reference TP1.

(11) Position sweep trace 1 cm below centerline of graticule.

(12) Set oscilloscope Channel 2 sensitivity to 1v per division.

6.12.2.2 Test and Adjustment Procedure (Long)

(1) Observe 'ones' window on oscilloscope Channel 2 (TP11) as shown in Figure 6-19.

(2) Measure the time between the leading edge of RPN TP10 to trailing edge of 'ones' window TP11.

(3) If the pulsewidth is not within adjusted tolerance listed in Table 6-5, adjust R83 for the specified value.

6.12.2.3 Test and Adjustment Procedure (Short)

(1) Write all-ones pattern via the disk exerciser.

(2) Observe 'ones' window on oscilloscope Channel 2 (TP11) as shown in Figure 6-19.

(3) Measure the time between the leading edge of RPN TP10 to trailing edge of 'ones' window (TP11).

(4) If the pulsewidth is not within adjustment tolerance listed in Table 6-5, adjust R79 for the specified value.

Table 6-5
RPN 'Ones' Window Pulsewidth Values

Speed	Zeros	Ones	Adjustment Tolerance
1500 rpm	485 nsec	445 nsec	± 8 nsec
2400 rpm	300 nsec	270 nsec	± 5 nsec

6.12.3 DATA AND CLOCK PULSEWIDTH ADJUSTMENT

6.12.3.1 Test Configuration

(1) Remove the interface connector and terminator PCBA from connector J101 and J102 on the Logic PCBA.
(2) Connect a disk exerciser having read/write capability to J101 on the Logic PCBA.
(3) Apply power to the exerciser and the drive. Observe that the READY indicator is illuminated; allow a 5-minute warmup period.
(4) Write an all-ones pattern via the disk exerciser.
(5) Connect oscilloscope Channel 1 probe to TP12 (Read Clock). Connect the test probe ground clip to ground reference TP1.
(6) Position sweep trace 1 cm below centerline of graticule.
(7) Set oscilloscope Channel 1 sensitivity to 1v per division.
(8) Set sync to internal, normal mode.
(9) Set oscilloscope to trigger on the negative slope of Channel 1.
(10) Connect oscilloscope Channel 2 probe to read data TP13. Connect the test probe ground clip to ground reference TP1.
(11) Position sweep trace 1 division below centerline of graticule.
(12) Set oscilloscope Channel 2 sensitivity to 1v per division.

6.12.3.2 Test Procedure

(1) Observe Read Data TP13 (and Read Clock TP12) on oscilloscope Channels 1 and 2, respectively, as shown in Figure 6-20.
(2) Measure and note the pulsewidth.
(3) Acceptable limits:
- ☐ 1500 rpm
  - 130 nsec (minimum)
  - 170 nsec (maximum)
- ☐ 2400 rpm
  - 100 nsec (minimum)
  - 120 nsec (maximum)

6.12.3.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustment is performed.

(1) Establish test configuration detailed in Paragraph 6.12.3.1.
(2) Adjust R86 (Read Data TP13) or R82 (Read Clock TP12) for the correct timing within the acceptable limits.

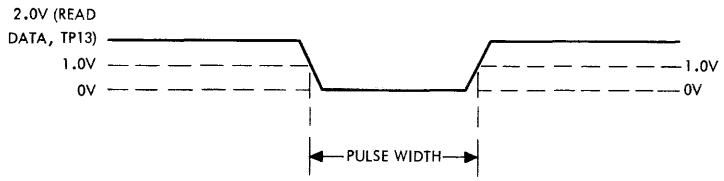


Figure 6-20. Read Clock/Read Data Pulsewidth

6.12.4 SQUARING AMPLIFIER (U2) BALANCE ADJUSTMENT

6.12.4.1 Test Configuration

(1) Disconnect P310 on Read/Write PCBA.
(2) Connect DVM (2v dc range) between TP4 and TP5 on the Read/Write PCBA.
(3) Apply power to the drive.

6.12.4.2 Test Procedure

(1) Measure dc voltage differential between TP4 and TP5.
(2) Acceptable limits:
- 0.0v + 0.01v (maximum)
- 0.0v − 0.01v (minimum)

6.12.4.3 Adjustment Procedure

(1) Adjust R59 to zero volts between TP4 and TP5.
(2) Reconnect P310 on the Read/Write PCBA.

6.13 TEMPERATURE COMPENSATION

The following paragraphs describe test configurations and test procedures for the Temperature Compensation PCBA. There are no adjustments for this PCBA.

6.13.1 TEMPERATURE COMPENSATION TESTS

The Temperature Compensation PCBA operates in conjunction with two thermistors mounted in the area of the removable disk and fixed disk(s). Thus, a signal is provided which is proportional to the temperature difference between the two temperature monitored areas and offsets the heads accordingly.

NOTE

All test points referred to in Paragraph 6.13 are located on the Temperature Compensation PCBA unless otherwise specified.

6.13.1.1 Test Configuration

(1) Prepare the drive to receive a disk cartridge as detailed in Paragraph 3.3.
(2) Insert the test disk cartridge.
(3) Operate the drive in the Ready mode for a minimum of 15 minutes.

6.13.1.2 Test Procedure

(1) Using a digital voltmeter, connect the positive lead to TP and the common test lead to TP8 (ground).
(2) Acceptable limits:
- + 0.1v (maximum)
- − 0.1v (minimum)

(3) If the acceptable limits of the voltage at TP2 are not met, continue to (4) below.

(4) Place a temperature probe between the upper two heads adjacent to the head-lift tower and allow 1 minute for temperature stabilization.

NOTE

Temperature measuring equipment should have a range from 20°C to 31°C (68°F to 87.8°F) with an error limit not greater than +0.5°C (+1°F).

(5) Using the digital voltmeter, move the positive lead to TP4 and keep the common test lead at TP8 (ground).

(6) Monitor the voltage on TP4 and note the reading on the temperature probe.

(7) Use the temperature probe reading to determine the RP4 voltage value graphed in Table 6-6.

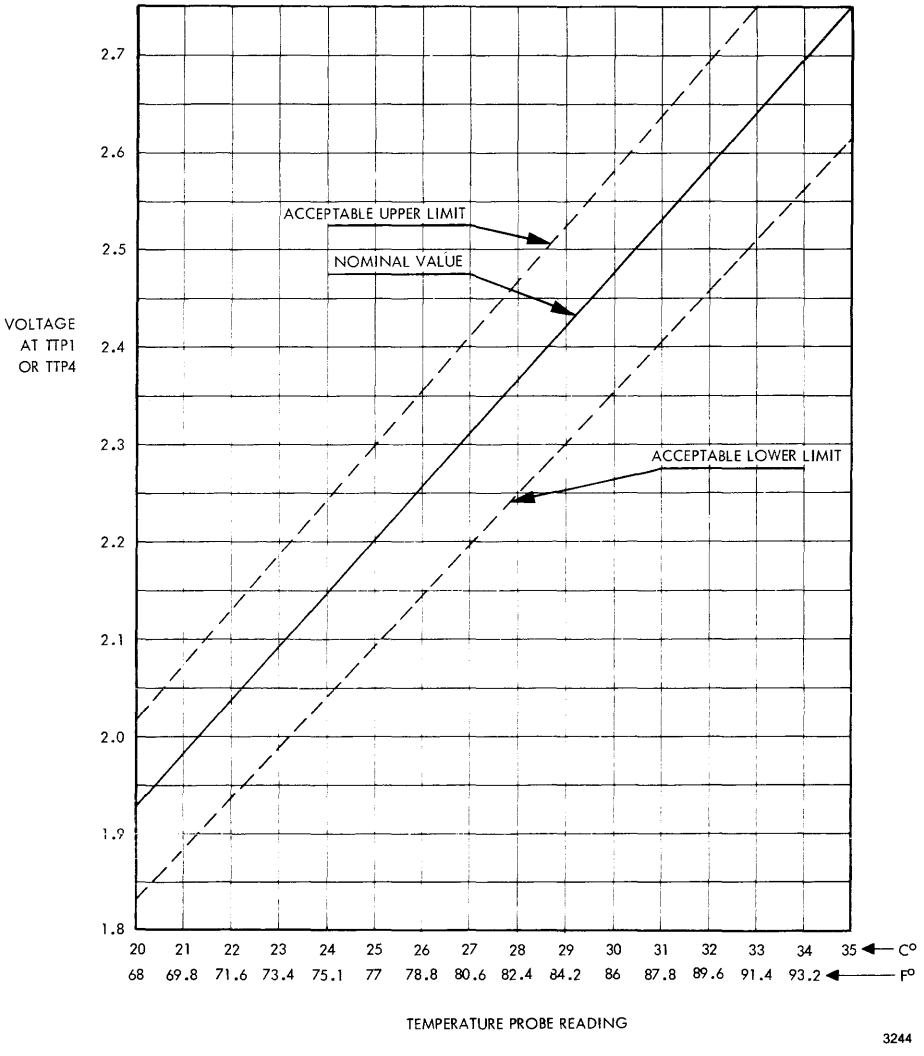
(8) Acceptable limits are indicated for each temperature probe reading in Table 6-6.

(9) Repeat Steps (5) through (8) using TP1 instead of TP4.

(10) If the test point voltage is not within acceptable limits, begin troubleshooting techniques with U1 or U3 and work backwards to U2.

Table 6-6

Output from Thermistors TP1 and TP4 Versus Temperature



6.14 CE ALIGNMENT PROCEDURE

NOTE

The steps for temperature compensation (Paragraph 6.13) must be performed before any CE alignment is attempted.

The circumferential and radial alignment of the disk drive is accomplished using a special CE disk cartridge that can usually be identified by a special top color and/or label. The CE cartridge contains pre-recorded cylinders which are used to adjust the read/write head radial alignment and the index-to-data circumferential alignment.

CE alignment procedures for a front load disk drive differ from those used with a top load model. Primarily, the differences are due to the top and front load CE cartridge configurations. The alignment tracks used are at different locations and the read data patterns for radial alignment are different. Therefore, separate CE alignment procedures are given for front and top load drives.

Paragraphs 6.14.1 and 6.14.2 provide descriptions of front and top load CE disk cartridges, respectively; Paragraph 6.14.3 describes the environmental stabilization requirements. The test configuration for top and front load drives is given in Paragraph 6.14.4.

Paragraphs 6.14.5 and 6.14.6 describe the radial and circumferential alignment procedures, respectively, for front load models; Paragraphs 6.14.7 and 6.14.8 describe the radial and circumferential alignment procedures, respectively, for top load models.

6.14.1 FRONT LOAD CE DISK CARTRIDGE

The front load CE disk cartridge contains two pre-recorded cylinders (190 and 200) which are used during adjustment procedures to the head/arm carriage assembly and to the upper photoelectric sensor.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT CYLINDERS 180 THROUGH 210 ARE NOT INADVERTENTLY WRITTEN ON; WRITING ON THESE CYLINDERS WILL CAUSE THE PRE-RECORDED DATA TO BE DESTROYED.

6.14.1.1 Cylinder 200

Cylinder 200 is used for adjustment of the head/arm location. The alignment pattern for front load is identical to that for top load models; refer to Paragraph 6.14.2.1 for description.

6.14.1.2 Cylinder 190

This cylinder has a single flux transition marker recorded approximately 180 degrees from the centerline of the index slot. To assist in identifying this marker, a burst of flux transitions occurs 10 μsec after the marker.

Cylinder 190 is used for circumferential adjustment of the upper photoelectric sensor. Information recorded on this cylinder is similar to that recorded on the top load CE cartridge in cylinder 010.

6.14.2 TOP LOAD CE DISK CARTRIDGE

The top load CE disk cartridge contains two pre-recorded cylinders (010 and 146) which are used during adjustment procedures to the head/arm carriage assembly and to the upper magnetic transducer.

CAUTION

WHEN USING 200 TPI CE PACKS, ENSURE THAT CYLINDERS 008 THROUGH 012 AND 142 THROUGH 150 ARE NOT INADVERTENTLY WRITTEN ON. WRITING ON THESE CYLINDERS WILL CAUSE PRE-RECORDED DATA TO BE DESTROYED.

6.14.2.1 Cylinder 146

For 200 tpi CE packs, cylinder 146 is used for adjustment of the head/arm location. Two concentric cylinders, either side of cylinder 146, are spaced 0.025 mm (0.010 inch) apart and are eccentric to the center of rotation of the disk by 0.0381 mm (0.0015 inch). The cylinders are written with slightly different frequencies. Radial adjustment of the head is carried out by monitoring the beat frequency at cylinder 146. A head that is correctly centered over track 146 gives an oscilloscope trace with an equal amplitude 2-lobe fringe pattern. Due to the amount of eccentricity, when a head is reading the pattern and the head is misaligned from the true cylinder radius, a lobed envelope pattern will be prodcued.

6.14.2.2 Cylinder 010

For 200 tpi CE packs, cylinder 010 is used for circumferential adjustment of the upper magnetic transducer. The cylinder has a single flux transition marker recorded approximately 180 degrees from the centerline of the index notch. To assist in identifying this marker, a burst of flux transitions occurs 10 μsec after the marker.

6.14.3 CE CARTRIDGE STABILIZATION

Prior to attempting alignment, the CE cartridge must be conditioned in the same environment in which the drive (to be aligned) is located. This conditioning must not be less than 2 hours. In addition to this stabilization period, the CE cartridge must be operated for at least 30 minutes with the drive in the Run condition; this allows the cartridge to reach the proper temperature for performing the alignment.

6.14.4 TEST CONFIGURATION

The following procedure is used to establish the test configuration for CE alignment of top and front load drives.

(1) Remove the cover from the drive and open the circuit boards to their fully extended positions.

(2) Remove the I/O cable and terminator PCBA from interface connectors J101 and J102 on the Logic PCBA.

(3) Connect a disk exerciser with read/write capabilities to interface connector J101 or J102.

(4) Set the upper disk Write Protect switch to the ON position.

(5) Connect the drive to ac power and set the ON/OFF switch to ON.

(6) When the SAFE indicator is illuminated, insert the special CE disk cartridge.

(7) Depress the RUN/STOP switch once to allow the drive to become Ready. Allow the drive to warm up for at least 30 minutes before proceeding.

(8) Disconnect the emergency unload capacitor connector P206 from the Servo PCBA, thereby deactivating the emergency unload system. If the disk speed slows noticeably due to loss of ac power or other malfunction, the heads must be manually unloaded.

NOTE

It is the responsibility of the person performing the CE alignment to perform the emergency unload function when P206 is disconnected.

(9) A dual trace oscilloscope having a 50 MHz vertical bandwidth or greater is required to perform CE alignment procedures.

NOTE

Depending on the type of oscilloscope utilized and its grounding arrangement, it may be necessary to use a differential measurement of the Read/Write PCBA signal in lieu of a single channel method. This will usually be the case when a ground loop exists between the scope and the drive. Refer to the applicable scope manual for differential measurement setup, if necessary.

(10) One X1 probe is required for single-ended measurement; two X1 probes are required for differential measurement.

CE alignment procedures for front load drives are outlined in Paragraphs 6.14.5 and 6.14.6; top load alignment procedures are outlined in Paragraphs 6.14.7 and 6.14.10.

6.14.5 RADIAL ALIGNMENT — FRONT LOAD DISK DRIVES

6.14.5.1 Test Procedure

The test configuration detailed in Paragraph 6.14.4 must be performed prior to performing this procedure. Values given in this procedure are for 1500 and 2400 rpm front load drives.

(1) Set up oscilloscope as follows.
- Connect oscilloscope vertical input to TP2 on the Read/Write PCBA (see Figure 5-5); use TP1 for ground reference.
- Set vertical sensitivity to 50 mv per division and select the ac input mode.
- Connect an X10 test probe from the external trigger input of the oscilloscope to TP7 (Index) on the Logic PCBA.
- Use external trigger and normal sync, ac coupled, on the negative trigger slope.
- Set sweep rate to 5 msec per division.

(2) Set exerciser to position the heads to cylinder 200.

(3) Select head 0 (upper surface of upper platter).

(4) Observe the waveform at TP2 on the Read/Write PCBA and compare the waveform to the relevant waveform shown in Figure 6-21 (when using the IBM or 3M-type CE cartridge), or Figure 6-22 (when using the CDC-type CE cartridge).

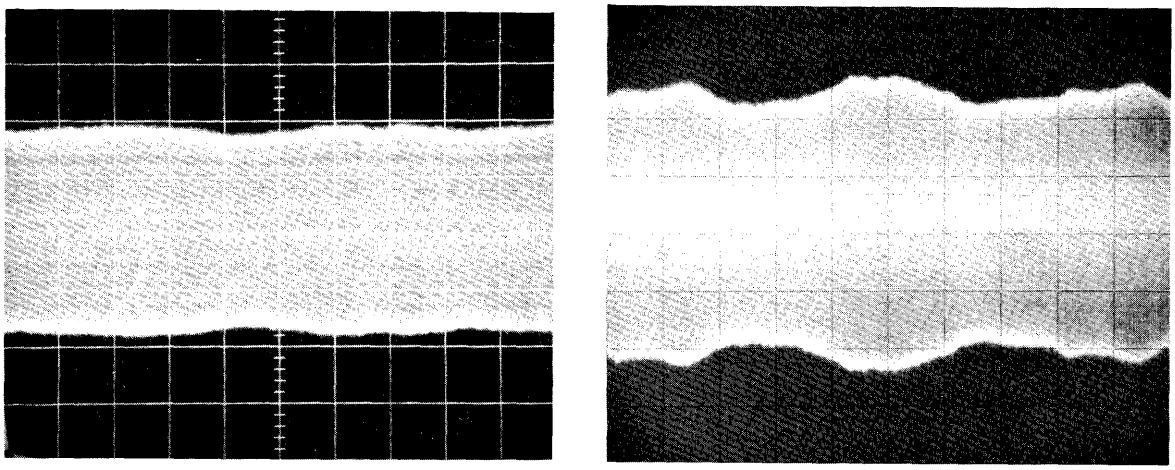
(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.14.5.3.

(6) Change vertical sensitivity to 20 mv per division and change vertical positioning to observe the edge of the waveform envelope.

(7) For each head selected, observe the edge of the waveform and compare it to the relevant waveform shown in Figure 6-23.

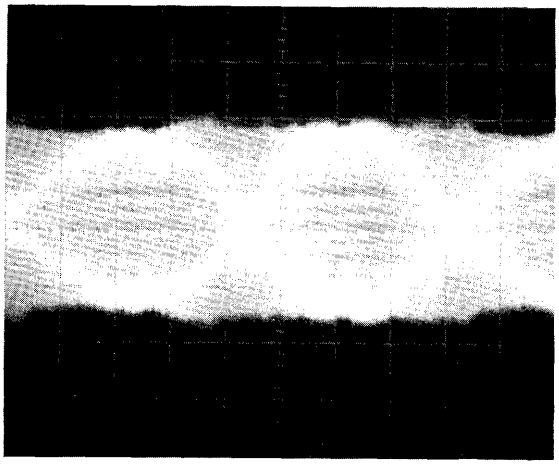


2147

IBM CE Cartridge

3M CE Cartridge

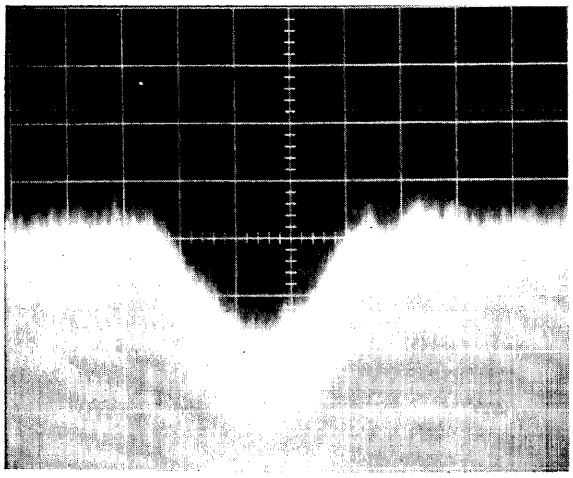
Figure 6-21. Approximately Aligned Heads, Front Load Disk Drive



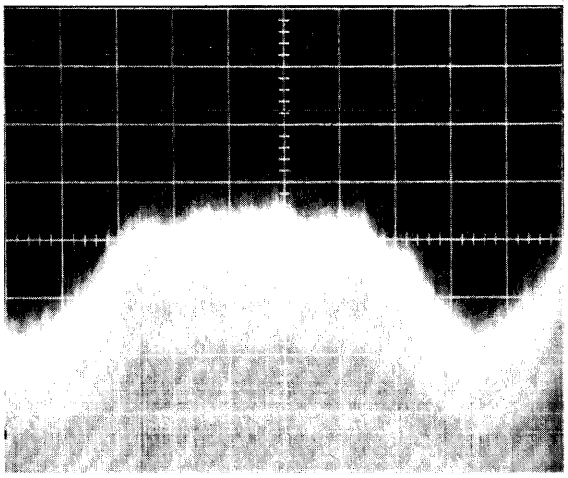
CDC/CFI Cartridge

2148

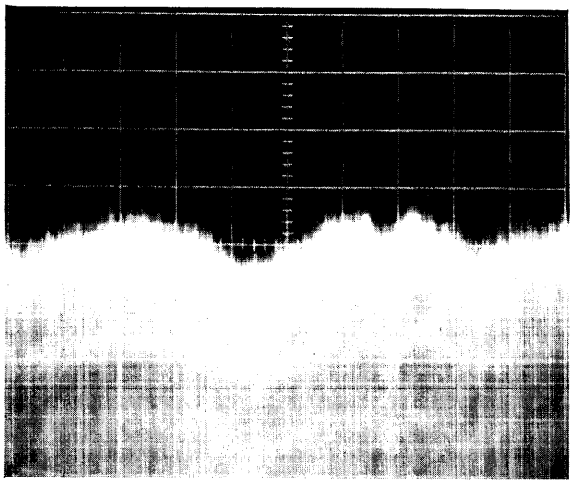
Figure 6-22. Head Aligned, Front Load Disk Drive



Heads Too Far Back



Heads Too Far Forward



2280

Correct Alignment

Figure 6-23. Head Alignment (IBM CE Cartridge) Track 200, Front Load Disk Drives

6.14.5.2 Adjustment Procedure

If radial alignment is required, perform the following adjustment procedure.

(1) Allow the drive to stabilize in the Ready mode for 30 minutes (minimum).

(2) Maintain the oscilloscope setting established in Paragraph 6.14.5.1, Step (1), except change Channel 1 sensitivity to 50—100 mv per division; perform Steps (2) through (7).

(3) Observe the waveforms shown in Figure 6-24 and determine which direction the heads must be moved.

(4) Locate the two radial positioning screws on the selected head.

(5) By loosening one screw and tightening the other, position the selected head until the waveform in Figure 6-24(C) is obtained. Without disturbing the adjustment, tighten both screws.

(6) Align both heads in the same manner.

(7)* Using the exerciser, position the heads to cylinder 000, then reposition them to cylinder 210 and observe that the waveform still appears as in Figure 6-24(C). This ensures that the heads have not been aligned to cylinder 210 which is a duplicate of cylinder 200.

NOTE

If a head cannot be adjusted to obtain the minimal lobe pattern, the head may not be flying correctly. This condition can be caused by either a dirty disk or head, incorrect head load force, or damaged head(s).

6.14.6 CIRCUMFERENTIAL ALIGNMENT — FRONT LOAD

*6.14.6.1 Test Procedure

Values given in this test procedure are for 1500 rpm front load disk drives.

(1) Set oscilloscope as follows.

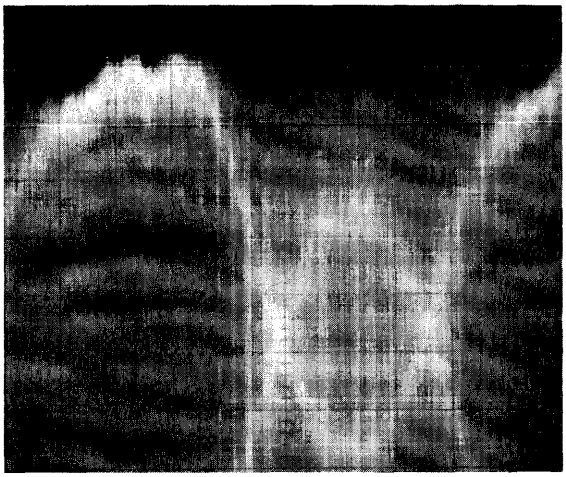
- Connect oscilloscope Channel 1 vertical input to TP2 on the Read/Write PCBA (see Figure 5-5).
- Connect oscilloscope Channel 1 ground to TP1 on the Read/Write PCBA.
- Set Channel 1 vertical sensitivity to 1v per division.
- Connect oscilloscope Channel 2 X10 probe to TP7 on the Logic PCBA.
- Set Channel 2 vertical sensitivity to 2v per division.
- Set Channel Select to Alternate mode.
- Use internal sync and negative sync on the leading edge of Index signal on Channel 2.
- Set the sweep rate to 5 μsec.

NOTE

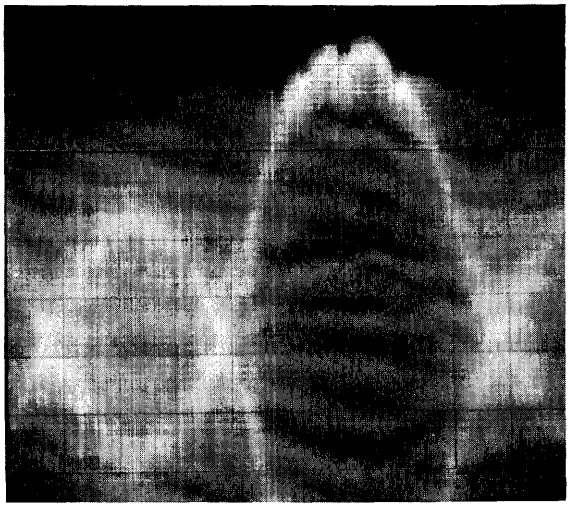
Depending on the type of oscilloscope utilized and its grounding arrangement, it may be necessary to use a differential measurement of the Read/Write PCBA signal in lieu of a single channel method. This will usually be the case when a ground loop exists between the scope and the drive. Refer to the applicable scope manual for differential measurement setup, if necessary.

- Adjust horizontal position to place start of sweep on left-most vertical graticule line. This will establish a time-zero reference to be used in lieu of actual viewing of the negative transition of the index pulse.

*Only applicable on cartridges with dual circumferential tracks.



A. Heads Too Far Back



B. Heads Too Far Forward

C. Heads Aligned

Figure 6-24. Radial Alignment

Take care not to disturb the horizontal position during the measurement. (This technique assumes that the start of the sweep corresponds to the triggering of the sweep; verify this if in doubt.)

(2) Set exerciser to position heads to cylinder 190.

(3) Select head 0.

(4) Observe the waveform at TP2 on the Read/Write PCBA (see Figure 5-5) with respect to the leading edge of the Index signal (time-zero reference).

(5) The first pulse of the waveform at TP2 should occur 30 ± 5 μsec from the negative-going edge of the Index signal (time-zero reference). See Figure 6-25.

(6) Select head 1.

(7) Observe the waveform at TP2. The first pulse should occur 30 ± 5 μsec from the negative-going edge of the Index signal (time-zero reference).

(8) Alternately switch between heads 0 and 1 and observe the relative displacement of the pulse for each head. The total displacement (separation) between pulse positions must be 10 μsec or less. See Figure 6-26.

6.14.6.2 Adjustment Procedure

If circumferential alignment is required, perform the following steps.

NOTE

If the separation between pulses, as measured in Step (8), Paragraph 6.14.6.1, exceeds 10 μsec, remove power from the drive and remove upper two heads. Check for foreign material or burrs on head seating surfaces. Replace one or both heads if a head problem is suspected. Reinstall heads and perform radial alignment procedure.

(1) Maintain the oscilloscope and exerciser according to Paragraph 6.14.6.1, Steps (1) and (2).

(2) Insert a Phillips-head screwdriver into the circumferential alignment adjusting screw (viewed facing the front of the drive, the screw is located under the cartridge receiver, toward the right).

NOTE

It may be necessary to lift the receiver slightly so the tool can be inserted.

CAUTION

CARE MUST BE TAKEN WHEN LIFTING THE RECEIVER; LIFTING IT TOO HIGH WILL CAUSE THE SPINNING DISK TO COME INTO CONTACT WITH THE CARTRIDGE HOUSING.

NOTE

Rotation of the tool in the CCW direction increases the pulse delay from Index.

(3) Select either head 0 or 1 and, while observing the waveform at TP2 on the Read/Write PCBA (see Figure 5-5), turn the adjusting screw until the first pulse after the falling edge of Index (Channel 2) falls within the 30 ± 5 μsec specifications.

(4) Select the other head and ensure that the specification detailed in Step (3) is met. A compromise adjustment may be required to meet the 30 ± 5 μsec requirement for both heads; see Figure 6-26.

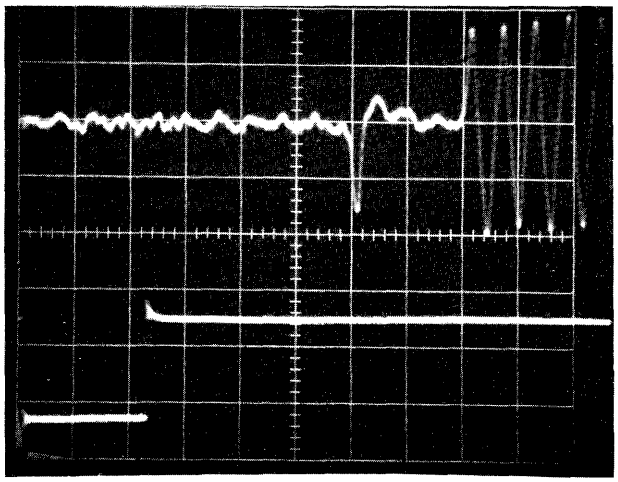


Figure 6-25. Circumferential Alignment, Front Load Drives
(Not to Scale)

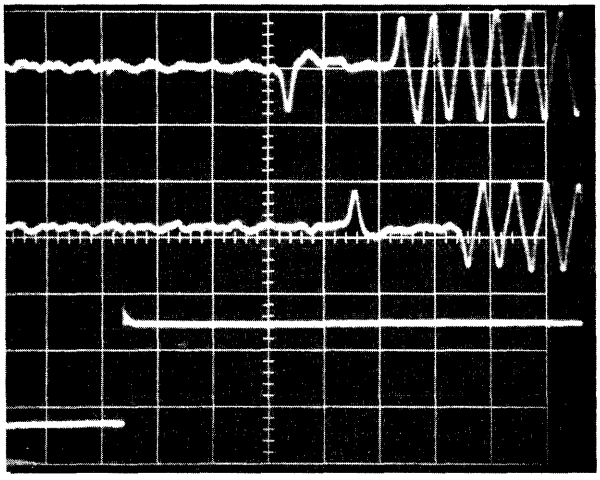


Figure 6-26. Compromise Circumferential Alignment, Front Load Drives
(Not to Scale)

(5) Turn the Phillips-head screwdriver slightly in the opposite direction of the last turn to cause the adjusting screw to relax the force on the mechanism (i.e., mid-range of the screw backlash).

(6) Recheck heads 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (3), (4), and (5), as necessary.

(7) Remove the Phillips-head screwdriver and bring the drive to the SAFE condition, then remove the CE disk cartridge. Return the drive to its former configuration. Do not forget to reset the write protect switch if the protect is not desired, and reconnect P206 on the Servo PCBA.

6.14.7 RADIAL ALIGNMENT — TOP LOAD

Paragraph 6.14.7.1 describes the test procedure for radial alignment of top load drives.

6.14.7.1 Test Procedure

(1) Set up oscilloscope as follows.

- Connect oscilloscope vertical input to TP2 on the Read/Write PCBA (see Figure 5-5).
- Connect oscilloscope ground to TP1.
- Set vertical sensitivity to 50 mv per division and select the ac input mode.
- Connect an X10 test probe from the external trigger input of the oscilloscope to TP7 (Index) on the Logic PCBA.
- Use external trigger, and normal sync, ac-coupled on the negative trigger slope.
- Set sweep rate to 5 msec per division.

(2) Set the exerciser to position heads to cylinder 146.

(3) Select head 0.

(4) Observe the waveform at TP2 on the Read/Write PCBA (Figure 5-5) and compare it to the waveform shown in Figure 6-27.

(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.14.7.2.

6.14.7.2 Adjustment Procedure

If radial alignment is required perform the following procedure.

(1) Set up oscilloscope as follows.

- Connect oscilloscope vertical input to TP2 on the Read/Write PCBA (Figure 5-5); use TP1 for ground reference.
- Set vertical sensitivity to 20 mv per division and select the input ac mode.
- Connect an X10 test probe from the external trigger input of the oscilloscope to TP7 (Index) on the Logic PCBA.
- Use external trigger and normal sync, ac-coupled on the negative trigger slope.
- Set sweep rate to 10 msec per division.

(2) Observe the waveforms shown in Figures 6-28 and 6-29 and determine which direction the heads must be moved.

(3) Locate the two radial positioning screws on the selected head.

(4) By loosening one screw and tightening the other, position the selected head until the waveform of Figure 6-30 is obtained; without disturbing the adjustment, tighten both screws.

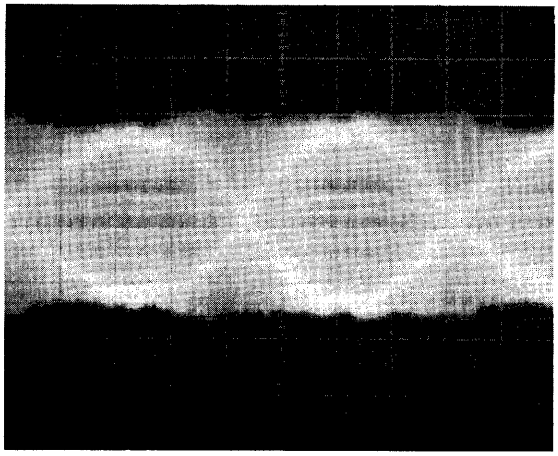


Figure 6-27. Radial Alignment, Head Aligned

Figure 6-28. Heads Too Far Back

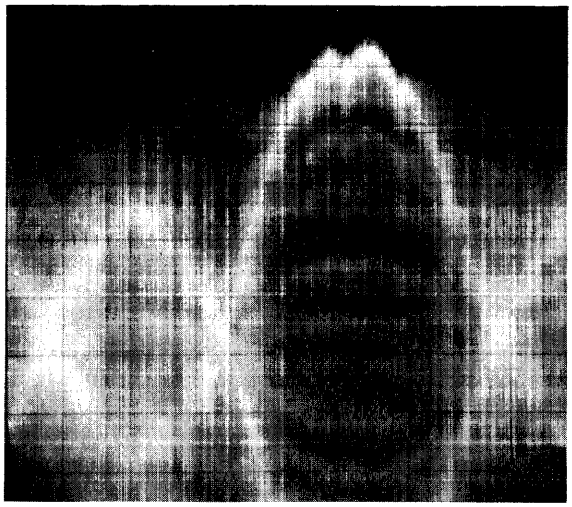


Figure 6-29. Heads Too Far Forward

Figure 6-30. Heads Aligned

(5) Align both heads in the same manner.

(6) Set exerciser to position the heads to cylinder 146.

(7) Select head 0.

(8) Observe the waveform at TP2 on the Read/Write PCBA and compare it to the one shown in Figure 6-30.

(9) Select head 1 and repeat Step (8).

NOTE

If a head cannot be adjusted to obtain the minimal lobe pattern, the head may not be flying correctly. This condition can be caused by either a dirty disk or head, incorrect head load force, or damaged head(s).

6.14.8 CIRCUMFERENTIAL ALIGNMENT — TOP LOAD

6.14.8.1 Test Procedure

(1) Set up oscilloscope as follows.

- Connect oscilloscope Channel 1 vertical input to TP2 on the Read/Write PCBA (see Figure 5-5).
- Connect oscilloscope Channel 1 ground to TP1.
- Set Channel 1 vertical sensitivity to 1v per division.
- Connect oscilloscope Channel 2 X10 probe to TP7 on the Logic PCBA.
- Set Channel 2 sensitivity to 2v per division.
- Set sweep rate to 5 μsec per division.
- Set Channel Select to Alternate mode.
- Use internal sync and negative sync on the leading edge of Index signal on Channel 2.

NOTE

Depending on the type of oscilloscope utilized and its grounding arrangement, it may be necessary to use a differential measurement of the Read/Write PCBA signal in lieu of a single channel method. This will usually be the case when a ground loop exists between the scope and the drive. Refer to the applicable scope manual for differential measurement setup, if necessary.

- Adjust horizontal position to place start of sweep on left-most vertical graticule line. This will establish a time-zero reference to be used in lieu of actual viewing of the negative transition of the index pulse.

  Take care not to disturb the horizontal position during the measurement. (This technique assumes that the start of the sweep corresponds to the triggering of the sweep; verify this if in doubt.)

(2) Set exerciser to position heads to cylinder 010.

(3) Select head 0.

(4) Observe the waveform at TP2 on the Read/Write PCBA (Figure 5-5) with respect to the falling edge of the Index signal (time-zero reference).

(5) The first pulse of the waveform should occur 30 ± 5 μsec from the negative-going edge of the Index signal (time-zero reference). See Figure 6-25.

(6) Select head 1.

(7) Observe the waveform at TP2. The first pulse should occur 30 ± 5 μsec from the negative-going edge of the Index signal (time-zero reference).

(8) Alternately switch between heads 0 and 1 and observe the relative displacement of the pulse for each head. The total displacement (separation) between pulse positions must be 10 μsec or less. See Figure 6-26.

6.14.8.2 Adjustment Procedure

If circumferential alignment is required, perform the following steps.

NOTE

If the separation between pulses, as measured in Step (8), Paragraph 6.14.8.1, exceeds 10 μsec, remove power from the drive and remove upper two heads. Check for foreign material or burrs on head seating surfaces. Replace one or both heads if a head problem is suspected. Reinstall heads and perform radial alignment procedure.

(1) Maintain the oscilloscope and exerciser according to Paragraph 6.14.8.1, Steps (1) and (2).

(2) Insert a Phillips-head screwdriver into the circumferential alignment adjusting screw (viewed facing the front of the drive, the screw is located under the cartridge receiver, toward the right).

(3) Select either head 0 or 1 and, while observing the waveform at TP2 on the Read/Write PCBA (see Figure 5-5), turn the adjusting screw until the first pulse after the falling edge of Index (Channel 2) falls within the 30 ± 5 μsec specifications.

(4) Select the other head and ensure that the specification detailed in Step (3) is met. A compromise adjustment may be required to meet the 30 ± 5 μsec requirement for both heads; see Figure 6-26.

(5) Turn the Phillips-head screwdriver slightly in the opposite direction of the last turn to cause the adjusting screw to relax the force on the mechanism (i.e., mid-range of the screw backlash).

(6) Recheck heads 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (3), (4), and (5), as necessary.

(7) Tighten the locking screw that was loosened in Step (3) above.

(8) Recheck heads 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (2) through (7), as necessary.

(9) Remove the Phillips-head screwdriver and reinstall the bezel.

6.15 CARTRIDGE INTERLOCK SYSTEM — FRONT LOAD MODELS

The front load disk drive is protected against physical damage by an electromechanical interlock system. This system, described in Paragraph 3.11, prevents the operator from removing a disk cartridge unless the drive is in the Safe condition, the spindle has stopped rotating, and the heads have been fully retracted. Two solenoids limit the opening of the front door until these conditions have been satisfied.

The interlock system also inhibits the start sequence if a disk cartridge has not been properly inserted by the operator. This condition is sensed by the interlock switch. The interlock is actuated by appropriate logic and driver circuits located on the Servo and Logic PCBAs.

CAUTION

BEFORE ATTEMPTING TO START A FRONT LOAD DISK DRIVE, THE DOOR MUST BE FULLY CLOSED.

6.15.1 CHECKING THE INTERLOCK SYSTEM

Proper adjustment of the interlock system may be verified as follows.

(1) Prepare the drive to receive a disk cartridge as detailed in Paragraph 3.3.

(2) Install an approved disk cartridge as detailed in Paragraph 3.4.1. Depress the RUN/STOP switch.

(3) When the READY indicator is illuminated, pull on the door handle with a force of approximately 10 pounds.

(4) If the unit continues to function normally, as evidenced by continuous illumination of the READY indicator, the interlock system adjustments are within tolerance. If the Ready condition is not maintained, perform the relevant adjustment procedures detailed in Paragraph 6.15.2.

6.15.2 ADJUSTING THE INTERLOCK SYSTEM

6.15.2.1 Test Configuration

(1) Withdraw the drive forward to the full extent of the slides.

(2) Remove the dust cover; refer to Paragraph 2.2, Step (5).

(3) Apply power to the drive and allow it to come to SAFE.

(4) Determine if a cartridge is installed in the drive by following the unloading instructions contained in Paragraph 3.4.2, Steps (1) through (4).

(5) Remove the cartridge from the drive if one is installed.

(6) Remove power from the drive.

6.15.2.2 Solenoid Plunger Clearance Test and Adjustment

When a solenoid plunger is manually depressed, the clearance between the right and left door link arms and the end of each solenoid plunger should measure between 0.040 to 0.060 inch. See Figure 6-31.

Solenoid adjustments are made as follows.

(1) Right-hand solenoid. Back off the two mounting screws and slide the solenoid toward or away from the link arm to decrease or increase the gap as required. Securely tighten solenoid adjusting screws.

(2) Left-hand solenoid. This adjustment is made with the door open using a long shank Phillips screwdriver to loosen the adjusting screws. Slide the solenoid toward or away from the link arm to decrease or increase the gap as required. Securely tighten the adjusting screws.

NOTE

To reach forward adjusting screw, shank of screwdriver must pass between top edge of bezel and left edge of switch bracket. Avoid scratching either surface.

6.15.2.3 Interlock Switch Test

The cartridge interlock switch is a leaf-actuated snap-action switch that is part of the upper sector sensor assembly attached to the top of the lower disk cover. The actuating leaf arm of the switch extends upward through the front center of the cartridge receiver and contacts the cartridge case.

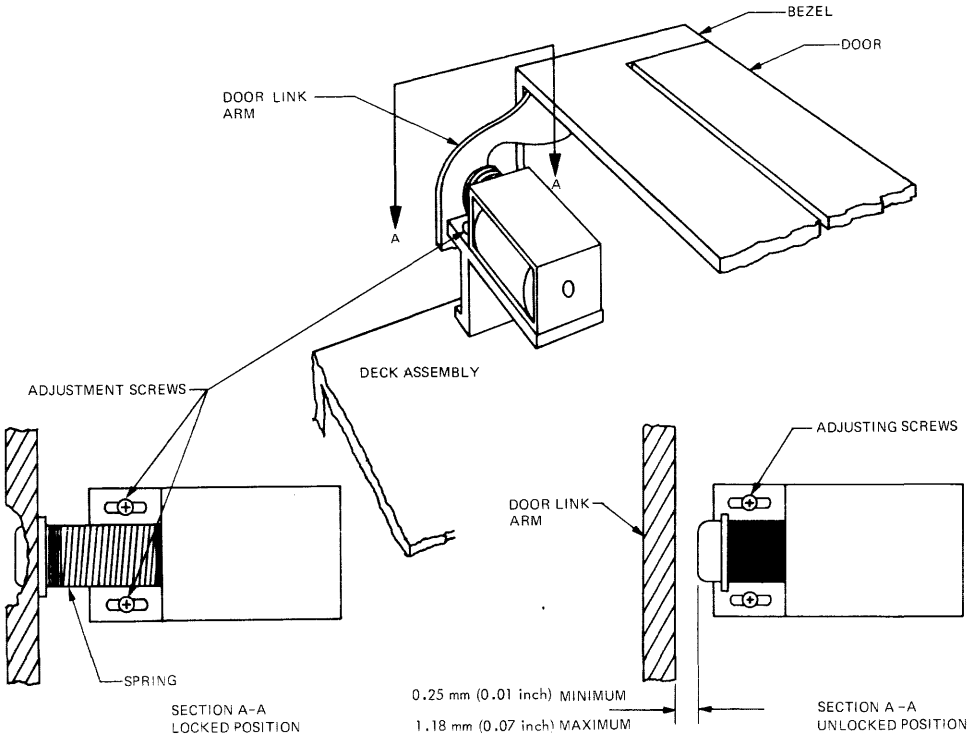


Figure 6-31. Solenoid Location and Clearance

The switch senses the correct location of the cartridge in the drive; this ensures that the cartridge is properly located upon the spindle and is ready for operation. The switch is electrically connected to control circuits on the Logic PCBA via connector P109.

To test for correct operation, perform the following.

(1) Remove power from the drive.
(2) Elevate the Logic and Servo PCBAs to the maintenance position.
(3) Remove connector P109 from the Logic PCBA.
(4) Connect a suitable continuity indicating device, such as an ohmmeter, to pins 1 and 2 of P109.
(5) Apply power to the drive.
(6) When the SAFE indicator becomes illuminated, open the front door and install a disk cartridge.
(7) Slowly close the door and note where the switch establishes continuity.

NOTE

The cartridge must not have completed its travel at this point and should not be completely seated.

(8) Reinstall P109 onto the Logic PCBA.
(9) If the requirements of Step (7) are not met, perform the adjustment procedure contained in Paragraph 6.15.2.4.

6.15.2.4 Interlock Switch Adjustment

(1) Remove the disk cartridge.
(2) Adjust the actuating leaf of the interlock switch by bending the leaf with a pair of long-nose pliers.
(3) Return the disk cartridge into cartridge receiver and perform the test procedure contained in Paragraph 6.15.2.3, Steps (1) through (7).
(4) Open and close the door several times with the disk cartridge in place to ensure reliable operation.
(5) Disconnect the indicating device connected to P109 in Step (4) of Paragraph 6.15.2.3.
(6) Reinstall P109 onto the Logic PCBA.
(7) Lower the Logic PCBA from the maintenance position to the normal operating position.
(8) Replace dust cover and return the drive into enclosure.

6.16 CARTRIDGE INTERLOCK SYSTEM — TOP LOAD MODELS

The top load disk cartridge is protected against physical damage by an electromechanical interlock system. This system, described in Paragraph 3.11, prevents the operator from removing a disk cartridge unless the drive is in the Safe condition, the spindle has stopped rotating and the heads have been fully retracted. It also inhibits the Start sequence when the cartridge has been improperly installed by the operator.

The interlock mechanism is located on the rim of the cartridge adapter assembly and consists of a cartridge lock arm, a snap-action interlock switch, and a solenoid. When properly positioned, the arm and the solenoid prevent cartridge removal. The interlock switch senses when a disk cartridge is properly installed.

In addition to the interlock mechanism, suitable logic and drivers are provided on the Servo and Logic PCBAs to control the system. Electrical connections are made via connector P109 to the Logic PCBA.

6.16.1 CHECKING THE INTERLOCK SYSTEM

Proper adjustment of the interlock system may be verified as follows.

(1) Prepare the drive to receive a disk cartridge as outlined in Paragraph 3.3.

(2) Install a disk cartridge as detailed in Paragraph 3.4.3. Depress the RUN/STOP switch.

(3) When the READY indicator is illuminated, apply approximately a 5-pound torque to the cartridge lock arm in the unlocking direction.

(4) If the drive continues to function normally, as evidenced by continuous illumination of the READY indicator, the interlock system upper limit adjustments are within tolerance.

(5) Actuate the RUN/STOP switch. When the SAFE indicator is illuminated, remove the disk cartridge and reinstall the lower cover of the cartridge, and then lock the arm.

(6) Actuate the RUN/STOP switch. If the solenoid does not lock in place, the interlock system lower limit is within tolerance.

CAUTION

SHOULD THE ARM LOCK, IMMEDIATELY REMOVE THE POWER AND MAKE CORRECTIVE ADJUSTMENTS.

6.16.2 ADJUSTING THE INTERLOCK SYSTEM

6.16.2.1 Test Configuration

(1) Extend the drive fully forward out of the rack; remove the disk cartridge and remove the source of power by disconnecting the line cord.

(2) Remove the dust cover as described in Paragraph 2.2, Step (9). Elevate the Logic PCBA to the maintenance position.

6.16.2.2 Solenoid Stroke Test and Adjustment

Check the stroke adjustment of the solenoid. With the solenoid plunger manually depressed and the lock-arm unlocked, the distance from the end of the plunger to the curved surface of the lock-arm body must be from 0.25 to 1.78 mm (0.01 to 0.07 inch) as shown in Figure 6-33. If adjustment is required, loosen the adjusting screws and position the solenoid body until the proper clearance is obtained.

6.16.2.3 Lock-Arm Travel Test and Adjustment

Check the lock-arm travel by rotating the lock arm to the locked position; attempt to insert a 0.762 mm (0.03 inch) thick feeler gauge between the neck of the lock arm and the adapter casting as shown in Figure 6-32. If the clearance is greater than 0.25 mm, adjust to correct clearance by loosening the retaining screws and sliding the solenoid body laterally across the mounting bosses until the clearance is less than 0.76 mm. After completing the adjustment, determine that the solenoid plunger is not binding against the lock arm body and is free to engage and disengage under its own spring force. Ensure that the stroke adjustment detailed in Paragraph 6.16.2.2 has not changed.

6.16.2.4 Snap Action Switch Test and Adjustment

(1) Remove power from the drive.

(2) Remove P109 from the Logic PCBA.

(3) With a suitable continuity indicating device, monitor the switch closure between pins 1 and 2 in the connector.

(4) Install adapter bowl setup tool, PCC PD Part No. 103619-01, onto the spindle cone. See Figure 6-34.

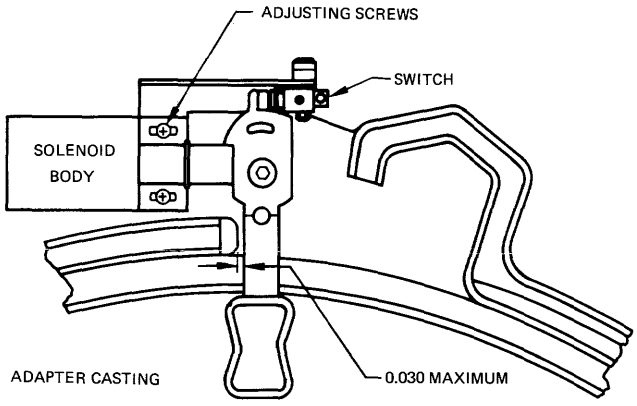


Figure 6-32. Retracted Solenoid Plunger and Lock-Arm Clearance

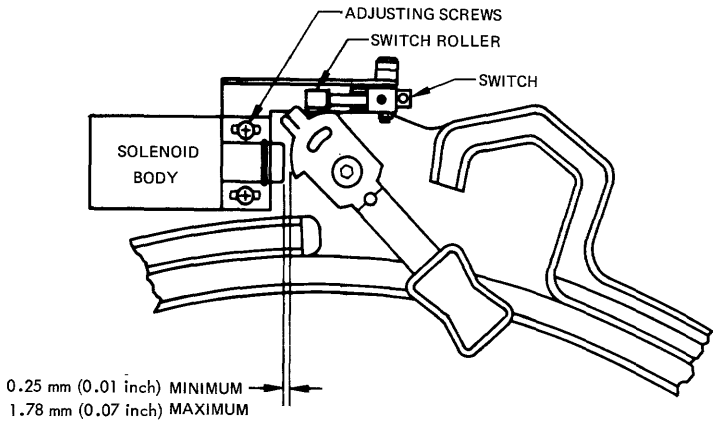


Figure 6-33. Adapter Casting and Lock-Arm Clearance

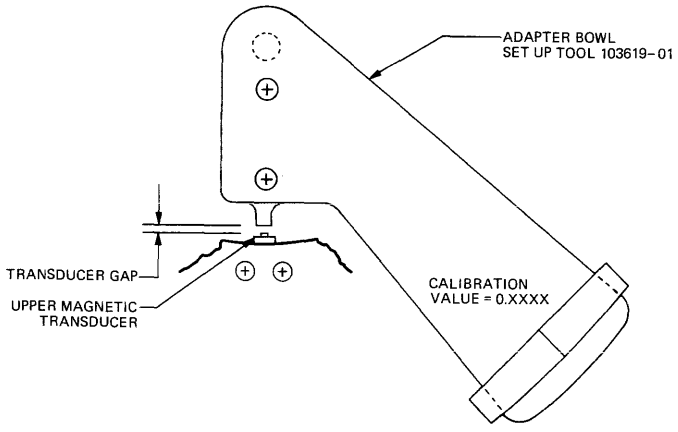


Figure 6-34. Upper Magnetic Transducer Gap

(5) Manually depress the solenoid plunger and rotate the lock arm to the locked position over the NO-GO position marked on the tool. See Figure 6-35. There should be no switch closure observed between pins 1 and 2.

(6) Retract the lock arm and move the tool to the GO position.

(7) Manually depress the solenoid plunger and rotate the lock arm to the locked position over the GO portion of the tool. Contact closure should be observed between pins 1 and 2.

(8) Adjust the closure point, if required, by loosening the No. 2 machine screws securing the switch in place and sliding the switch body vertically until the previously established requirements are met. Remove the tool.

(9) Reinstall P109 onto the Logic PCBA.

(10) Return the Logic PCBA to the normal position.

(11) Reinstall the dust cover and return the drive to the enclosure.

6.16.2.5 Cartridge Thermistor Mechanism Test and Adjustment

(1) Extend the drive fully forward out of the rack; remove the disk cartridge and disconnect the line cord.

(2) Remove the dust cover as described in Paragraph 2.2, Step (9). Elevate the Logic PCBA to the maintenance position.

(3) Remove a disk from its cartridge.

(4) Place the disk on the spindle so that it is seated normally, but without cartridge.

(5) Observe the gap between the thermistor edge and the edge of the upper disk.

(6) Acceptable limits:

- 0.76 mm (0.03 inch) (minimum)
- 1.27 mm (0.05 inch) (maximum)

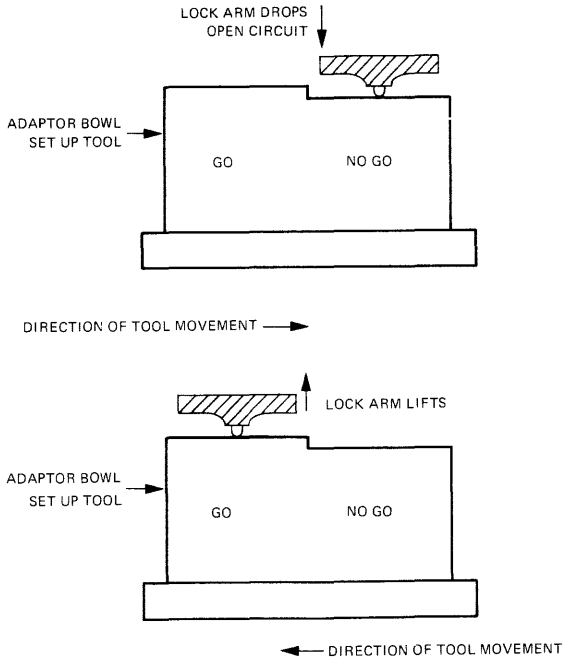


Figure 6-35. GO/NO GO Adjustment Tool, End View

(7) If the acceptable limits are not met, adjustment can be made by loosening the four mounting screws at the base of the assembly and moving the whole thermistor assembly.

(8) Connect the power cord to the voltage source.

(9) Place the ON/OFF Power Switch to ON.

(10) Allow drive to come to the SAFE condition. This will cause the upper disk thermistor solenoid to activate.

(11) While the thermistor solenoid is activated, observe the tip of the thermistor in relation to the inside wall of the adapter bowl.

(12) If the tip of the thermistor is recessed less than 0.76 mm (0.03 inch) below the inside wall of the adapter bowl, loosen the two hex nuts holding the solenoid coil and adjust the tip of the thermistor so that it is recessed 0.76 mm or more below the inside wall of the adapter bowl.

(13) Remove power from the drive. This will deactivate the thermistor solenoid.

(14) Confirm that the gap between the edge of the thermistor and the edge of the upper disk is still within acceptable limits.

(15) Return the Logic PCBA to the normal position.

(16) Reinstall the dust cover and return the drive to the enclosure.

6.17 BEZEL AND POWER SWITCH

6.17.1 REMOVAL OF BEZEL

Removal or adjustment of the bezel is made by loosening six socket-head countersunk Allen machine screws securing the assembly to the base assembly.

NOTE

The holes through which the screws pass are slotted to allow for bezel removal without removing screws.

To remove the bezel, proceed as follows.

(1) Back off the six machine screws enough to clear bezel supports on each side of the bezel.

(2) Pull the assembly forward and away from the deck assembly.

(3) Access to parts requiring replacement or adjustment is now available.

6.17.2 INSTALLATION OF BEZEL

To install the bezel, proceed as follows.

(1) Ensure that the six machine screws are backed off enough to clear the bezel support on each side of the bezel.

(2) Carefully position the bezel to the deck assembly and secure the bezel mounting screws.

6.17.3 REMOVAL OF POWER SWITCH BRACKET

Remove the bezel as outlined in Paragraph 6.17.1. Access to three switch bracket screws is now available. Two mounting screws are located below the bracket and one is located to the right side of the bracket. See Figure 6-36.

6.18 MAGNETIC TRANSDUCER GAP

Magnetic transducers are used in one place on front load models and two places on top load models. In each case, the distance between the transducer pole tip and its respective rotating surface must be precisely controlled to produce acceptable signal levels.

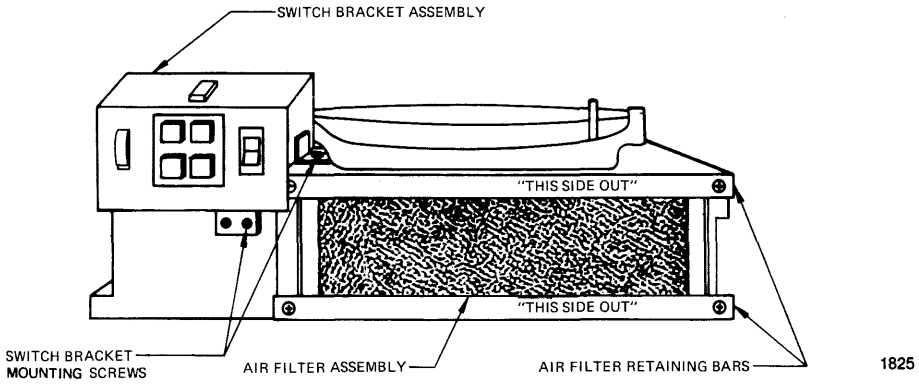


Figure 6-36. Switch Bracket and Air Filter Retaining Screw Locations

Paragraphs 6.18.1 and 6.18.2 describe the test and adjustment procedures for the upper and lower transducers, respectively.

6.18.1 UPPER TRANSDUCER TEST AND ADJUSTMENT — TOP LOAD MODELS

Extend the unit forward out of the rack and install the Adapter Bowl Setup Tool (PCC PD Part No. 103619-01) onto the spindle cone. Ensure that cone and tool are clean.

CAUTION

WHEN GAUGING GAP CLEARANCE, ENSURE THAT NO DAMAGE IS DONE TO THE SENSING TIP OF THE TRANSDUCER BY THE FEELER GAUGE.

A feeler gauge is used to measure the gap distance between the transducer pole tip and the tool (see Figure 6-34). Each adapter bowl setup tool will have marked on it a calibration value to be added to the normal feeler gauge value.

The nominal feeler gauge value is given in Table 6-7. The calibration value for the particular tool is added to the value obtained from the table and rounded to the nearest half mil to obtain the actual feeler gauge thickness to be used. A single feeler gauge blade, or two or more stacked, may be used to obtain the thickness required. Use clean, dry blades.

If the gap clearance requires adjustment, slightly loosen the No. 4 machine screws securing the transducer clamp (see Figure 6-37). Position the transducer body to the required clearance and retighten the screws. Recheck gap clearance and perform the circumferential alignment procedure detailed in Paragraph 6.14.6 or 6.14.8.

6.18.2 LOWER TRANSDUCER ALIGNMENT — FRONT LOAD AND TOP LOAD MODELS

The gap clearance between the transducer pole tip and the phase-lock ring located on the spindle should be 0.18 ± 0.05 mm (0.007 ± 0.002 inch). See Figure 6-38. A feeler gauge is used to establish the clearance between the transducer pole tip and the center of a phase lock ring segment located on the spindle.

CAUTION

WHEN GAUGING GAP CLEARANCE, ENSURE THAT NO DAMAGE IS DONE TO THE SENSING TIP OF THE TRANSDUCER BY THE FEELER GAUGE.

When the gap clearance requires adjustment, slightly loosen the No. 4 machine screws securing the transducer clamp. Position the transducer to establish correct gap clearance and retighten clamping screws. Recheck gap clearance.

Table 6-7
Upper Transducer Calibration Data

Adapter Bowl Setup Tool Revision Level	Allowable Nominal Armature Plate Notch Width	Nominal Feeler Gauge Value	Allowable Armature Plate Diameter	Maximum Allowable Armature Plate Runout (TIR*)
A	2.032 mm (0.080″)	0.48 mm (0.019″)	145.75 + 0.13 mm (5.738 + 0.005″)	0.254 mm (0.010″)
B	2.032 mm (0.080″)	0.23 mm (0.009″)	145.75 + 0.05 mm (5.738 + 0.002″)	0.076 mm (0.003″)
and	1.016 mm (0.040″)			
subsequent	0.058 mm (0.020″)			
	2.032 mm (0.080″)	0.74 mm (0.029″)	145.75 + 0.13 mm (5.738 + 0.005″)	0.254 mm (0.010″)
	2.03mm (0.079″)	0.74 mm (0.029″)	145.75 + 0.13 mm (5.738 + 0.005″)	
*Total Indicated Runout				

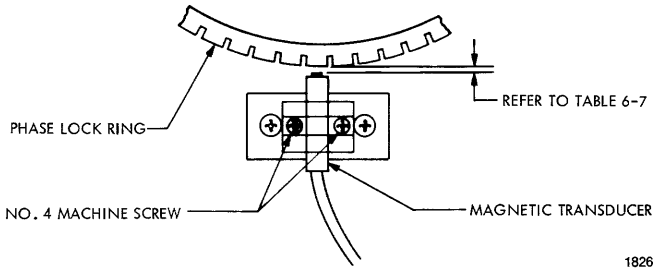


Figure 6-37. Upper Transducer Alignment, Top Load Only

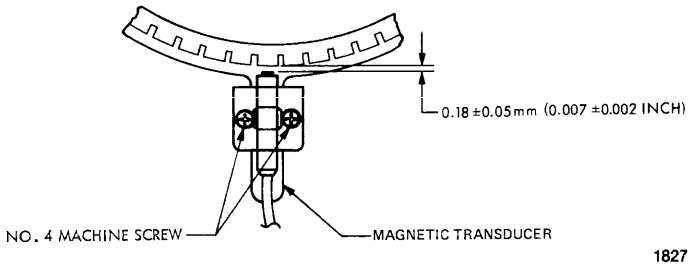


Figure 6-38. Lower Transducer Alignment, Front and Top Load

6.19 DISK DRIVE PULLEY SYSTEM

The drive utilizes a flat belt and crowned pulleys to operate the spindle and blower at correct speeds. Operation at 1500 and 2400 rpm is obtained at 50 or 60 Hz by changes of pulley sizes and belt length. Refer to Table 6-8 for identification of belt and pulley combinations.

6.19.1 BELT REMOVAL

Location of pulleys and direction of rotation is indicated in Figure 6-39. To replace a belt, proceed as follows.

(1) Remove four No. 10 machine screws securing the belt guard in place.

(2) Slide the belt guard forward until it drops away from the base.

(3) Insert a large shanked screwdriver between the tension idler plate and the base. Compress the tension idler spring until the belt is released from the motor pulley.

(4) Remove the belt from the area.

6.19.2 BELT REPLACEMENT

The following sequence is followed when replacing a drive belt. Refer to Figure 6-39 for threading pattern.

(1) Loop one end of drive belt around spindle pulley. Center the belt on crown of pulley and, by hand, hold the remainder of belt taut until Step (2) is completed.

(2) Feed the remainder of the belt loop under the idler tension roller arm.

NOTE

At this point the outside face of the belt contacts the crown of the tension roller.

(3) Feed the remainder of the belt loop again under the tension roller arm and up toward the blower pulley.

(4) Loop the belt around the blower pulley. Release the loop and extend the remainder of the belt loop to the drive motor pulley.

NOTE

At this point the inside face of the belt contacts the traction area of the blower pulley.

(5) Continue the remainder of the belt loop up to the drive motor pulley. Spread the belt apart to form a loop which can be slid down and around the traction area of the drive motor pulley.

(6) With a large shank screwdriver (used as a crowbar), pry the tension arm forward by compressing the tension arm spring toward the front of the base. This action will establish enough slack in the belt to allow the belt loop mentioned in Step (5) to be slipped down around the drive motor pulley. Release pressure on the tension arm.

(7) Inspect the belt for location on all driven surfaces and also determine that the belt does not contact any surface that will cause belt abrasion.

(8) By hand, pull the belt through several revolutions of the drive system in order to allow the belt to seek its normal operating path. This action will also establish the correct tension of the belt between pulley spans.

NOTE

If the belt comes in contact with any structural member, either raise or lower the drive motor pulley on the motor shaft until the belt clears the obstruction.

(9) Inspect the static discharge contact that touches, located on the end of the spindle shaft (see Paragraph 6.20).

(10) Reinstall the belt guard and return the drive to the enclosure.

Table 6-8
Pulley and Belt Identification

Disk Speed	Line Frequency	Motor Pulley P/N and Crown Dia.	Blower Pulley P/N and Crown Dia.	Spindle Pulley P/N and Dia.	Belt P/N and Inside Circum.*
1500 rpm	60 Hz	102636-01 43.69 mm (1.720″)	102722-01 43.69 mm (1.720″)	102635-02 88.14 mm (3.470″)	102634-01 1071.56 mm (42.1875″)
1500 rpm	50 Hz	102636-02 54.43 mm (2.143″)	102722-01 43.69 mm (1.720″)	102635-02 88.14 mm (3.470″)	102634-02 1086.64 mm (42.7812″)
2400 rpm	60 Hz	102636-02 54.43 mm (2.143″)	102722-02 54.43 mm (2.143″)	102635-01 68.22 mm (2.686″)	102634-01 1071.56 mm (42.1875″)
2400 rpm	50 Hz	102636-03 65.10 mm (2.563″)	102722-02 54.43 mm (2.143″)	102635-01 68.22 mm (2.686″)	102634-02 1086.64 mm (42.7812″)

*Inside circumference + 3.175 mm (+ 0.125″)
- Tension Roller P/N 102609-01; 49.53 mm (1.950″) Dia.
- Drive Motor P/N 103579-01

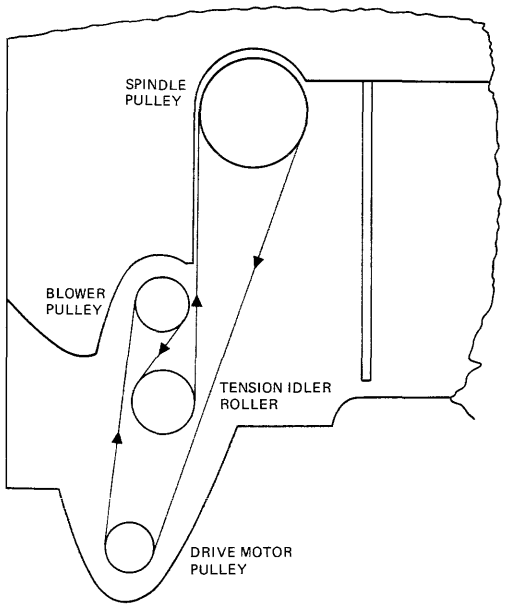


Figure 6-39. Belt Threading Pattern

6.20 STATIC DISCHARGE CONTACT

The static discharge Rulon contact assembly is mounted on the belt guard. This contact provides a ground path from the spindle shaft to ground. Continuity is maintained by the tension of the metal spring on which the Rulon contact is mounted. Grounding of the spindle shaft thus prevents a buildup of static electricity on the disk surface.

Inspection is made as follows.

(1) Remove the four No. 10 machine screws securing the belt guard in place.

(2) Slide the belt guard forward until it is free of the base.

(3) Inspect the static discharge Rulon contact for wear.

NOTE

If the Rulon contact shows signs of excessive wear from the pointed end of the spindle shaft, replace the belt guard (PCC PD Part No. 102748).

(4) Reinstall the belt guard and return the drive to the enclosure.

6.21 CARE AND HANDLING OF HEADS

Figure 6-40 shows examples of proper care and handling of the magnetic heads. Peak performance of the drive cannot be expected unless proper care is taken when handling these heads.

Figure 6-41 shows examples of improper handling of the magnetic heads; these examples are only a few of the ways a head can be damaged by improper care.

6.21.1 LOAD PIN SEATING

Proper seating of the load pin is essential to ensure gimbaling and flying characteristics of the ceramic slider. Examples of correct and incorrect positions of the load pin are shown in Figure 6-42.

CAUTION

IF ANY HEAD IS MISHANDLED (FIGURE 6-41), OR IF ANY GIMBAL SPRING IS DAMAGED, THE HEAD ASSEMBLY MUST BE REPLACED, OR DISK DAMAGE MAY OCCUR.

6.22 HEAD REMOVAL AND INSTALLATION

Removal of a head is occasioned by mechanical damage, electrical failure, or for the purpose of cleaning. In the event one head needs attention, it is recommended that all heads be removed from the carriage, inspected, and cleaned. It is also recommended that data stored on the lower platter(s) be transferred to a cartridge prior to any head removal.

6.22.1 HEAD REMOVAL PROCEDURE

The magnetic head is removed as follows.

(1) Disconnect the drive from the power source.

(2) Extend the drive fully forward from the enclosure, if necessary.

(3) Remove the dust cover (refer to Paragraph 2.2).

(4) Disconnect head connectors from the Read/Write Selection Matrix PCBA.

NOTE

The steel protective sheath on each connector lead is magnetic and will allow the connectors to be laid on the side surface of the magnet, thus preventing damage to the connectors while removing other components.

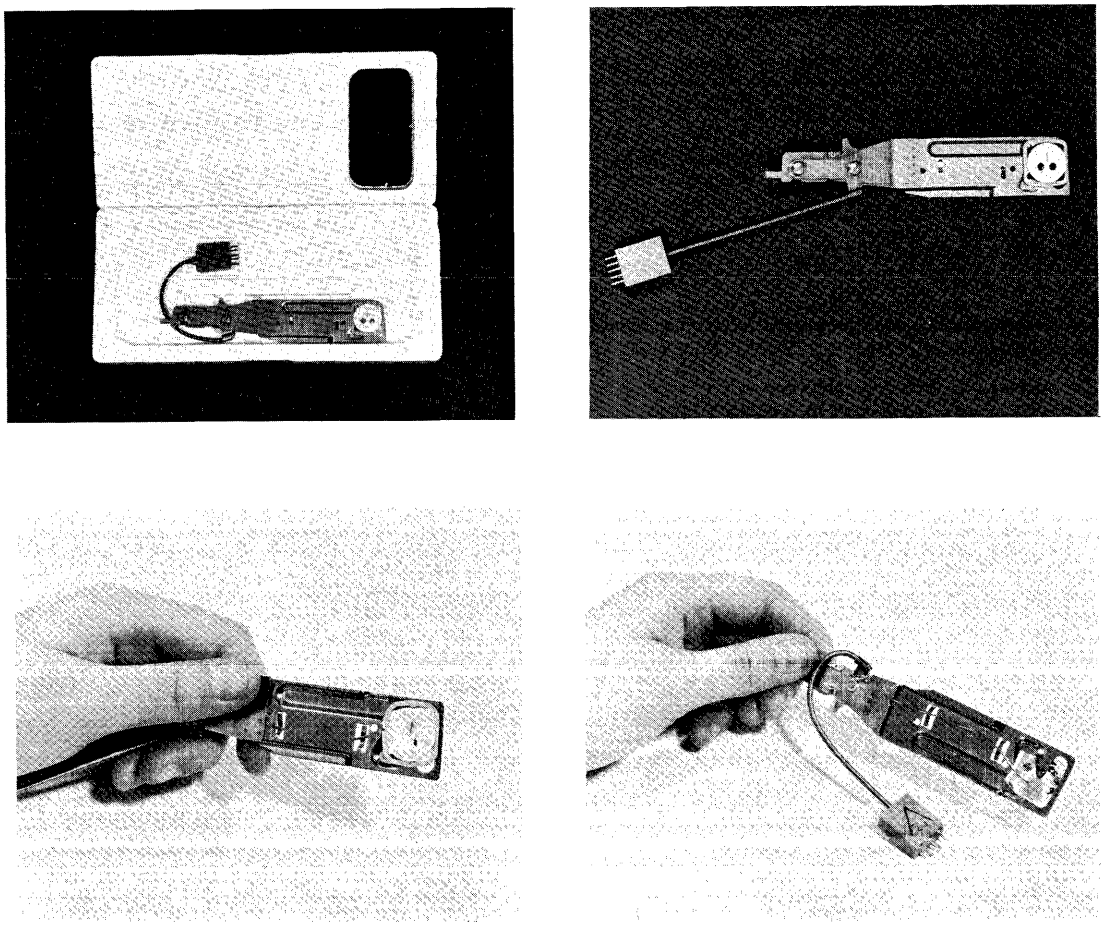


Figure 6-40. Examples of Proper Care and Handling of Heads

(5) Disconnect all connectors from the Read/Write PCBA and Read/Write Selection Matrix PCBA; remove only the Read/Write PCBA from the drive.

(6) Prepare four lint-free pads, approximately 1-inch square and 1/8-inch thick. Lay a lint-free wipe on a clean flat surface on which to lay the heads when they are removed from the carriage.

(7) Refer to Figure 6-43 for parts identification.

(8) Insert between the ceramic sliders of each pair of heads the pads prepared in Step (6); these pads will protect the ceramic sliders from clashing together as they are being removed.

(9) Install positioner tie-down screw to anchor the positioner carriage.

(10) Loosen the four recessed Allen-head cone-pointed setscrews in the clamp plate to a position where the point of each screw is recessed below the surface of the clamp plate.

CAUTION

CARRIAGE MUST BE FULLY RETRACTED AND REMAIN RETRACTED WHILE REMOVING HEAD ASSEMBLIES.

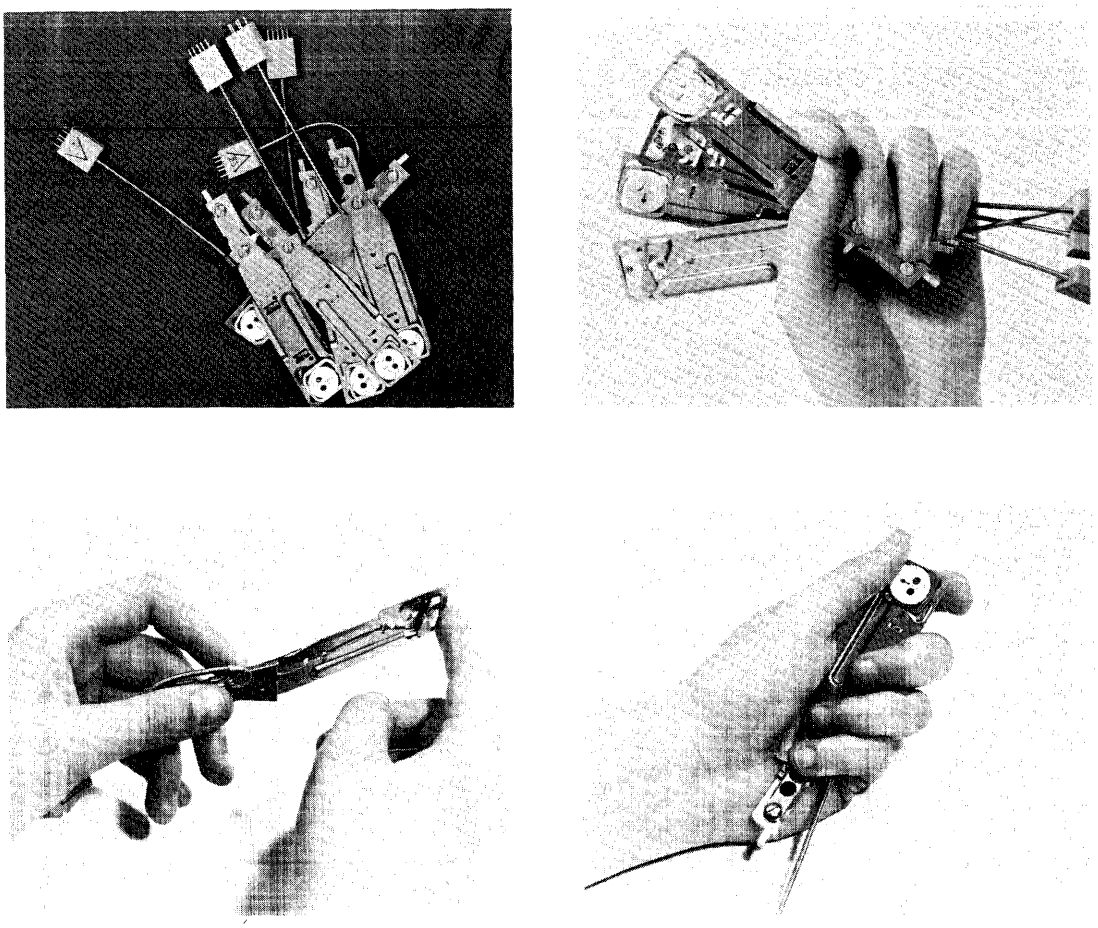


Figure 6-41. Examples of Improper Care and Handling of Heads

(11) Loosen the two Allen-head retaining screws from the clamp plate. Remove the clamp plate and screws from the carriage.

(12) Loosen and remove the Allen-head screw and clamp washer from each of the remaining three pairs of head-support arms that are anchored to the carriage (see Figure 6-43 A and B).

(13) Remove the heads in the following sequence: head 0 (top), head 1 (second), head 2 (third), head 3 (fourth), head 6 (fifth), head 7 (sixth), head 4 (seventh), and head 5 (eighth).

CAUTION

EXERT EVERY PRECAUTION TO PREVENT DAMAGE TO THE GIMBAL SPRING AND CERAMIC SLIDER WHILE REMOVING AND HANDLING THE HEADS.

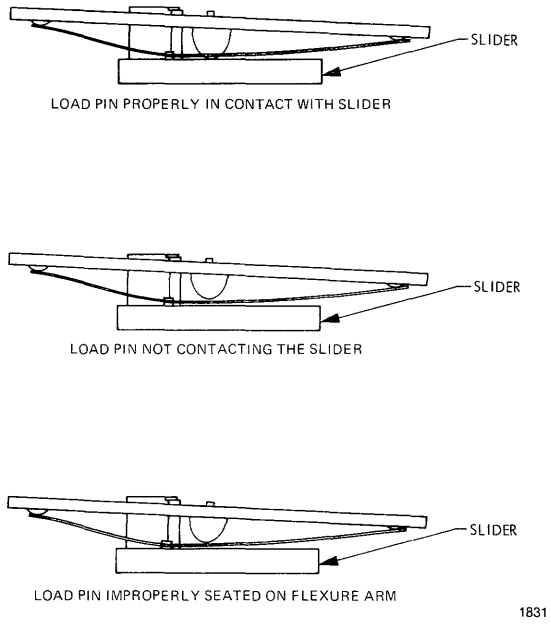


Figure 6-42. Load Pin Seating

- Using thumb and forefinger, apply sufficient pressure to the head end of the support arm to separate the body of the support arm from the ramp. Push the head arm approximately 3/8-inch straight forward into the disk cavity by applying pressure to the die cast positioning arm while holding positioning arm flat against the carriage mounting surface until the arm is free of the carriage slots. Again, use extreme caution not to allow the gimbal spring or the ceramic slider to come in contact with any other surrounding part.
- When a head is free, place it on a lint-free wipe in the clean area with the ceramic slider facing up.
- Remove other heads in succession, observing equal precautions for each head.

6.22.2 HEAD INSTALLATION PROCEDURE

Installation of the heads after cleaning, or replacing a damaged head, is accomplished as follows.

(1) If required, perform the necessary Steps (1) through (5) of Paragraph 6.22.1.

(2) Prior to installing heads, inspect carriage and surrounding area for any foreign material that could contaminate heads or interfere with installation. Clean the head mounting area with 91-percent isopropyl alcohol.

NOTE

Use only 91-percent isopropyl alcohol to clean disks and heads. Use of any other type of cleaner or solvent, such as carbon tetrachloride or trichlorethylene may result in damage. Do not use contaminated alcohol which could contain any form of residue.

Examine the carriage slots into which the supporting arm of the head is placed for any nicks or burrs that would obstruct installation or alignment.

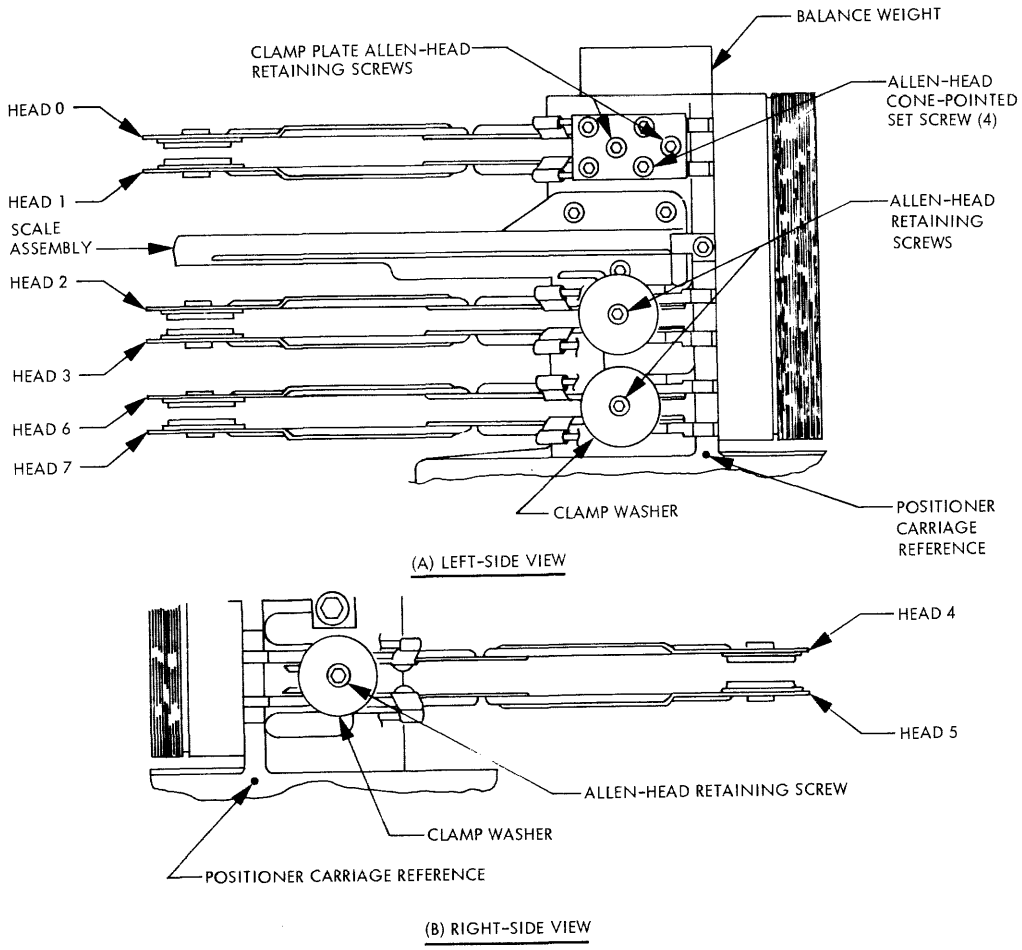


Figure 6-43. Heads Installed on Positioner Carriage

(3) Examine the ceramic slider of each head for cleanliness. Also inspect gimbal spring and slider pivot for proper alignment. Refer to Figure 6-42.

(4) Prepare four lint-free wipe pads, approximately 1-inch square and 1/8-inch thick; these pads will be used to separate each pair of heads to prevent possible damage to the ceramic slider during installation.

(5) Note that there are two V-shaped indentations on the side of the die-cast support arm. Fore and aft head alignment of several thousandths of an inch can be made when the pointed screws in the clamp plate engage with the V slots in the support arm. Figure 6-43 illustrates the support arm used in all models.

6.22.2.1 Installation of Head-to-Carriage Slots

(1) Insert the support arm for head 7 into the Head Installation Tool (PCC PD Part No. 104839).

(2) Locate the threaded holes on the carriage used for the clamp plate(s) retaining screws.

CAUTION

CARRIAGE MUST BE FULLY RETRACTED AND REMAIN RETRACTED WHILE INSTALLING HEAD ASSEMBLIES.

NOTE

When installing heads, it is recommended that the bottom head be installed first, progressing up to the top head.

CAUTION

CARRIAGE MUST NOT BE MOVED FROM THE FULLY RETRACTED POSITION UNTIL ALL HEADS ARE SECURED IN PLACE BY THE CLAMP PLATE.

(3) Carefully guide the bottom head into place with the ceramic slider facing upward and insert the die-cast body of the support arm into the carriage slots part of the way. Figure 6-44 shows the position of the head support arm in relation to the carriage slot(s).

(4) Visually position the support arm Vs to be approximately on center with the two retainer clamp screw holes.

NOTE

Improper horizontal positioning of the head into the carriage slot may result in improper loading of the head. Make sure that the end-protruding tab of the head support arm is inserted into the carriage slot so that the head-to-carriage distance shown in Figure 6-44 is obtained. Ensure that the head support arm does not contact the loading/unloading ramp during a Restore operation.

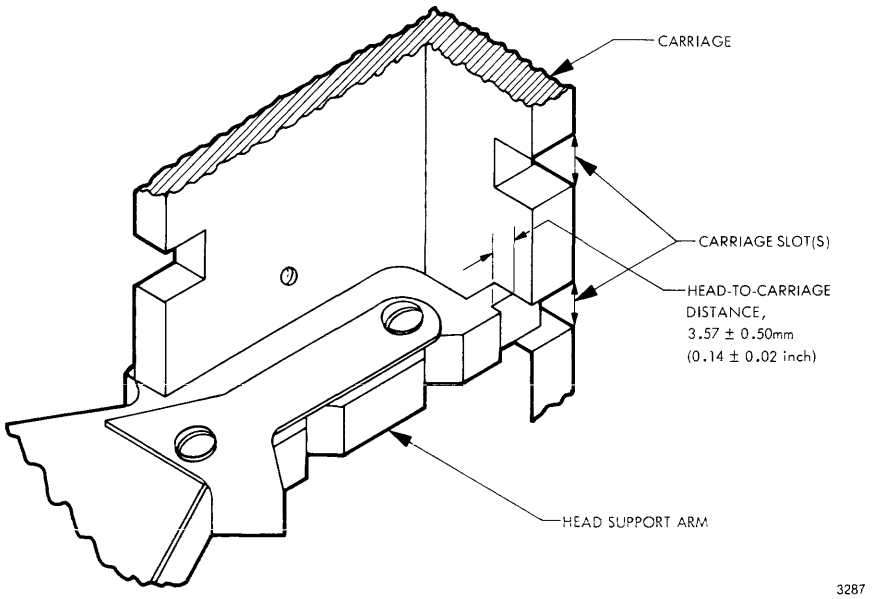


Figure 6-44. Head to Carriage Adjustment

(5) Firmly press the support arm back against the carriage surface and at the same time position the flange of the head on the underside of the lower ramp.

CAUTION

DO NOT OVER-STRESS HEAD GIMBAL SPRING DURING INSTALLATION.

(6) Place a lint-free wipe protective pad on the ceramic slider.

(7) In succession, install the other heads in the manner described in the preceding steps (refer to Figure 6-43(A) and (B) for head identification).

6.22.2.2 Installation of Clamp Plate and Clamp Washers

When all heads are in place on the carriage, proceed as follows.

NOTE

As a precaution, before installing the clamp plate, determine that all pointed setscrews are recessed below the surface of the clamp plate.

(1) Install the upper pair and lower pair of retaining screws through the holes in the clamp plate for heads 1 and 0.

NOTE

Under no circumstances should a clamp plate screw or a spacer be substituted for the original hardware.

(2) Tighten clamp plate retaining screws. Torque to approximately 10 to 12-inch pounds.

(3) Install the clamp washers and Allen-head screws removed in 6.22.1 Step (13).

CAUTION

WHEN TIGHTENING THE CLAMP RETAINING SCREWS, CAUTION MUST BE TAKEN NOT TO OVER-TORQUE THE SCREWS. OVER-TORQUEING CAN CAUSE THREADS IN THE CARRIAGE CASTING TO STRIP.

6.22.2.3 Head Positioning

(1) Starting with heads 1 and 0, run in each pair of pointed setscrews so that each engages with a side of the V on the support arm to an approximate equal depth. Do not allow points of setscrews to bottom out in the V on the arm.

NOTE

Horizontal position of Heads 2 through 7 is not critical.

(2) Maintain the position of heads 3 through 7 as installed in 6.22.2.2, Step (3).

(3) Inspect installation; install the connectors to the Read/Write PCBA.

(4) To correctly position head 1 and head 0, a CE alignment must be made; refer to Paragraph 6.14 for procedure.

(5) After satisfactory CE alignment is made, return the drive to original configuration.

6.23 LAMP/LENS ASSEMBLY REMOVAL AND INSTALLATION

The Lamp/Lens Assembly is located between the upper pair of recording heads and the positioner scale, and is mounted to the base assembly.

Removal of the Lamp/Lens Assembly is occasioned by mechanical damage to the lens or electrical failure of the lamp.

6.23.1 LAMP/LENS ASSEMBLY REMOVAL

(1) Remove the Phillips head screw that anchors the Lamp/Lens Assembly to the Sensor Receiver Assembly.

(2) Remove tie wraps as necessary to free Lamp/Lens Assembly connecting leads.

(3) Disconnect P203 from the Servo PCBA and extract pins 10 and 12 from P203 using a Molex pin extractor (Mfg. Part No. HT2285); the wires on these pins are connected to the Lamp/Lens Assembly.

(4) Remove the Lamp/Lens Assembly and discard.

6.23.2 LAMP/LENS ASSEMBLY INSTALLATION

(1) Align the Lamp Assembly in such a manner that the locating pins on the assembly fit into the appropriate holes on the Sensor Receiver Assembly.

(2) Replace the Phillips head screw removed in Paragraph 6.23.1, Step (1).

(3) Insert pins 10 and 12, at the end of the leads connected to the Lamp/Lens Assembly, into mating pin holes of P203 and reinstall P203 onto the Servo PCBA.

(4) Replace the tie wraps removed in Paragraph 6.23.1, Step (2).

(5) Perform the positioner servo calibration procedures in Paragraphs 6.8 and 6.9.

6.24 RETICLE REMOVAL AND INSTALLATION

Removal of the reticle is occasioned by mechanical damage to this component. The reticle is an integral part of the Sensor Receiver Assembly and is located immediately below the positioner scale, vertically in line with the Lamp/Lens Assembly. If the reticle is damaged, the entire Sensor Receiver Assembly (Part No. 104500-02) must be replaced.

6.24.1 RETICLE REMOVAL

(1) Remove the Lamp/Lens Assembly according to the procedure in Paragraph 6.23.1, Steps (1) and (2).

(2) Loosen the horizontal hexagonal head screw located on the thermal compensation block, but do not loosen the thermal block itself. This will loosen the receiver post so that it can be rotated.

(3) Rotate the receiver post clockwise until the reticle is clear of the Scale Assembly.

CAUTION

WHEN ROTATING THE RECEIVER POST, ENSURE THE RETICLE DOES NOT CONTACT ANY PART OF THE SCALE ASSEMBLY.

(4) Remove tie wraps from wires connecting the reticle and P203 on the Servo PCBA.

(5) Disconnect P203 from the Servo PCBA. Extract leads 1, 2, 3, 6, 7, 8, 10, and 12 with their pins from P203 using a Molex pin extractor (Mfg. Part No. HT2285).

(6) Remove the Sensor Receiver Assembly.

6.24.2 RETICLE INSTALLATION

The reticle is an integral part of the Sensor Receiver Assembly and is installed in the drive in accordance with the following procedure.

(1) Insert leads 1, 2, 3, 6, 7, 8, 10, and 12 with their pins into the mating holes in J203 on the replacement Sensor Receiver Assembly, reinstall onto the Servo PCBA.

(2) With the reticle arm pointing toward the rear of the drive, insert the sensor receiver post into the hole provided in the thermal compensation block.

(3) Rotate the Sensor Receiver Assembly counterclockwise until the reticle is directly under the scale. If this cannot be done, adjust the Phillips head screw inside the sensor receiver assembly post so that the bottom of the Phillips head screw is flush with the bottom of the post.

CAUTION

WHEN ROTATING THE SENSOR RECEIVER ASSEMBLY, ENSURE THE RETICLE DOES NOT CONTACT ANY PART OF THE SCALE ASSEMBLY.

(4) Tighten the horizontal hexagonal head screw on the temperature compensation block until it is possible to rotate the post.

(5) Adjust the Phillips head screw inside the sensor receiver post so that the clearance between reticle and the scale is 0.005 inch. A 0.005-inch mylar shim can be used for this purpose (PCC PD Part No. 104476-02).

(6) Replace the Lamp/Lens Assembly according to the procedure in Paragraph 6.23.2.

(7) Replace the tie wraps removed in Paragraph 6.24.1, Step (4).

(8) Perform the positioner servo calibration procedures in Paragraphs 6.7 through 6.9.

6.25 SCALE ASSEMBLY REMOVAL AND INSTALLATION

Removal of the Scale Assembly is occasioned by mechanical damage to the scale frame, or in the event that the glass scale is cracked or broken.

6.25.1 SCALE ASSEMBLY REMOVAL

(1) Remove all magnetic heads by following the procedure in Paragraph 6.22.1.

(2) Remove the Lamp/Lens Assembly by following the procedure in Paragraph 6.23.1, Steps (1) and (2).

(3) Remove the three Allen-head screws and the scale clamp that holds the Scale Assembly to the carriage. The Scale Assembly will still be held in place by the locating pin on the carriage.

(4) Remove the Scale Assembly by carefully applying sufficient pressure to disengage it from the locating pin.

CAUTION

WHEN REMOVING THE SCALE ASSEMBLY, ENSURE THAT IT DOES NOT CONTACT THE RETICLE. DO NOT TOUCH ANY PORTION OF THE GLASS SCALE.

6.25.2 SCALE ASSEMBLY INSTALLATION

(1) Align the hole in the frame of the replacement Scale Assembly with the locating pin on the carriage.

CAUTION

WHEN REPLACING THE SCALE ASSEMBLY, ENSURE THAT IT DOES NOT CONTACT THE RETICLE ASSEMBLY.

(2) Press Scale Assembly firmly against the carriage so the locating pin is firmly seated.

(3) Replace the scale clamp but do not tighten the three Allen-head screws removed in Paragraph 6.25.1, Step (3).

(4) Replace the Lamp/Lens Assembly removed in Paragraph 6.25.1, Step (2).

(5) Disconnect connector P205 from the Servo PCBA; this removes power from the linear motor so that the heads can be positioned manually.

(6) Apply power to the drive and observe that the SAFE indicator becomes illuminated. The carriage can now be manually extended and retracted.

(7) Extend the carriage fully toward the drive spindle.

(8) Adjust the Scale Assembly so that the clearance between the reticle and the glass scale is 0.127 mm (0.005 inch) at both ends of the carriage travel. A 0.127 mm (0.005-inch) mylar shim can be used for this purpose.

(9) Connect an oscilloscope's Channel 1 test probe to TP21 on the Servo PCBA, use TP26 as ground.

(10) Set channel sensitivity to 2v per division.

(11) Set horizontal sweep rate to 0.5 msec per division.

(12) Observe the peak-to-peak amplitude.

(13) Move the carriage back and forth over its full stroke; the peak-to-peak amplitude (envelope) noted in Step (9) should remain constant.

NOTE

If the voltage obtained varies more than ± 10%, rotate the Scale Assembly about the pin until the voltage observed over the full carriage stroke remains within ± 10%.

(14) Tighten the three Allen-head screws on the Scale Assembly.

(15) Replace the heads by following the procedure detailed in Paragraph 6.22.2.

NOTE

Do not replace P205 at this time.

(16) Perform the static and dynamic positioner procedures given in Paragraphs 6.8 and 6.9, respectively, and also the CE alignment given in Paragraph 6.14.

6.26 AIR FILTER

The filter assembly consists of two parts, the pre-filter, which is a fine-meshed open-cell foam material covering the air intake area of the absolute filter, and the absolute filter. The absolute filter consists of a labyrinth of small metallic separators forming the filter path between the filter media.

The absolute filter is encased within a plastic frame for ease of handling and preventing damage to the internal structure. Handle the absolute filter by the edges of the plastic framework. Use caution not to compress the sides or center of the filter, as puncturing of the filtering media could result, thereby lessening the effectiveness of the filter.

6.26.1 PRE-FILTER CLEANING

(1) Remove the bezel as described in Paragraph 6.17.1.

(2) The pre-filter is removed by lifting one corner of the meshed material and gently pulling it away from the front surface of the absolute filter.

NOTE

The pre-filter may be washed in soap and water and reused. It must be completely dry and free from any cleaning residue before replacing it on the front of the absolute filter.

6.26.2 REMOVAL OF ABSOLUTE FILTER

(1) Remove the bezel (refer to Paragraph 6.17.1) and observe two retaining bars marked THIS SIDE OUT (see Figure 6-36). Remove the two retaining bars that are purposely curved to hold the absolute filter under tension against the base casting.

(2) Withdraw the absolute filter from the air duct cavity in the base by grasping the two edges and pulling straight forward. After removing, inspect for any plastic chips or other matter remaining in the air duct cavity.

(3) Discard the used absolute filter.

NOTE

Always replace the absolute filter rather than attempting to clean it.

6.26.3 REPLACEMENT OF ABSOLUTE FILTER

Before installing a new absolute filter, inspect the plastic framework for any contamination. Especially inspect for plastic flashing clips or excess plastic that could be shaved off the edges by the air duct during installation. If the filter is not easily inserted into the air duct, or its shape is distorted, there is a likelihood that the filter is defective and should not be used.

CAUTION

TOBACCO ASHES AND SMOKE WILL CONTAMINATE THE AIR SYSTEM AND THE ABSOLUTE FILTER. HANDLE THE FILTER IN THE CLEANEST ENVIRONMENT AVAILABLE.

Inspect the air duct leading up to the blower for any other matter that could have passed through the filter system. Clean with a lint-free cloth, if required. Replace the filters and secure the assembly into place. Be sure the retaining bars are correctly installed with the THIS SIDE OUT showing (see Figure 6-36).

6.27 POWER SUPPLY

The power supply is a removable module located on the underside of the base assembly.

6.27.1 REMOVAL OF POWER SUPPLY

WARNING

VOLTAGES MAY BE PRESENT IN THE POWER SUPPLY AREA WHICH ARE CONSIDERED DANGEROUS TO LIFE. THE EMERGENCY UNLOAD AND MOTOR START CAPACITORS MAY REMAIN CHARGED FOR A CONSIDERABLE LENGTH OF TIME, EVEN THOUGH POWER HAS BEEN REMOVED. OBSERVE EXTREME CAUTION.

(1) Disconnect power.

(2) Extend the unit out of the cabinet and remove the dust cover (refer to Paragraph 2.2, Step (9).

(3) Position the Logic and Servo PCBAs to the maintenance position.

(4) Disconnect the power switch cable connector J501.

(5) Disconnect the power supply cables P212 and P213 at the Servo PCBA.

(6) Remove the high voltage cover from the Motor Control PCBA; disconnect P401, P402, P403, or P404, and fan leads.

(7) Remove the belt guard; refer to Paragraph 6.19.1, Steps (1) and (2).

(8) The Read/Write PCBA and Temperature Compensation PCBA, with retaining hardware, should be removed as needed prior to power supply removal.

(9) Remove the eight No. 10 screws securing the power supply chassis to the base. Carefully lower the power supply chassis out and away from the base.

CAUTION

AVOID SQUEEZING ANY CABLES BETWEEN THE BASE AND CHASSIS DURING REMOVAL, AS DAMAGE TO THE CABLING CAN RESULT.

6.27.2 POWER SUPPLY INSTALLATION

WARNING

VOLTAGES MAY BE PRESENT IN THE POWER SUPPLY AREA WHICH ARE CONSIDERED DANGEROUS TO LIFE. THE EMERGENCY UNLOAD AND MOTOR START CAPACITORS MAY REMAIN CHARGED FOR A CONSIDERABLE LENGTH OF TIME, EVEN THOUGH POWER HAS BEEN REMOVED. OBSERVE EXTREME CAUTION.

(1) Verify that power is removed from the drive.

(2) Extend the unit out of the cabinet and remove the dust cover; refer to Paragraph 2.2, Step (9).

(3) Position the Logic and Servo PCBAs to the maintenance position.

(4) Check connections at power transformer primary and ensure that it is connected for the correct line voltage (refer to Figure 4-14 for line voltage connections).

(5) Secure the power supply in place using the screws removed in Step (9) of Paragraph 6.27.1.

(6) Inspect all wiring extended through casting to the upper deck area for crushed or abraded wires.

(7) Install the belt guard.

(8) Reconnect all cables disconnected in Steps (4) and (5) of Paragraph 6.27.1.

(9) Remount the Read/Write PCBA, Temperature Compensation PCBA, and retaining hardware.

(10) Lower the Logic and Servo PCBAs into operating position.

(11) Inspect the interior of the drive for any items or parts that could interrupt operation.

(12) Return the drive to normal operating condition.

6.28 EXHAUST FAN REMOVAL AND INSTALLATION

Removal of the exhaust fan is occasioned by mechanical damage to the fan blade, fan cage, or if the fan becomes electrically inoperative. The fan is located at the extreme rear left side of the drive immediately over the smaller of the two heat sinks and must be removed from the rear in accordance with the following procedure.

(1) Make sure all power is removed from the drive, then position the Logic and Servo PCBAs to the maintenance position.

(2) Disconnect the voltage line connector (P2) from the top of the fan cage.

(3) While facing the rear of the disk drive, loosen the two Phillips screws in each upper corner of the fan cage.

(4) Note the position of the plastic cable anchor and the hinged standoff that is fastened to the metal base strip of the Logic PCBA.

(5) Remove both screws that were loosened in (3) while making sure the Logic PCBA remains in an upright position.

(6) Note the position of the printed arrow on the top side of the fan cage. The arrow should be pointing to the rear of the drive.

(7) Loosen and remove the two bottom corner Phillips screws. This will free the exhaust fan assembly so that it can be removed.

NOTE

The hinged standoff supports part of the weight of the Logic PCBA. As the exhaust fan assembly is removed, make sure that the Logic PCBA does not sag to one side.

(8) Insert a new exhaust fan assembly (Part No. 518-0005) making sure that the printed arrow on the top of the fan cage points to the rear and the four mounting holes line up with those on the drive base.

(9) Install the two Phillips screws removed in Step (7).

(10) Insert the two Phillips screws, making sure the hinged standoff and plastic cable anchor are installed as noted in Step (4).

(11) Tighten each corner Phillips screw.

(12) Connect the voltage line connector removed in Step (2).

(13) Lower the Logic and Servo PCBAs into their operating position.

6.29 DRIVE MOTOR

6.29.1 DRIVE MOTOR REMOVAL

(1) Refer to Figure 6-45. Pull the drive forward to the full extent of the slides; remove the dust cover as described in Paragraph 2.2.

(2) Raise the Servo and Logic PCBAs to the maintenance position.

(3) Remove the cover from the Motor Control PCBA.

(4) Carefully remove cable ties from the cable bundle terminating at connectors on the Motor Control PCBA and to the point where wiring to the drive motor breaks out of the cable bundle.

CAUTION

DO NOT CUT OR NICK ANY WIRES IN CABLE BUNDLE.

(5) Disconnect connectors P405 and P406 from the Motor Control PCBA and separate out of the cable to the drive motor (Figure 6-46).

(6) Remove the belt guard; remove belt from motor pulley only (refer to Paragraph 6.19.1).

(7) Remove the motor pulley from the motor shaft.

(8) Use a thin-shank Phillips head screwdriver to remove four motor mounting screws from the motor mounting plate; refer to Figure 6-45.

(9) Remove the ground wire connected to the top of the drive motor housing.

(10) Remove the drive motor from the mounting plate and from the drive.

6.29.2 DRIVE MOTOR INSTALLATION

From the top side of the drive, proceed as follows. Refer to Figure 6-45.

(1) Position the motor so the motor cable exits from the motor frame as shown in Figure 6-46.

(2) From beneath the drive, install four motor mounting screws through the motor mounting plate. See Figure 6-45. Secure motor to plate.

(3) Install the drive motor pulley on the motor shaft.

(4) Replace belt as noted in Paragraph 6.19.2.

(5) From the top side of the drive, route the motor cable as shown in Figure 6-46. Install connectors P405 and P406 to the Motor Control PCBA.

(6) Retie the motor cable into the existing cable bundle.

(7) Secure the motor cable to the motor frame with a tie wrap.

(8) Replace the ground wire removed in 6.29.1 Step (9).

(9) Replace the cover on the Motor Control PCBA.

(10) Lower the Servo and Logic PCBA into operating position.

(11) Reinstall dust cover and return drive to enclosure.

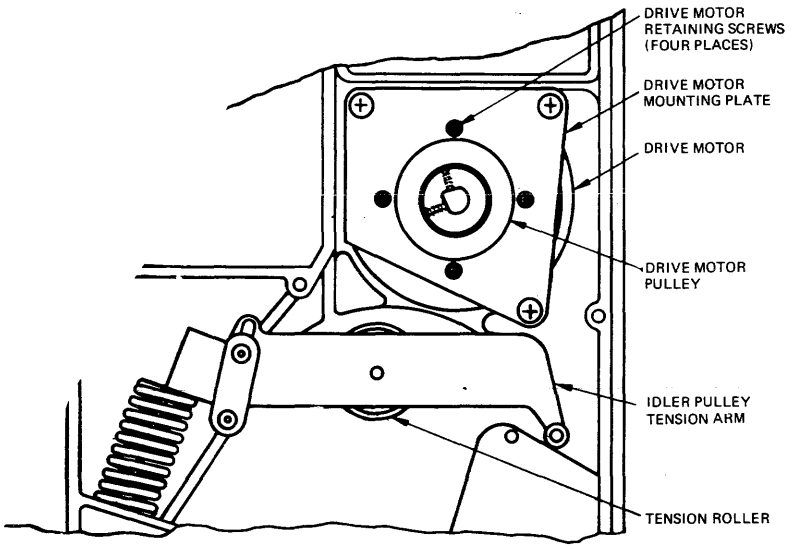


Figure 6-45. Drive Motor Replacement

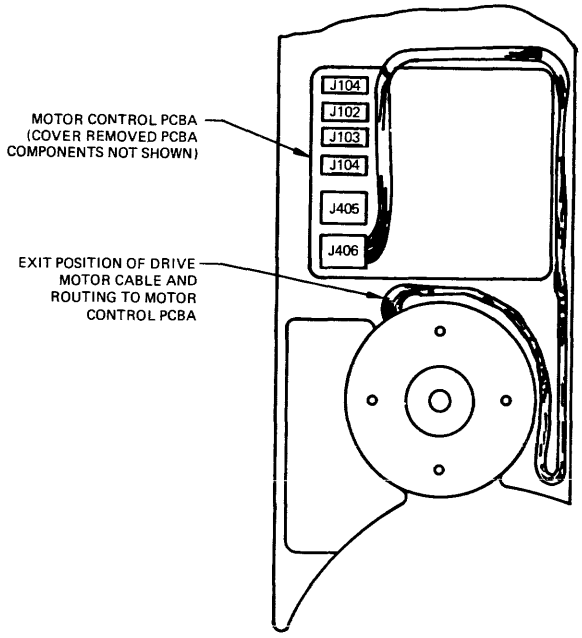


Figure 6-46. Drive Motor Cable Routing

6.30 MAINTENANCE TOOLS

The following is a list of tools required to maintain the disk drive. All tools, except the PCC PD testing equipment aligning and adjustment tools, may be obtained from local sources.

(1) Hex socket key set, 1/16- through 5/32-inch sizes.
(2) Thickness gauge.
(3) Open-end wrenches, sizes 3/16, 1/4, 5/16, and 3/8-inch.
(4) Long-nose pliers.
(5) Phillips screwdriver set.
(6) Standard blade screwdriver set (heavy shank).
(7) Soldering aid.
(8) Soldering iron.
(9) Small diameter (3/16-inch shank, 8-inch long) No. 1 Phillips screwdriver.
(10) Lint-free wipes, e.g., Microwipes TX500.
(11) Lint-free cloth.
(12) Cotton swabs.
(13) Isopropyl alcohol (91 percent).
(14) Torque wrench, 0—15 inch-pounds.
(15) Molex pin extractor (Molex Products, Inc. Part No. HT2285).
(16) Voice Coil Polarity Tester, PCC PD Part No. 103607.
(17) Adapter bowl setup tool, PCC PD Part No. 103619-01.
(18) Head Installation Tool, PCC PD Part No. 104839-02.
(19) Temperature Probe, e.g., Fluke Model 80T150. Range: 20°C to 31°C (68°F to 87.8°F) with an error limit not greater than +0.5°C (+1°F).
(20) Disk Exerciser, PCC PD Model TED02, PCC PD No. 895540-01.
(21) Six-foot extension for Model TED02 Disk Exerciser, PCC PD No. 895035-01A.
(22) Mylar shims 0.127 mm (0.005 inch), PCC PD Part No. 104476-02.
(23) Ball tip hex driver, 9/16-inch.

SECTION VII
PARTS LISTS AND SCHEMATIC/ASSEMBLY DRAWINGS

7.1 INTRODUCTION

This section contains the illustrated parts lists, recommended spare parts lists, interconnect and programming array lists, and schematic/assembly drawings.

7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figures 7-1 through 7-8, used in conjunction with Tables 7-1 through 7-8, respectively, provide identification by PCC PD part number of the mechanical and electrical components of the D3400 Series Dual and Quad Disk Drives. Notations are made when parts do not apply to all model configurations.

7.3 RECOMMENDED SPARE PARTS

Table 7-9 provides a list of the recommended subassembly spare parts for the D3400 Series Dual and Quad Disk Drives. The Customer should always furnish the model number and the serial number of the disk drive when ordering parts.

An additional recommended spare parts list containing the part number, description, current price for component parts, subassembly parts, and special tools is also available. This list can be obtained by providing the unit part number, from the ID label on the disk drive, to the Logistics Section, PCC PD, 9600 Irondale Avenue, Chatsworth, CA 91311.

7.4 PART NUMBER CROSS REFERENCE LIST

Table 7-10 provides a cross reference from PCC PD component series part numbers to the basic part identification.

7.5 INTEGRATED CIRCUIT PIN SUMMARY

A summary of the power and ground pins for the various integrated circuits employed in the disk drive is contained in Table 7-11. A summary of the function control for certain integrated circuits is listed in Table 7-12.

7.6 PCBA INTERCONNECTIONS

Interconnections between PCBAs installed in the disk drive are listed in Table 7-13 and illustrated in Figure 7-9*.

*Foldout drawing, see end of this Section.

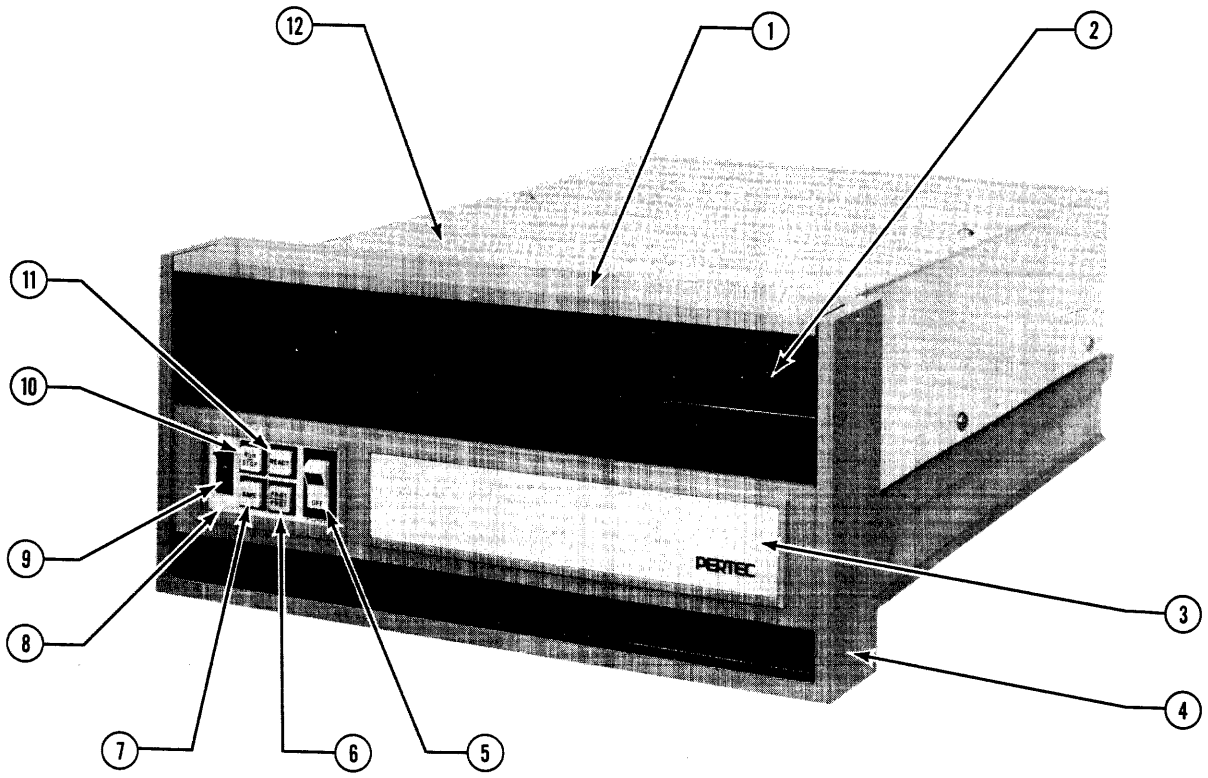


Figure 7-1. D3000 Extension Disk Drive, Photo Parts Index, Front View

Table 7-1
D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-1		
1	102644-01	Door Handle (Front Load Only)
2	102643-01	Door
3	102647-01	Accent Panel White with Logo
	102647-02	Accent Panel White without Logo
	102647-03	Accent Panel Clear with Logo
	102647-04	Accent Panel Clear without Logo
4	102703-01	Bezel Assembly (Front Load Only)
	102704-01	Bezel Assembly (Top Load Only)
5	506-1816	ON/OFF Power Switch/Indicator
6	103663-30	PROT/PROT Switch Assembly
	659-0730	Lamp, Switch
7	103663-28	SAFE Switch Assembly
	659-0730	Lamp, Switch
8	104616-01	Switch Panel Cover
9	102759-01	Unit Selector Switch
10	103663-27	RUN/STOP Switch Assembly
	659-0730	Lamp, Switch
11	103663-29	READY Switch Assembly
	659-0730	Lamp, Switch
12	103746-01	Dust Cover (Front Load Only)
	103747-01	Dust Cover (Top Load Only)
	615-0084	Screw (8)
	612-1022	Washer (8)
Not Shown	103670-01	Slide Assembly with Hardware

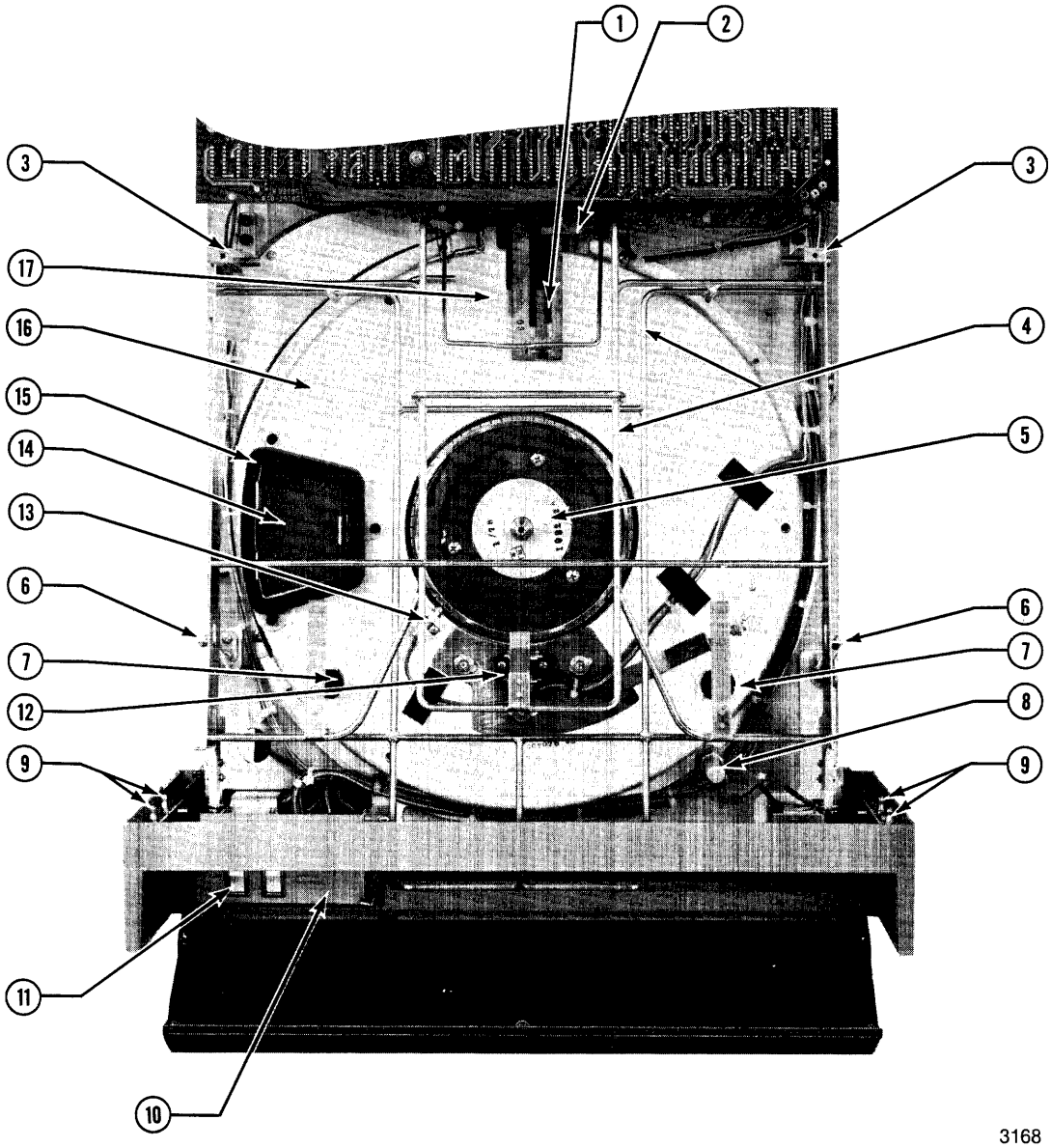


Figure 7-2. D3000 Extension Disk Drive, Photo Parts Index (Front Load Models)

Table 7-2
D3000 Extension Disk Drive Photo Parts Index (Front Load Models)

Figure and Index No.	Part Number	Description
Figure 7-2		
1	104501-03	Scale Assembly
2	108266-02	Left Head Cam
3	103486-01	Pivot Support
4	103472-01	Cartridge Receiver Wire Form Assembly
5	108222-02	Spindle Assembly
6	103488-01	Receiver Spring
7	102627-02	Cartridge Support Post
8	102626-01	Cartridge Pin
9	615-4997 604-2600	Ball Stud Hex Nut
10	102658-04	Write Protect Plate
11	102761-02 506-0001	Write Protect Switch Assembly Rocker Switch
12	103481-01	Sector Sensor Assembly (Photo-Electric)
13	104621-06	Transducer Assembly (Magnetic Only)
14	102669-01	Air Screen
15	103474-01	Air Duct Gasket
16	103478-03	Lower Disk Cover
17	102683-03	Disk Guide

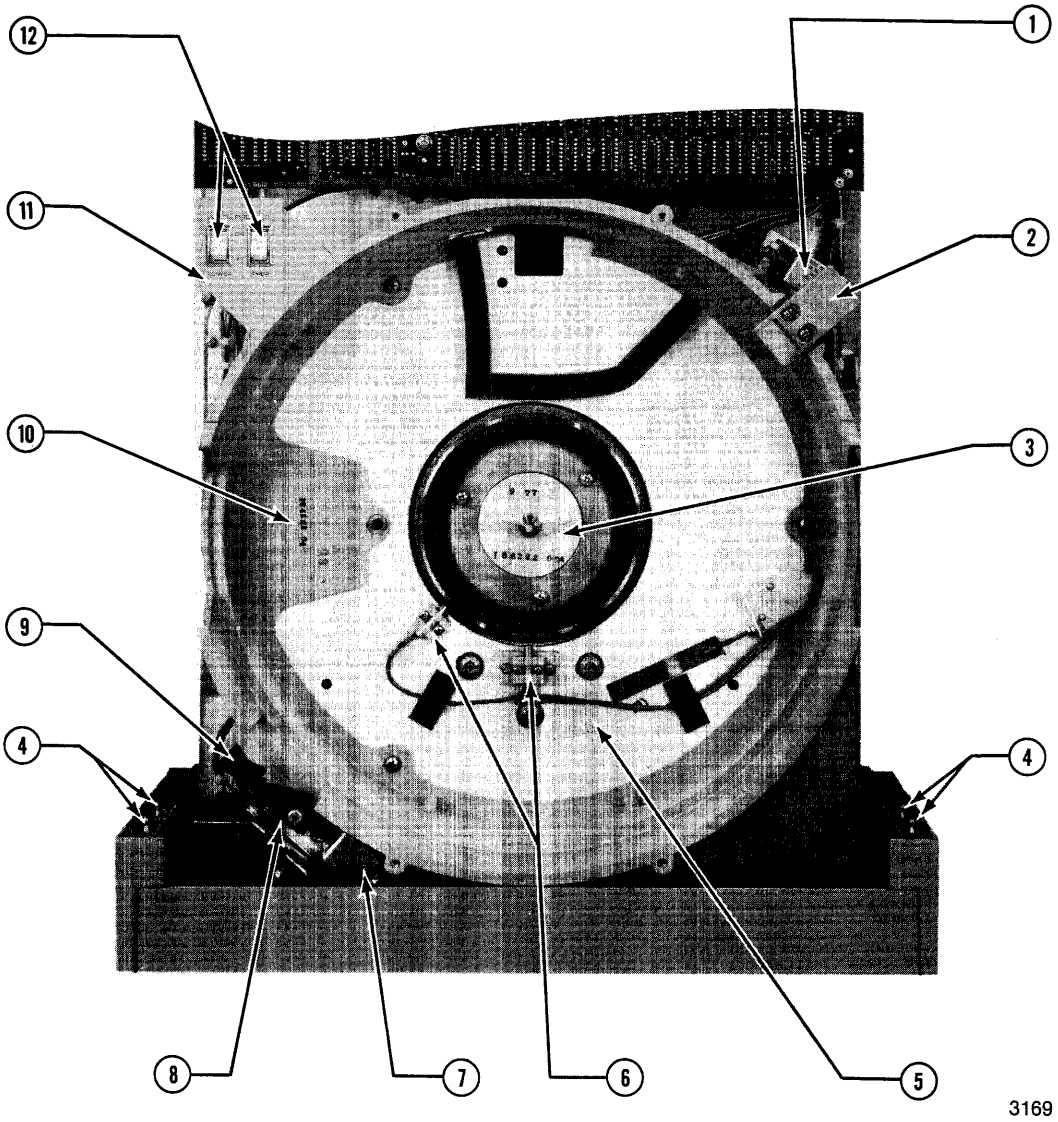


Figure 7-3. D3000 Extension Disk Drive, Photo Parts Index (Top Load Models)

Table 7-3
D3000 Extension Disk Drive Photo Parts Index (Top Load Models)

Figure and Index No.	Part Number	Description
Figure 7-3		
1	108230-01	Thermistor Mechanism Assembly
	517-0003	Solenoid Only
	101110-01	Spring
2	103479-01	Cartridge Retainer
	600-0806	Screw
3	108222-02	Spindle Assembly
4	615-4997	Ball Stud
	604-2600	Nut
5	103467-01	Sector Adjust Plate Assembly
6	102764-02	Transducer Assembly (Upper and Lower)
	104621-06	Transducer Assembly (Lower Only)
	104621-07	Transducer Assembly (Upper Only)
7	102754-02	Solenoid Assembly
	517-0001	Solenoid Only
	101110-01	Spring
8	102762-02	Cartridge Lock Switch Assembly
9	102612-02	Cartridge Lock Arm
10	104503-04	Cartridge Adapter Assembly
11	102658-01	Write Protect Name Plate
12	506-0001	Rocker Switch

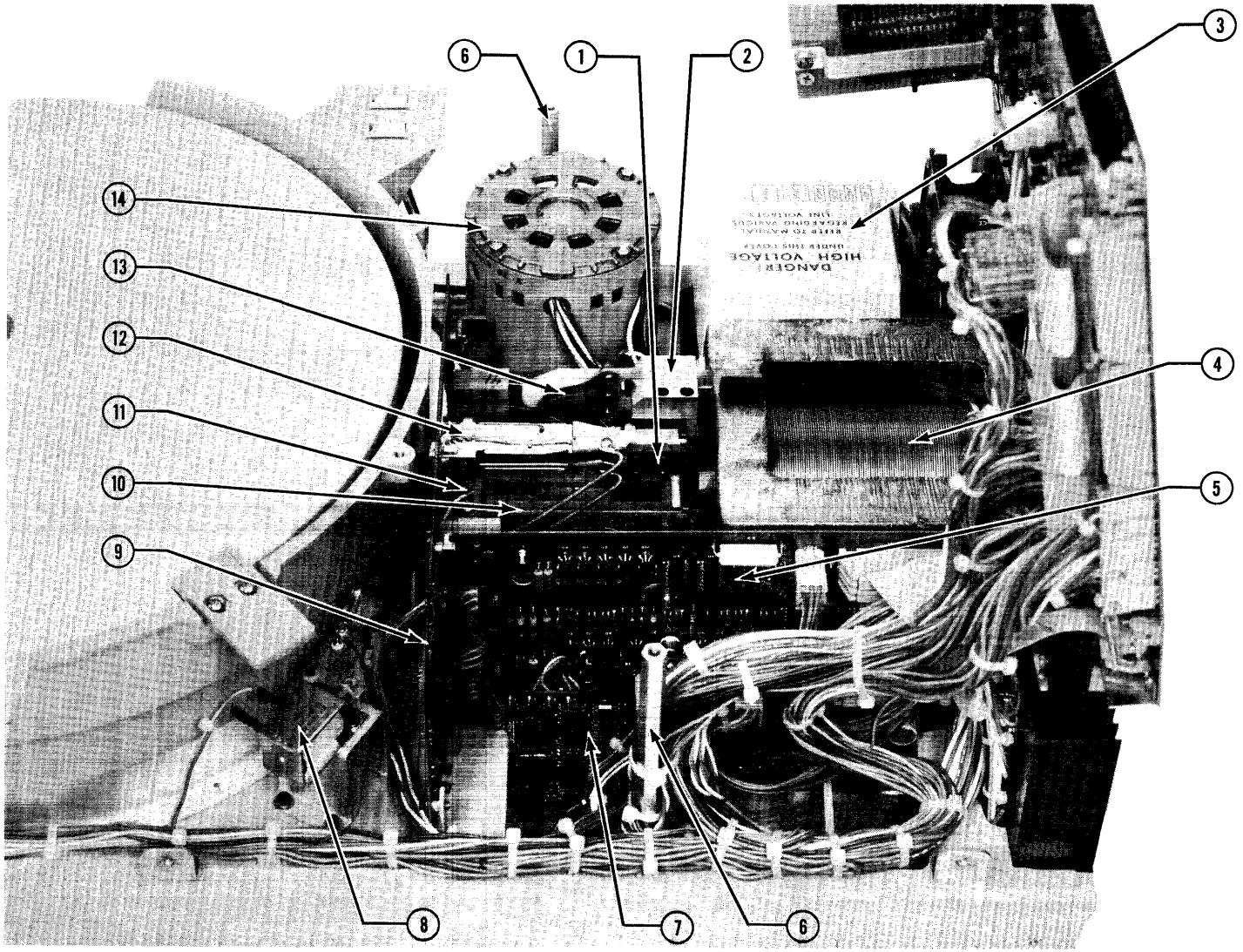


Figure 7-4. D3000 Extension Disk Drive, Photo Parts Index

Table 7-4
D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-4		
1	103432-01	Head Clamp Plate
	102853-01	Clamp Plate Spacer
	602-0614	Socket Head Screw
	603-3604	Screw
Not Shown	104070-01	Lower Head Clamps (3)
	602-0612	Socket Head Screw
2	108279-01	Counter Weight
	602-0608	Socket Head Screw
3	102666-01	Protective Cover
4	108220-01	Voice Coil Assembly
5	108141-*	Read/Write PCBA
6	102709-01	Standoff
7	108176-*	Temperature Compensation PCBA
8	108230-01	Thermistor Mechanism Assembly
	517-0003	Solenoid Only
	101110-01	Spring
9	108146-*	Matrix Select PCBA
10	108224-01	Carriage Scale Assembly
	104501-03	Scale Only
11	104514-02	Position Transducer Assembly
	104500-02	Sensor Receiver Assembly
	103499-01	Lamp and Lens Assembly
12	526-**	Read/Write Head
13	104512-01	Flex Strip Assembly
14	103579-02	Drive Motor Assembly

*Order as indicated on PCBA.
**Refer to Table 7-9 for specific part numbers.

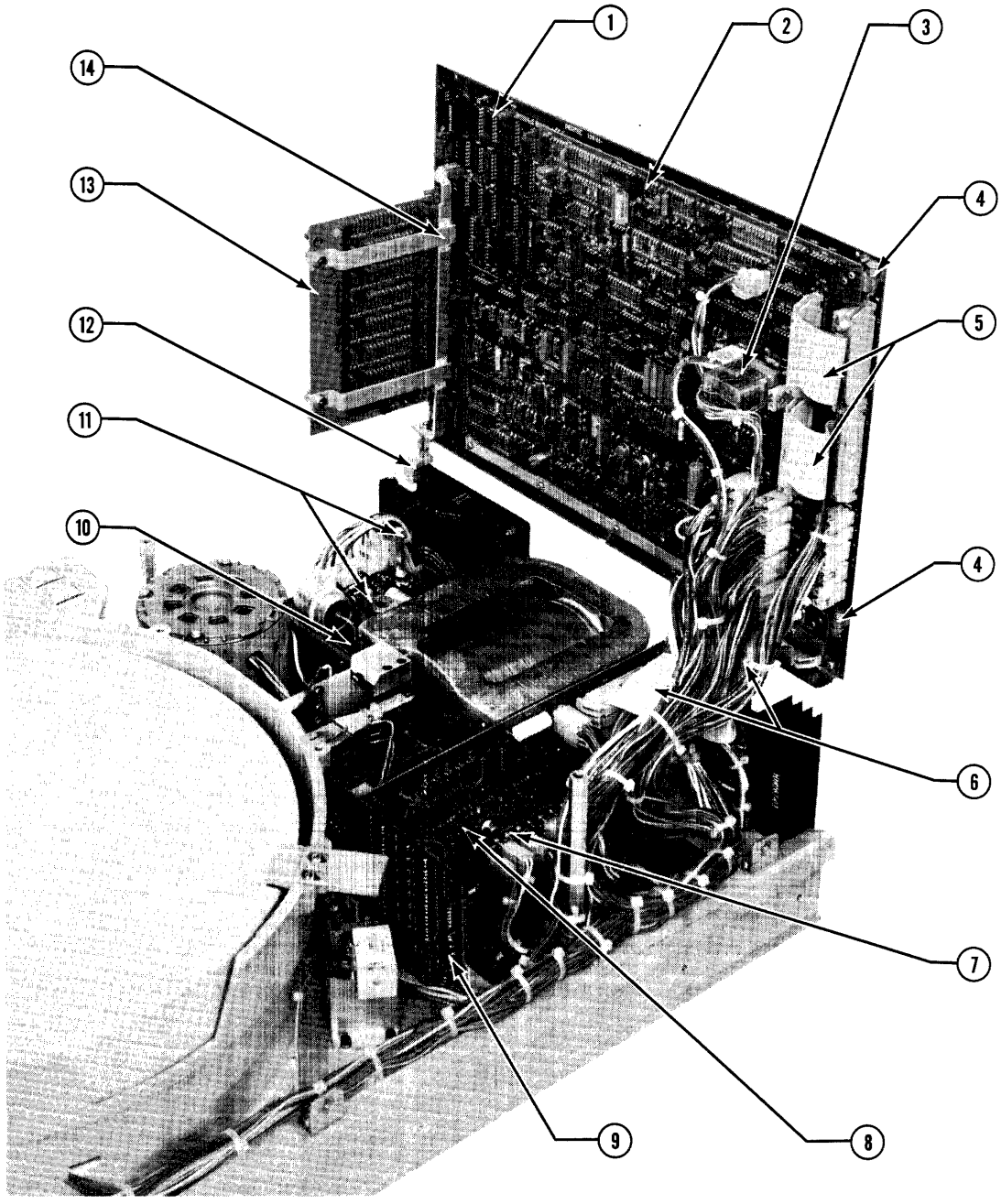


Figure 7-5. D3000 Extension Disk Drive, Photo Parts Index, PCBAs in Extended Position

Table 7-5
D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-5		
1	XXXXXX-*	Logic PCBA
2	108131-*	Servo PCBA
3	502-1243 502-6113	Relay Relay Socket
4	615-0082 609-5901	Clevis Pin Pin
5	102755-01	Interboard Cable Assembly
6	102755-04	Interboard Cable Assembly
7	108176-*	Temperature Compensation PCBA
8	108141-*	Read/Write PCBA
9	108146-*	Matrix-Select PCBA
10	103571-01 103571-02	Motor Control PCBA, 90—125v ac Motor Control PCBA, 190—250v ac
11	108284-01	Standoff
12	108270-01	Bracket
13	102801-*	I/O Terminator PCBA
14	108271-01	Strain Relief

*Order as indicated on PCBA.

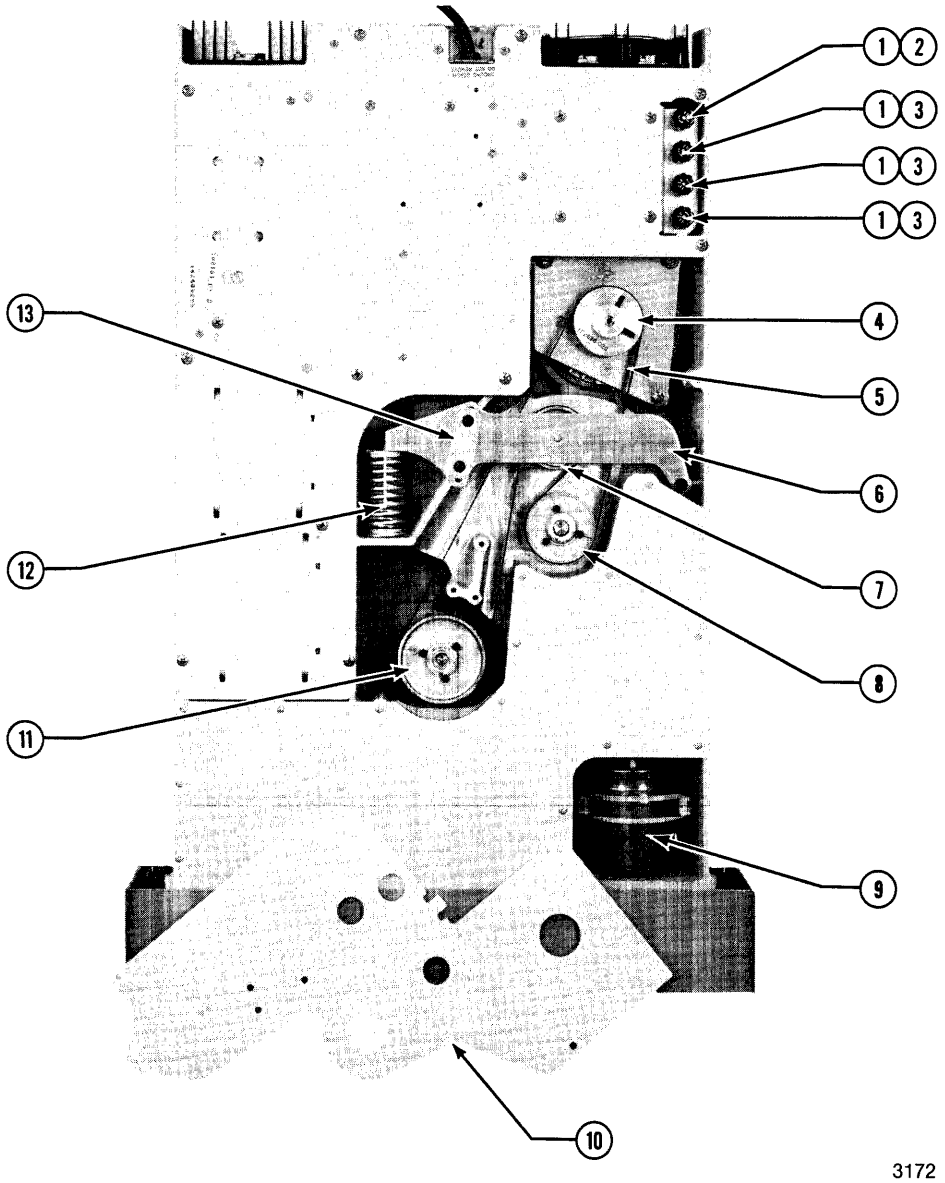


Figure 7-6. D3000 Extension Disk Drive, Photo Parts Index, Bottom View

Table 7-6

D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-6		
1	658-2038	Fuse Holder, Panel Mounted, 3AG Miniature
2	663-3700	Fuse, F1, 10A, 250v, Slo-Blo, 95—125v Operation
	663-2052	Fuse, F1, 5A, 250v, Slo-Blo, 190—250v Operation
3	663-3100	Fuse, F2, F3, F4, 10A, 32v, 3AG, Fast-Blo
4	103642-01	Drive Motor Pulley, 1500 rpm 60 Hz Drives
	103642-02	Drive Motor Pulley, 2400 rpm 60 Hz Drives or 1500 rpm 50 Hz drives
	103642-03	Drive Motor Pulley, 2400 rpm 50 Hz Drives
5	102634-01	Drive Belt, 60 Hz Operation
	102634-02	Drive Belt, 50 Hz Operation
6	108256-01	Idler Arm
	615-0107	Screw
	616-0011	Spring
7	102637-01	Tension Idler Assembly
	615-0083	Screw
8	102722-01	Blower Pulley, 1500 rpm Drives
	102722-02	Blower Pulley, 2400 rpm Drives
9	134-6293	Capacitor
10	108263-01	Belt Guard
	103764-01	Static Discharge Kit
	600-0007	Screw
	605-0000	Lock Washer
11	102635-01	Spindle Pulley, 2400 rpm Drives
	102635-02	Spindle Pulley, 1500 rpm Drives
12	102667-01	Spring
13	103584-01	Thrust Washer — Teflon
	103584-02	Thrust Washer — Steel
	615-0107	Screw

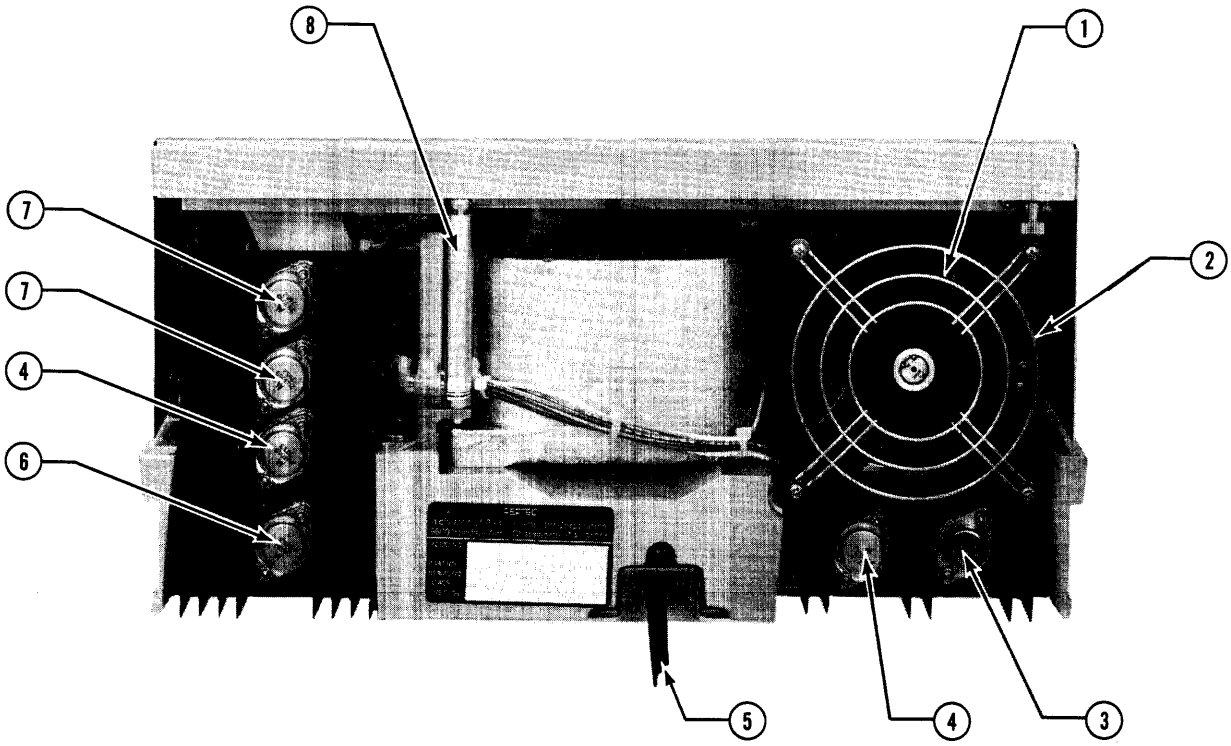


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Figure 7-7. D3000 Extension Disk Drive, Photo Parts Index, Rear View

Table 7-7
D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-7		
1	518-0005	Fan
2	518-0006	Fan Grill
3	400-0323	Linear IC
4	200-6058	Transistor
5	108190-01 108190-02 108190-03	Power Cord Assembly, 95—125v ac, 50/60 Hz Power Cord Assembly, 190—250v ac, 60 Hz Power Cord Assembly, 190—250v ac, 50 Hz
6	200-6051	Transistor
7	200-3055	Transistor
8	103466-02 612-1017 616-0026	Pivot Standoff Pivot Sleeve Spring

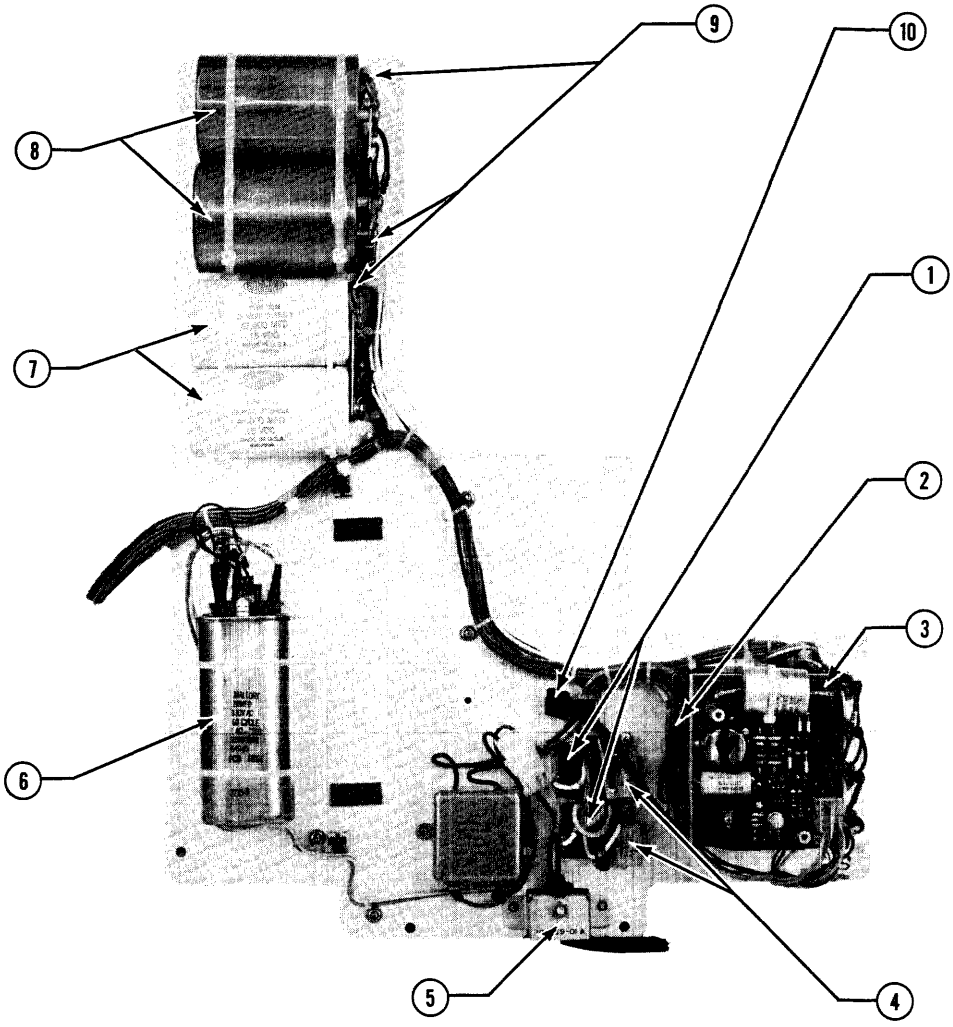

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Figure 7-8. D3000 Extension Disk Drive, Photo Parts Index (Power Supply Assembly)

Table 7-8
D3000 Extension Disk Drive Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-8		
1	320-1010	Rectifier Bridge
2	511-3600	Power Transformer
3	103571-01 103571-02	Motor Control PCBA, 90—125v ac Motor Control PCBA, 190—250v ac
4	131-2051	Capacitor
5	108190-01 108190-02 108190-03	Power Cord Assembly, 95—125v ac, 50/60 Hz Power Cord Assembly, 190—250v ac, 60 Hz Power Cord Assembly, 190—250v ac, 50 Hz
6	140-1003 140-1203 661-0004	Capacitor, 1500 rpm Units Capacitor, 2400 rpm Units Tie Wrap
7	134-4792 661-0013	Capacitor Tie Wrap
8	134-3393 661-0013	Capacitor Tie Wrap
9	103-4715	Resistor
10	692-0787	Fan Plug and Cord Assembly

Table 7-9
Recommended Spare Parts List

	Description	Part Number
1.	Logic PCBA	XXXXXX-*
2.	Servo PCBA	108131-*
3.	Read/Write PCBA	108141-*
4.	Temperature Compensation PCBA	108176-*
5.	Matrix-Select PCBA	108146-*
6.	Disk Platter	522-0016
7.	Lamp and Lens Assembly	103499-01
8.	Drive Motor Assembly	103579-02
9.	Motor Control PCBA, 95—125v ac Motor Control PCBA, 190—250v ac	103571-01 103571-02
10.	Head, Lower, 2200 BPI, 200 TPI, 1500 rpm (RA) Head, Upper, 2200 BPI, 200 TPI, 1500 rpm (RA) Head, Lower, 2200 BPI, 200 TPI, 1500 rpm (RO) Head, Upper, 2200 BPI, 200 TPI, 1500 rpm (RO) Head, Lower, 2200 BPI, 200 TPI, 1500 rpm (RO) Head, Upper, 2200 BPI, 200 TPI, 1500 rpm (RO)	526-0314 526-0315 526-0034 526-0035 526-0036 526-0037
10A.	Head, Lower, 2200 BPI, 200 TPI, 2400 rpm (RA) Head, Upper, 2200 BPI, 200 TPI, 2400 rpm (RA) Head, Lower, 2200 BPI, 200 TPI, 2400 rpm (RO) Head, Upper, 2200 BPI, 200 TPI, 2400 rpm (RO) Head, Lower, 2200 BPI, 200 TPI, 2400 rpm (RO) Head, Upper, 2200 BPI, 200 TPI, 2400 rpm (RO)	526-0316 526-0317 526-0038 526-0039 526-0040 526-0041
11.	Sensor Receiver Assembly	104500-02
12.	Scale Assembly	104501-03
13.	Fuse, 10A, 250v, Slo-Blo, 95—125v ac Fuse, 5A, 250v, Slo-Blo, 190—250v ac	663-3700 663-2052
14.	Fuse, 10A, 32v, 3AG, Fast-Blo	663-3100
15.	Filter (Air)	614-0006
16.	ON/OFF Power Switch/Indicator	506-1816
17.	RUN/STOP Switch Assembly	103663-27
18.	SAFE Switch Assembly	103663-28
19.	READY Switch Assembly	103663-29
20.	PROT/PROT Switch Assembly	103663-30
21.	Lamp, Switch	659-0730

*Order as indicated on PCBA.
RA = Radially Aligned
RO = Radially Offset

Table 7-10
Part Number Cross Reference

Pertec Part No.	Manufacturer	Manufacturer Part No.*/Description
Composition Resistors	(Comply with MIL-R-11)	
100-0395		3.9 ohms ±5%, ¼w
100-1005		10 ohms ±5%, ¼w
100-1015		100 ohms ±5%, ¼w
100-1025		1.5k ohms ±5%, ¼w
100-1055		1 meg ohm ±5%, ¼w
100-1235		150 ohms ±5%, ¼w
100-1525		1.5k ohms ±5%, ¼w
100-1535		15k ohms ±5%, ¼w
100-1815		180 ohms ±5%, ¼w
100-1825		1.8k ohms ±5%, ¼w
100-1845		180k ohms ±5%, ¼w
100-2215		220 ohms ±5%, ¼w
100-2225		2.2k ohms ±5%, ¼w
100-2235		22k ohms ±5%, ¼w
100-2705		27 ohms ±5%, ¼w
100-2725		2.7k ohms ±5%, ¼w
100-3305		33 ohms ±5%, ¼w
100-3315		390 ohms ±5%, ¼w
100-3325		3.3k ohms ±5%, ¼w
100-3925		3.9k ohms ±5%, ¼w
100-4705		47 ohms ±5%, ¼w
100-4715		470 ohms ±5%, ¼w
100-4725		4.7k ohms ±5%, ¼w
100-5625		5.6k ohms ±5%, ¼w
100-6805		68 ohms ±5%, ¼w
100-6815		680 ohms ±5%, ¼w
100-8215		820 ohms ±5%, ¼w
100-8235		82k ohms ±5%, ¼w
101-1025		1k ohms ±5%, ½w
101-1505		15 ohms ±5%, ½w
101-1515		150 ohms ±5%, ½w
101-2205		22 ohms ±5%, ½w
101-2715		270 ohms ±5%, ½w
101-3305		33 ohms ±5%, ½w
101-3325		3.3k ohms ±5%, ½w
101-3915		390 ohms ±5%, ½w
101-4715		470 ohms ±5%, ½w
101-6805		68 ohms ±5%, ½w
101-8205		82 ohms ±5%, ½w
102-5615		560 ohms ±5%, 1w
102-8205		82 ohms ±5%, 1w
103-1215		120 ohms ±5%, 2w
103-1815		180 ohms ±5%, 2w
103-4705		47 ohms ±5%, 2w
Precision Resistors		
104-1000		100 ohms ±1%, ¼w
104-1001		1k ohms ±1%, ¼w
104-1002		10k ohms ±1%, ¼w

Table 7-10
Part Number Cross Reference (Continued)

Pertec Part No.	Manufacturer	Manufacturer Part No.*/Description
Precision Resistors (Cont.)		
104-1003		100k ohms ± 1%, ¼ w
104-1100		110 ohms ± 1%, ¼ w
104-1101		1.1k ohms ± 1%, ¼ w
104-1102		11k ohms ± 1%, ¼ w
104-1211		1.21k ohms ± 1%, ¼ w
104-1330		133 ohms ± 1%, ¼ w
104-1331		1.33k ohms ± 1%, ¼ w
104-1332		13.3k ohms ± 1%, ¼ w
104-1623		162k ohms ± 1%, ¼ w
104-1781		1.78k ohms ± 1%, ¼ w
104-1782		17.8k ohms ± 1%, ¼ w
104-1961		1.96k ohms ± 1%, ¼ w
104-1962		19.6k ohms ± 1%, ¼ w
104-2151		2.15k ohms ± 1%, ¼ w
104-2152		21.5k ohms ± 1%, ¼ w
104-2370		237 ohms ± 1%, ¼ w
104-2610		261 ohms ± 1%, ¼ w
104-2611		2.61k ohms ± 1%, ¼ w
104-2612		26.1k ohms ± 1%, ¼ w
104-2870		287 ohms ± 1%, ¼ w
104-3481		3.48k ohms ± 1%, ¼ w
104-3831		3.83k ohms ± 1%, ¼ w
104-3832		38.3k ohms ± 1%, ¼ w
104-3833		383 ohms ± 1%, ¼ w
104-3482		34.8k ohms ± 1%, ¼ w
104-3483		348k ohms ± 1%, ¼ w
104-4220		422 ohms ± 1%, ¼ w
104-4221		4.22k ohms ± 1%, ¼ w
104-4222		42.2k ohms ± 1%, ¼ w
104-4641		4.64k ohms ± 1%, ¼ w
104-4753		475k ohms ± 1%, ¼ w
104-5110		511 ohms ± 1%, ¼ w
104-5111		5.11k ohms ± 1%, ¼ w
104-5113		511k ohms ± 1%, ¼ w
104-5620		562 ohms ± 1%, ¼ w
104-5621		5.62k ohms ± 1%, ¼ w
104-6192		61.9k ohms ± 1%, ¼ w
104-6811		6.81k ohms ± 1%, ¼ w
104-6812		68.1k ohms ± 1%, ¼ w
104-7500		750 ohms ± 1%, ¼ w
104-8252		82.5k ohms ± 1%, ¼ w
104-9090		909 ohms ± 1%, ¼ w
104-9092		90.9k ohms ± 1%, ¼ w
104-9093		909k ohms ± 1%, ¼ w
107-1000		100 ohms ± 1%, 1/8w
107-1001		1k ohms ± 1%, 1/8w
107-1002		10k ohms ± 1%, 1/8w
107-1003		100k ohms ± 1%, 1/8w
107-1101		1.1k ohms ± 1%, 1/8w

Table 7-10
Part Number Cross Reference (Continued)

Pertec Part No.	Manufacturer	Manufacturer Part No.*/Description
Precision Resistors (Cont.)		
107-1102		11k ohms ±1%, 1/8w
107-1211		1.21k ohms ±1%, 1/8w
107-1332		13.3k ohms ±1%, 1/8w
107-1471		1.47k ohms ±1%, 1/8w
107-1781		1.78k ohms ±1%, 1/8w
107-1782		17.8k ohms ±1%, 1/8w
107-1961		1.96k ohms ±1%, 1/8w
107-1962		19.6k ohms ±1%, 1/8w
107-1963		196k ohms ±1%, 1/8w
107-2152		21.5k ohms ±1%, 1/8w
107-2611		2.61k ohms ±1%, 1/8w
107-2612		26.1k ohms ±1%, 1/8w
107-2870		287 ohms ±1%, 1/8w
107-3482		34.8k ohms ±1%, 1/8w
107-3483		348k ohms ±1%, 1/8w
107-3832		38.3k ohms ±1%, 1/8w
107-4221		4.22k ohms ±1%, 1/8w
107-4222		42.2k ohms ±1%, 1/8w
107-5110		511 ohms ±1%, 1/8w
107-5111		5.11k ohms ±1%, 1/8w
107-5112		51.1k ohms ±1%, 1/8w
107-5113		511k ohms ±1%, 1/8w
107-5620		562 ohms ±1%, 1/8w
107-6192		61.9k ohms ±1%, 1/8w
107-6811		6.81k ohms ±1%, 1/8w
107-6812		68.1k ohms ±1%, 1/8w
107-8252		82.5k ohms ±1%, 1/8w
107-9090		909 ohms ±1%, 1/8w
109-0003		0.10 ohms ±3%, 5w
113-0111		10 ohms ±1%, 1w
Variable Resistors		
121-1020	Beckman	79PR1K, Variable, 1k ohms ±10%, ¾w
121-1030	Beckman	79PR10K, Variable, 10k ohms ±10%, ¾w
121-5020	Beckman	79PR5K, Variable, 5k ohms ±10%, ¾w
123-5020	Spectrol	53-1-1-502, Variable, 5k ohms ±10%, ½w
Dipped Mica Capacitors	(Comply with MIL-C-5)	
130-1005		10 pf ±5%, 500v dc
130-1015		100 pf ±5%, 500v dc
130-1515		150 pf ±5%, 500v dc
130-2205		22 pf ±5%, 500v dc
130-2215		220 pf ±5%, 500v dc
130-3305		33 pf ±5%, 500v dc
130-4705		47 pf ±5%, 500v dc
130-4715		470 pf ±5%, 500v dc
130-5605		56 pf ±5%, 500v dc
130-6805		68 pf ±5%, 500v dc
130-7515		750 pf ±5%, 500v dc

Table 7-10
Part Number Cross Reference (Continued)

PCC Part No.	Manufacturer	Manufacturer Part No.*/Description
Mylar Film Capacitors		
131-1020	TRW	663uw series, 0.001 μfd ± 10%, 100v dc
131-1030	TRW	663uw series, 0.01 μfd ± 10%, 100v dc
131-1040	TRW	663uw series, 0.10 μfd ± 10%, 100v dc
131-2220	TRW	663uw series, 0.0022 μfd ± 10%, 100v dc
131-4720	TRW	663uw series, 0.0047 μfd ± 10%, 100v dc
Solid Tantalum Polarized Capacitors		
132-1062	Mallory	TIM106M010POW, 10 μfd ± 20%, 10v dc
132-2752	Mallory	TIM275M035POW, 2.7 μfd ± 20%, 35v dc
139-2244	Kemet	T310A225M020AS, 2.2 μfd ± 20%, 20v dc
139-2262	Kemet	T310B226M015AS, 22 μfd ± 20%, 15v dc
139-3352	Kemet	T310A335M015AS, 3.3 μfd ± 20%, 15v dc
Aluminum Foil Polarized Capacitor		
134-2680	Mallory	TOW282N025N1R3P, 2600 μfd + 100% − 10%, 20v dc
Ceramic Capacitors		
135-1002	Centralab	DD-102, 0.001 μfd ± 10%, 1000v dc
135-4742	Erie	8131-050651-474M, 0.47 μfd ± 20%, 50v dc
Transistors		
200-3053	RCA	2N3053, NPN, Silicon Annular, T0-5
200-3055	RCA	2N3055, NPN, Silicon Power, T0-3
200-3251	Motorola	2N3251, PNP, Switching, T0-18
200-3771	RCA	2N3771, NPN, Silicon Power, T0-3
200-4123	Motorola	2N4123, NPN, Silicon, T0-92
200-4125	Motorola	2N4125, PNP, Silicon, T0-92
200-4400	Motorola	2N4400, NPN, Silicon, T0-92
200-4402	Motorola	2N4402, PNP, Silicon, T0-92
200-5321	RCA	2N5321, NPN, Silicon, T0-5
200-5323	RCA	2N5323, PNP, Silicon, T0-5
200-6051	Motorola	2N6051, PNP, Power Darlington, T0-3
200-6058	Motorola	2N6058, NPN, Power Darlington, T0-3
200-6282	Motorola	2N6282, NPN, Power Darlington, T0-3
200-6285	Motorola	2N6285, PNP, Power Darlington, T0-3
Field Effect Transistors		
204-4943	National	2N4393, N-Channel, Switching, T0-18
Diodes		
300-4002	Motorola	1N4002, Rectifier, 1A, 100 PIV, D0-41
300-4446	Components, Inc.	1N4446, Switching, 75 PIV, D0-7
Zener Diodes		
300-0475	Motorola	1N4732A, Zener, 4.7v dc ± 5%, 1w, D0-41
330-0515	Motorola	1N4733A, Zener, 5.1v dc ± 5%, 1w, D0-41
330-1005	Motorola	1N4740A, Zener, 10v ± 5%, 1w, D0-41

Table 7-10
Part Number Cross Reference (Continued)

PCC Part No.	Manufacturer	Manufacturer Part No.*/Description
Zener Diodes (Cont.)		
330-1205	Motorola	1N4742A, Zener, 12v ±5%, 1w
331-0275	Motorola	1N5223B, Zener, 2.7v dc ±5%, 500mw, D0-7
331-0395	Motorola	1N5228B, Zener, 3.9v dc ±5%, 500mw, D0-7
331-0515	Motorola	W5231B, Zener, 5.1v dc ±5%, 500mw, D0-7
331-0605	Motorola	1N5233B, Zener, 6v dc ±5%, 500mw, D0-7
Light Emitting Diode		
301-0055	Optron	OR133W-3, Light Emitting, Infra Red, T0-46
Operational Amplifiers		
400-0307	National	LM307N, IC, Op Amp
400-0319	National	LM319N, IC, Dual Comparator
400-0592	Signetics	NE592A, IC, Op Amp
400-2741	National	LM741CN, IC, Op Amp
400-5558	National	LM1458N, IC, Dual Op Amp
Relays		
502-1244	Potter & Brumfield	R10E-3725-2, 12v dc, 4PDT, Contact Rating 7A at 28v dc
Inductors		
515-1015	Delevan	1537-76, 100 μH ±5%, 4.5 ohms
515-3305	Delevan	1537-52, 33 μH ±5%, 2.9 ohms
515-6805	Delevan	1537-68, 68 μH ±5%, 3.3 ohms
Crystals		
524-0002	Northern Eng Lab	NE12, 10.00 MHz ±0.005
Adhesives		
667-0050	DuPont	RTV 732, Silastic

*or equivalent

Table 7-11
IC Power and Ground Pin Summary

Type	Gnd	+5V	—5V	+V	—V
715	—	—	—	13	10
733	—	—	—	10	5
741	—	—	—	11	6
7400	7	14	—	—	—
7402	7	14	—	—	—
7404	7	14	—	—	—
7405	7	14	—	—	—
7410	7	14	—	—	—
7413	7	14	—	—	—
7430	7	14	—	—	—
7450	7	14	—	—	—
7476	13	5	—	—	—
7483	12	5	—	—	—
7486	7	14	—	—	—
7493	10	5	—	—	—
7496	12	5	—	—	—
74161	8	16	—	—	—
74164	7	14	—	—	—
74193	8	16	—	—	—
75107	7	14	13	—	—
75451	4	8	—	—	—

Table 7-12
Function Control Summary

Type	Clocking Transition	Clearing Level	Loading Level
7476	H to L	Low	—
74H106	H to L	Low	—
7493	H to L	High	—
7496	L to H	Low	High
74161	L to H	Low	Low (and clock)
74164	L to H	Low	—
74193	L to H	High	Low

Table 7-13
PCBA Interconnections

Logic PCBA	
J101	Interface Connector
J102	Interface Connector
J103	Interboard Connector (R/W PCBA J305)
J104	Interboard Connector (Servo PCBA J201)
J105	Interboard Connector (Servo PCBA J202)
J106	Power Link Cable (Servo PCBA J210)
J107	Power Link Cable (R/W PCBA J304)
J108	Write Protect Switches
J109	Cartridge Switch/Door Lock Solenoids and Cartridge Lock Solenoid
J110	Control Panel Switches
J111	Control Panel Lamps and Temperature Compensation PCBA
J112	Upper Index (Sector) Sensor/Lower Index (Phase) Sensor
J114	Current Cylinder Address to Temperature Compensation PCBA
Servo PCBA	
J201	Interboard Connector (Logic PCBA J104)
J202	Interboard Connector (Logic PCBA J105)
J203	Position and Velocity Transducer
J204	Heatsink No. 1
J205	Positioner Coils
J206	Emergency Unload Capacitor
J207	Cartridge Lock Solenoid
J208	Heatsink No. 2
J210	Power Link Cable to Logic PCBA
J212	Unregulated Power from Power Supply
J213	Trigger to Motor Control PCBA
J214	Emergency Unload Driver
J215	Temperature Compensation PCBA Offset
J216	+5v dc Auxiliary Regulator on Heatsink
J217	+5v dc Auxiliary Power to Logic PCBA J110
Read/Write PCBA	
J304	Power Link Cable from Logic PCBA
J305	Interboard Connector (Logic PCBA J103)
J306	Interboard Connector (Temperature Compensation PCBA J506)
J310	R/W Data Signals to Matrix PCBA J610
J311	Head Select Signals from Matrix PCBA J611
Motor Control PCBA	
J401	Trigger from Servo PCBA (Servo PCBA J213)
J402	AC Power from Power Supply Circuits
J403	Motor Capacitor (115v Operation)
J404	Motor Capacitor (220v Operation)
J405	Drive Motor (115v Operation)
J406	Drive Motor (220v Operation)
Temperature Compensation PCBA	
J502	Logic PCBA — Power Link Cable
J503	Logic PCBA Current Address
J504	Servo PCBA Temperature Compensation Offset
J505	Thermistor Cable Assembly
J506	Interboard Connector (R/W PCBA J306)
R/W Selection Matrix and Preamp	
J600 Thru J607	Head 0 through Head 7
J610	Read Signals, Write Drivers
J611	Head Select Signals

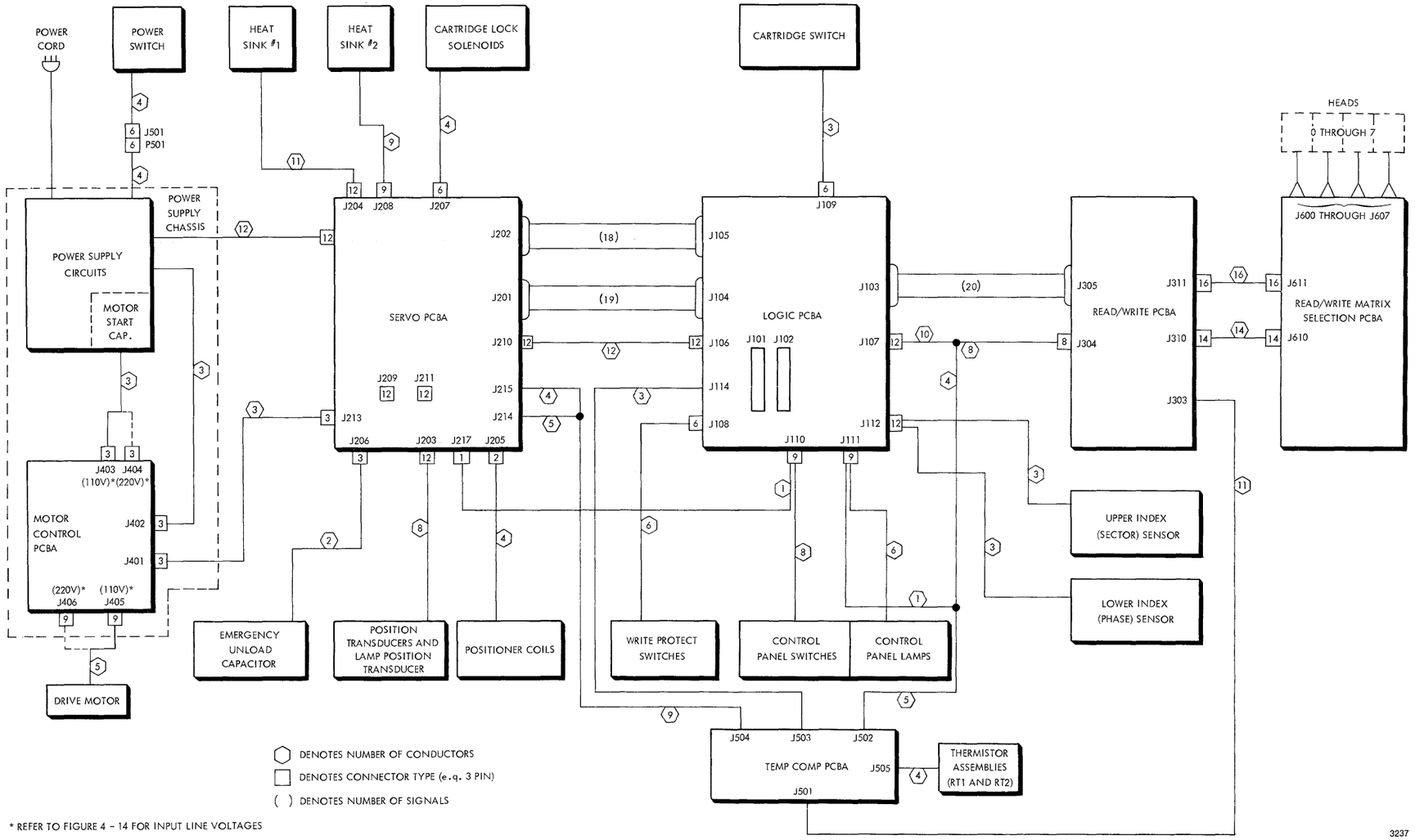
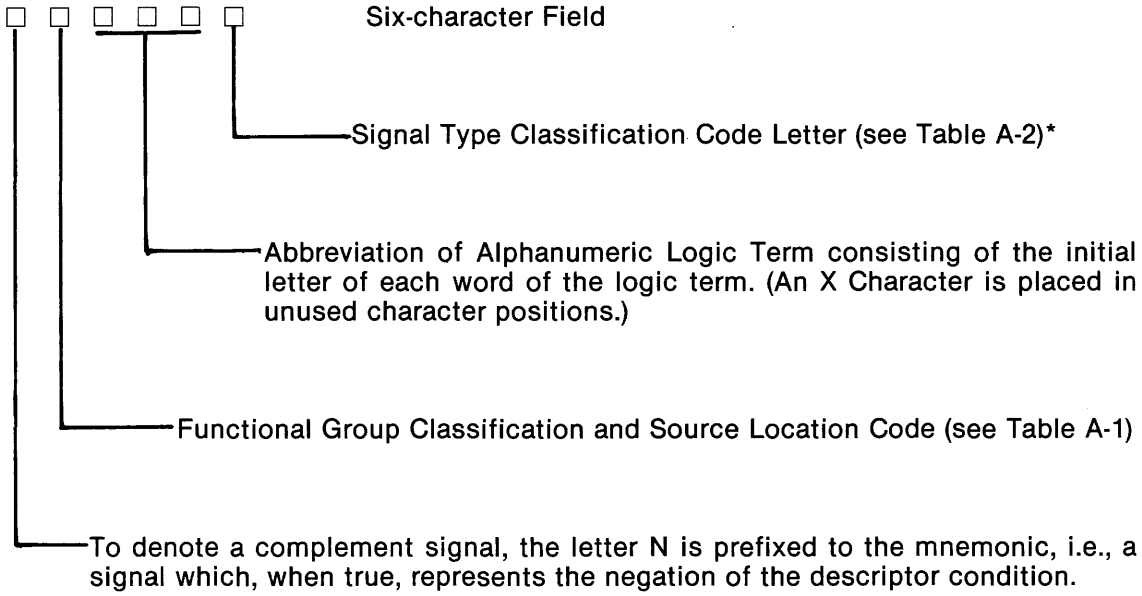


Figure 7-9. PCBA Interconnections

APPENDIX A — D3000 MNEMONICS

A D3000 mnemonic term consists of a six-character field and is defined in Figure A-1. Figure A-1 should be used in conjunction with Tables A-1 and A-2 for interpretation of the D3000 mnemonics scheme. The D3000 mnemonics are listed in Table A-3.



NOTE: The numeral zero (0) has no slash through it; the alphabet O has a slash through it and is presented as Ø.

Figure A-1. Mnemonic Construction

Table A-1
Functional Group Classification

Prefix Symbol	Definition
I	Interface
R	Read/Write PCBA
C	Components Group (Base Assy Components)
S	Servo PCBA
L	Logic PCBA

Table A-2
Signal Type Classification

Suffix Symbol	Definition
F	Flip-Flop Output
L	Latch Flip-Flop Output*
G	Gate Output, Active Pullup or Open Collector with Pullup to +5v; Includes Transistors
S	Switch or Relay Contact Generated Signals
A	Analog Signals and Returns, Shields and Similar Signals
1,2,3,etc.	Buffering Levels of 1 through 9
R	Receiver, Line Receiver Input
D	Driver, Line Driver Output
T	Translator, Open Collector Gate Output without Pullup, or Pullup to Other than +5v such as Special Logic Levels

*Used only if latch is mechanized by cross-couple gates.

Table A-3
D3000 Mnemonics

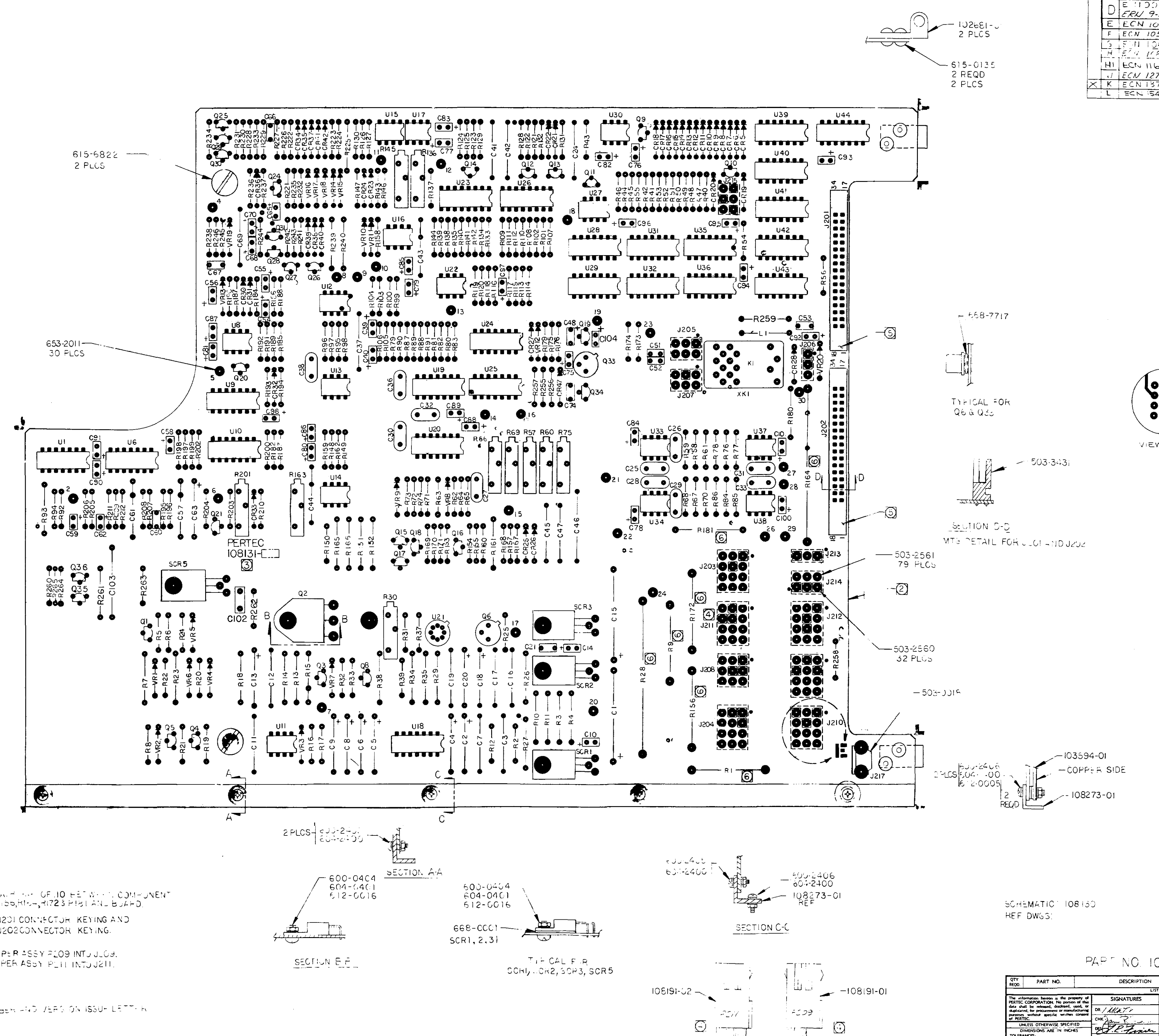
Mnemonic	Logic Term Name	Mnemonic	Logic Term Name
CCR1S	Cartridge (Switch) Return No. 1	IQPDD	Quad Platter Drive
CCS1S	Cartridge Switch No. 1	IRCXD	Read Clock
CCS2S	Cartridge Switch No. 2	IRDXD	Read Data
CCSIS	Cartridge Correctly Inserted	IREXR	Read Enable
CLMRA	Lower Magnetic (Sensor) Return	IRGXR	Read Gate
CLMSA	Lower Magnetic Sensor Signal	IRICR	Restore Initial Cylinder
CLPOS	Lower Protect (Switch) On	IRTRR	Restore Initial Cylinder
CLSRS	Lower (Protect) Switch Return	IRXXD	Ready
CLSSA	Lower Sensor Shield	ISC0D	Sector Count Bit 0
CRSRS	Run/Stop (Switch) Return	ISC1D	Sector Count Bit 1
CRSSS	Run/Stop Switch	ISC2D	Sector Count Bit 2
CSSRS	(Unit) Selector Switch Return	ISC3D	Sector Count Bit 3
CUESA	Upper Electronic Sensor Signal	ISC4D	Sector Count Bit 4
CUMSA	Upper Magnetic Sensor Signal	ISC5D	Sector Count Bit 5
CUPOS	Upper Protect (Switch) On	ISC6D	Sector Count Bit 6
CUS1S	Unit Selector (Switch) No. 1 Position	ISISD	Special Interface Signal
CUS2S	Unit Selector (Switch) No. 2 Position	ISIXD	Seek Incomplete
CUS3S	Unit Selector (Switch) No. 3 Position	ISMXD	Sector Mark
CUS4S	Unit Selector (Switch) No. 4 Position	ISPXD	Sector Pulse
CUSRA	Upper Sensor Return	ISRWD	Ready to Seek, Read, or Write
CUSRS	Upper (Protect) Switch Return	ISSDR	Start/Stop Disk Drive
CUSSA	Upper Sensor Shield	ISTRR	Strobe
CUSXS	Unit Selector (Switch) No. 1—4	ITA0R	Track Address Bit 1
IAAXD	Address Acknowledge	ITA1R	Track Address Bit 2
IAEUR	Activate Emergency Unload	ITA2R	Track Address Bit 4
IAIXD	Address Interlock	ITA3R	Track Address Bit 8
IAU1D	Attention Unit 1	ITA4R	Track Address Bit 16
IAU2D	Attention Unit 2	ITA5R	Track Address Bit 32
IAU3D	Attention Unit 3	ITA6R	Track Address Bit 64
IAU4D	Attention Unit 4	ITA7R	Track Address Bit 128
IBS1D	Busy Seeking No. 1	ITAER	Track Address Extension Bit 256
IBS2D	Busy Seeking No. 2	ITOMR	Track Offset Minus
IBS3D	Busy Seeking No. 3	ITOPP	Track Offset Plus
IBS4D	Busy Seeking No. 4	IUS1R	Unit Select 1
ICASR	Cylinder Address Strobe	IUS2R	Unit Select 2
ICD0R	Cylinder Demand (Address) Bit 0	IUS3R	Unit Select 3
ICD1R	Cylinder Demand (Address) Bit 1	IUS4R	Unit Select 4
ICD2R	Cylinder Demand (Address) Bit 2	IWCKD	Write Check
ICD3R	Cylinder Demand (Address) Bit 3	IWDSR	Write Data Signal
ICD4R	Cylinder Demand (Address) Bit 4	IWDXR	Write Data and Clock
ICD5R	Cylinder Demand (Address) Bit 5	IWEXR	Write Enable
ICD6R	Cylinder Demand (Address) Bit 6	IWGXR	Write Gate
ICD7R	Cylinder Demand (Address) Bit 7	IWPIR	Write Protect Input
ICDER	Cylinder Demand (Address) Extension	IWPSD	Write Protect Status
IDPDD	Dual Platter Drive	L1PSG	Platter Select No. 1
IDTDD	Double Track Drive	L2PSG	Platter Select No. 2
IEEXR	Erase Enable	L3PSG	Platter Select No. 3
IEGXR	Erase Gate	L0WPG	No. 0 (Platter) Write Protect
IEPLD	Extension Line (Status)	L1WPG	No. 1 (Platter) Write Protect
IESLR	Extension Select Line	L2WPG	No. 2 (Platter) Write Protect
IFPXR	File Protected	L3WPG	No. 3 (Platter) Write Protect
IFRXD	File Ready	LA13G	Address 1 or 3
IHDiD	High Density indication	LAD0G	Address Difference Bit 0
IHSXR	Head Select	LAD1G	Address Difference Bit 1
IICAD	Illegal Cylinder Address	LAD2G	Address Difference Bit 2
IIMXD	Index Mark	LAD3G	Address Difference Bit 3
IIPXD	Index Pulse	LAD4G	Address Difference Bit 4
ILAID	Logic Address Interlock	LAD5G	Address Difference Bit 5
IMDXD	Malfunction Detected	LAD6G	Address Difference Bit 6
IPLFF	Phase-Lock Flip-Flop	LAD7G	Address Difference Bit 7
IPSER	Platter Select Extension	LADEG	Address Difference Extension Bit
IPSMD	Pseudo Sector Mark	LADXG	Address Difference
IPSXR	Platter Select	LAEXG	Any Emergency

Table A-3
D3000 Mnemonics (continued)

Mnemonic	Logic Term Name	Mnemonic	Logic Term Name
LAPXG	Address Pulse	LLCMG	Lock Cartridge Mechanism
LATSG	Auto Start	LLDPG	Lower Detector Pulse
LAU1G	Attention Unit 1	LLDRA	LED Return
LAU2G	Attention Unit 2	LLHFF	Load Heads Flip-Flop
LAU3G	Attention Unit 3	LLMEG	Lower Multiplexer Enable
LAU4G	Attention Unit 4	LLNPG	Load • Not Purge
LAVCG	Address Valid Code	LLOL1	Logic One Level (No. 1)
LBCEG	Brake Cycle Enable	LLOL2	Logic One Level (No. 2)
LBCFF	Brake Cycle Enable Flip-Flop	LLOL3	Logic One Level (No. 3)
LBSXG	Busy Signal	LLOL4	Logic One Level (No. 4)
LBTFF	Busy Time Flip-Flop	LLOL5	Logic One Level (No. 5)
LCAE1	Cylinder Demand Address Extension	LLOL6	Logic One Level (No. 6)
LCA6I	Cylinder Demand Address Bit 6	LLOL7	Logic One Level (No. 7)
LCA7I	Cylinder Demand Address Bit 7	LLOL8	Logic One Level (No. 8)
LCAX1	Current Address Bits 6, 7, & E	LLOL9	Logic One Level (No. 9)
LC01F	Clock No. 01	LLOX1	Logic One (No. 1)
LC02F	Clock No. 02	LLOX2	Logic One (No. 2)
LC03F	Clock No. 03	LLOX3	Logic One (No. 3)
LC04F	Clock No. 04	LLOX4	Logic One (No. 4)
LC08F	Clock No. 08	LLOX5	Logic One (No. 5)
LC09F	Clock No. 09	LLOX6	Logic One (No. 6)
LC09G	Clock No. 09	LLOX7	Logic One (No. 7)
LC10F	Clock No. 10	LLPLT	Lower Protect Lamp (Drive)
LC13F	Clock No. 13	LLPNG	Load and Purge Not
LC17F	Clock No. 17	LLPOS	Lower Protect On (Switch)
LC20F	Clock No. 20	LLPSG	Lower Platter Select
LC21F	Clock No. 20	LLPXG	Load • Purge
LCCIG	Cartridge Correctly Inserted	LLSCK	Lower Sector Clock
LCOUG	Clear or Unload	LLSEG	Latched Seek Error
LDACG	Demand Address Clear	LODAS	Offset Disable
LDAMG	Demand Address Most (Significant) Bit	LNLPG	Not Load • Purge
LDAWG	Track Number 256	LNRSG	Not Run • Sequence Not
LDISG	Disable Index & Sector	LWOEG	Write or Erase
LDIDG	Disk Initial Delay	LP05A	Plus 05 Volts Power Indicator Voltage
LDMEG	Drive Motor Enable	LP5VA	Plus 5 Volts Signal
LDPSG	Dual Platter Signal	LP10VA	Plus 10 Volts Lamp Power
LDRCG	Delayed Ready Condition	LP12VA	Plus 12 Volts Signal
LDRXG	Disk Rotating	LPCFF	Purge Cycle Flip-Flop
LDSEG	Disk Speed Error	LPCXG	Power Clear
LDSFG	Disk Starting Fault	LPIRA	Power Indicator Return
LEBXG	End Busy	LPLEG	Position Limit Error
LECEG	Erase Current Enable	LPLFF	Phase Lock Flip-Flop
LEOFG	Emergency or Failure Condition	LPMXG	Position Mode
LERFF	End (of) Run Flip-Flop	LPSMF	Pseudo Sector Mark
LESCG	Electronic Sector Clock	LPSRS	Lower Protect Switch
LESDG	Enabled Selected Drive Detection	LRCSG	Removable Cartridge Select
LEUCG	Emergency Unload Command	LRECG	Read Enable Control
LEUEG	Emergency Unload Enable	LRERG	Reset End of Run
LEUFF	Emergency Unload Flip-Flop	LRFFF	Run Flip-Flop
LEXSG	Extension Status	LRLDT	Ready Lamp Driver
LFDX1	Forward Direction	LROFF	Restore Operation Flip-Flop
LFPML	File Protect Mode	LRPXG	Run Switch Pulse
LFSM1	Forward Slow Mode	LRSCG	Reset Counter
LHLEG	Head Loading Error	LRSM1	Reverse Slow Mode
LHRXG	Heads Retracted	LRSPG	Run Switch Pulse
LIAXG	Illegal Address	LRSSS	Run/Stop Switch
LIESG	Interrupt Enable Signal	LRXDT	Run (Lamp) Driver
LIMS1	Increase Motor Speed	LRXXG	Ready
LISMG	Index or Sector Mark	LSARG	Selected and Ready
LL1DA	LED No. 1 Drive	LSCEG	Sequency Control Enable
LL2DA	LED No. 2 Drive	LSCFF	Sequence Control Flip-Flop
LLAIG	Logical Address Interlock	LSCRG	Speed Count Reset
LLAXG	Load Address	LSDDG	Start Disk Drive

Table A-3
D3000 Mnemonics (continued)

Mnemonic	Logic Term Name	Mnemonic	Logic Term Name
LSDMD	Start Drive Motor		
LSDMG	Start Drive Motor		
LSLDT	Safe Lamp Driver		
LSNHG	Sequence • Not Heads Retracted		
LSOTF	Speed Out (of) Tolerance		
LSRNG	Select, Ready, No Write Fault		
LSSDG	Start/Stop Drive		
LSTEG	Seek Time Error		
LSTPF	Sequence Timing Pulse Flip-Flop		
LSXXG	Selected		
LTOMG	Track Offset Minus		
LTOPG	Track Offset Plus		
LTPCG	Temperature Compensation		
LTSCG	Transfer Speed Count		
LUDPG	Upper Detector Pulse		
LUHSG	Upper Head Select		
LUICK	Upper Index Clock		
LUMEG	Upper Multiplexer Enable		
LUPLG	Upper Protect Lamp		
LUPLT	Upper Protect Lamp Drive		
LUPOG	Upper Protect On (Switch)		
LUPSG	Upper Platter Select		
LUSCK	Upper Sector Clock		
LVCO	Voltage Control Oscillator		
LVREG	Velocity Reference Enable		
LVSCG	Voltage Sector Control		
LWCKG	Write Check		
LWDFT	Write Double Frequency		
LWMXG	Write Mode		
LWOEG	Write or Erase		
LWPDG	Write Protect Delay		
LWPTG	Write Protect		
RRCSG	Read Clock Signal		
RRDSG	Read Data Signal		
RRGCG	Reduce Gain Control		
RWECG	Write Emergency Condition		
S10SS	10 Volts Switched		
S12SS	Switched – 12 Volts		
SCLSG	Cartridge Lock Solenoids		
SFWDG	Forward Direction		
SHRXG	Heads Retracted		
SL11G	Logic One No. 1		
SL12G	Logic One No. 2		
SPCSA	Power Clear Signal		
SPCXG	Power Clear		
SPQCG	Position Quadrature Clock		
SPRCG	Position Reference Clock		
SPTFG	Position Transducer Failure		
SPTIG	Position Transducer Index		
SVRVA	Velocity Reference Velocity Mode		
T5RTT	+5-Volt Timer		
TDIDG	Disk Initial Delay		
TDISG	Disable Index and Sector		
TRHCG	Ready Hold Control		
TTPCG	Top Platter Compensation		
TTREG	Temperature Read Enable		



REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-WF PRE PROD. RELEASE	9/14/76			AKD
B	ERN 9522	2/1/77	RJ		
C	ECN 9821A [illegible]				
D	E [illegible] / ERN 9-77 PROD. RELEASE		RJ		
E	ECN 10484	8-22-77	DP		
F	ECN 10534				
G	ECN 1065[illegible]				
H	ECN 10[illegible]				
H1	ECN 11665				
J	ECN 12736				
K	ECN 13744				
L	ECN 15400	7/30/80	I.S.		

SCHEMATIC 108130
REF DWGS:

PART NO. 108131-01 REV. T

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
2. THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 108132-01 REV H AND SUBSEQUENT.
3. MARK VERSION NUMBER AND VERSION ISSUE LETTER IN AREA SHOWN.
4. INSTALL POWER JUMPER ASSY P209 INTO J209. INSTALL POWER JUMPER ASSY P211 INTO J211.
5. REMOVE PIN 34 FOR J201 CONNECTOR KEYING AND REMOVE PIN 24 FOR J202 CONNECTOR KEYING.
6. MA[illegible] UM [illegible] OF .10 BETWEEN COMPONENT BODY OF R1, R9, R28, R156, R164, R172 & R181 AND BOARD.

QTY REQD	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

The information hereon is the property of PERTEC CORPORATION. No portion of this data shall be released, disclosed, used, or duplicated, for procurement or manufacturing purposes without specific written consent of PERTEC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. [illegible]	
CHK. [illegible]	
DES. J.R. [illegible]	10/1/76
ENGR AK DESAI	10-1-76
PROJ. ENGR AK DESAI	10-1-76

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA, SERVO BOARD

NEXT ASSY	1ST USED ON
TOP ASSY	D3600 EXT

APPLICATION

FINISH:

MATL: SEE L/M

SIZE: E | CODE IDENT NO. | DWG NO. 108131 | REV L

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
100-1005	R22
100-1015	R42
100-1025	R1, 3, 5, 7, 15, 16, 19, 24, 25, 27, 29, 33, 37, 39, 40, 44, 49, 50, 60, 61, 64, 65, 68, 72, 75, 80
100-1045	R51
100-1515	R13, 18
100-1525	R23, 28
100-2205	R77
100-2225	R73
100-3315	R14
100-3915	R26
100-4705	R9, 10, 11, 12, 54, 55, 66, 67
100-4715	R34, 35, 38, 46, 47
100-4725	R2, 4, 6, 8, 74
100-5625	R41
100-6815	R52, 53
102-6805	R71
102-8205	R45, 76
104-1100	R17
104-4220	R20, 21
107-1212	R58
107-1961	R70
107-3831	R56, 57, 62, 63
107-5111	R81, 85
107-7501	R43
121-5020	R59, 69, 79, 82, 83, 86
131-1030	C4, 5
133-7060	C9
135-1002	C27, 29, 30 42
135-4731	C6
139-2244	C1, 2, 7, 8, 10, 11, 12, 14, 19, 20, 26, 28, 31, 32, 34, 35, 38 41
200-2219	Q7, 8
200-3053	Q15
200-4123	Q10, 13, 17, 20
200-4125	Q1 THRU 6, 9, 11, 14, 19
200-4490	Q12, 16
204-0074	Q18
300-4446	CR1 THRU 11
330-0565	VR4
330-0685	VR2, 3
330-1005	VR1

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
400-0592	U1
515-6805	L1, 2, 3, 8, 9
700-0116	U2
700-4010	U15, 16
700-4123	U9, 17
700-4741	U5, 18
700-7400	U10
700-7402	U13
700-7404	U6, 12
700-7416	U3, 8
700-8020	U7
710-7400	U4
710-7420	U11
710-7474	U14

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTER-ISTIC	C3						C15, 17	
		VALUE	PART NO.					VALUE	PART
-01	2200 BPI/ 1500 RPM	---	OMIT					.022	131-2
-02	2288 BPI/ 2400 RPM	---	OMIT					.015	131-1

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTER-ISTIC	L4, 5		L6, 7			
		VALUE	PART NO.	VALUE	PART NO.		
-01	2200 BPI/ 1500 RPM	43 UH	515-4305	24 UH	515-2405		
-02	2200 BPI/ 2400 RPM	27 UH	515-2705	15 UH	515-1505		

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
C42	C13	
CR11		
L9		
Q20		
R86		
TP13		
U18		
VR4		
W10		

TYPE	◆
NE592A	1
7416	1
7400	1
74S10	1
74S74	1
74LS00	1
7402	1
7404	1
74LS20	1
74LS74	1
8T20B	1
10116	1
74123	

(1) TABLE I

PART NO.	REFERENCE DESIGNATION
100-1005	R22
100-1015	R42
100-1025	R1, 3, 5, 7, 15, 16, 19, 24, 25, 27, 29, 33, 37, 39, 40, 44, 49, 50, 60, 61, 64, 65, 68, 72, 75, 80
100-1045	R51
100-1515	R13, 18
100-1525	R23, 28
100-2205	R77
100-2225	R73
100-3315	R14
100-3915	R26
100-4705	R9, 10, 11, 12, 54, 55, 66, 67
100-4715	R34, 35, 38, 46, 47
100-4725	R2, 4, 6, 8, 74
100-5625	R41
100-6815	R52, 53
102-6805	R71
102-8205	R45, 76
104-1100	R17
104-4220	R20, 21
107-1212	R58
107-1961	R70
107-3831	R56, 57, 62, 63
107-5111	R81, 85
107-7501	R43
121-5020	R59, 69, 79, 82, 83, 86
131-1030	C4, 5
133-7060	C9
135-1002	C27, 29, 30, 42
135-4731	C6
139-2244	C1, 2, 7, 8, 10, 11, 12, 14, 19, 20, 26, 28, 31, 32, 34, 35, 38 41
200-2219	Q7, 8
200-3053	Q15
200-4123	Q10, 13, 17, 20
200-4125	Q1 THRU 6, 9, 11, 14, 19
200-4930	Q12, 16
204-0074	Q18
300-4446	CR1 THRU 11
330-0565	VR4
330-0685	VR2, 3
330-1005	VR1

(1) TABLE I

PART NO.	REFERENCE DESIGNATION
400-0592	U1
515-6805	L1, 2, 3, 8, 9
700-0116	U2
700-4010	U15, 16
700-4123	U9, 17
700-4741	U5, 18
700-7400	U10
700-7402	U13
700-7404	U6, 12
700-7416	U3, 8
700-8320	U7
710-7400	U4
710-7420	U11
710-7474	U14

(2) TABLE II

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTERISTIC	C3						C15, 17		C16		C18		C21		C22, 23		C24, 25		C33		C36, 37		C39, 40	
		VALUE	PART NO.					VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	2200 BPI/ 1500 RPM	---	OMIT					.022	131-2230	68 PF	130-6805	39 PF	130-3905	39 PF	130-3905	.0022 100V	131-2220	68 PF	130-6805	22 PF	130-2205	150 PF	130-1515	33 PF	130-3305
-02	2288 BPI/ 2400 RPM	---	OMIT					.015	131-1530	39 PF	130-3905	15 PF	130-1505	22 PF	130-2205	.001 1KV	135-1002	47 PF	130-4705	15 PF	130-1505	68 PF	130-6805	22 PF	130-2205

(2) TABLE II (CONT'D)

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTERISTIC	L4, 5		L6, 7				R30		R31, 32		R36		R48		R78, 84		
		VALUE	PART NO.	VALUE	PART NO.			VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	
-01	2200 BPI/ 1500 RPM	43 UH	515-4305	24 UH	515-2405			1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	4.64K	107-4641	
-02	2200 BPI/ 2400 RPM	27 UH	515-2705	15 UH	515-1505			1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	5.62K	107-5621	

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
C42	C13	
CR11		
L9		
Q20		
R86		
TP13		
U18		
VR4		
W10		

(4) TABLE IV

VOLTAGE AND GROUND PIN NO.				
TYPE	+5V	GND	+6.8V	-6.8V
NE592A			3	10
7416	14	7		
7400	14	7		
74S10	14	7		
74S74	14	7		
74LS08	14	7		
7402	14	7		
7404	14	7		
74LS20	14	7		
74LS74	14	7		
8T20B	16	8		
10116	16	8		
74123				

(5) TABLE V

SPARE LOGIC ELEMENTS	
TYPE	REFERENCE DESIGNATION
7416	U8F, U8A
74S74	U18B
7400	U10A
74S74	U5A
7404	U12E
74LS20	U11A

(12) TABLE VI

CONFIGURATION
READ ALWAYS ENABLE
SYNCHRONOUS READ ENABLE
ASSYNCHRONOUS READ ENABLE
PULSE DATA, PULSE CLOCK
LEVEL CHANGE DATA, PULSE CLOCK
COMPOSITE DATA ONLY

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-DK 108 PROD RELEASE	9/8	DK	MB	RB
B	ECN 0503	3/27	RJ	RB	RB
	ERN 9-TR PROD REL.	6/7	CJ	-	-

(2) TABLE II

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTER-ISTIC	C3						C15, 17		C16		C18		C21		C22, 23		C24, 25		C33		C36, 37		C39, 40	
		VALUE	PART NO.					VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	2200 BPI/ 1500 RPM	---	OMIT					.022	131-2230	68 PF	130-6805	39 PF	130-3905	39 PF	130-3905	.0022 100V	131-2220	68 PF	130-6805	22 PF	130-2205	150 PF	130-1515	33 PF	130-3305
-02	2288 BPI/ 2400 RPM	---	OMIT					.015	131-1530	39 PF	130-3905	15 PF	130-1505	22 PF	130-2205	.001 1KV	135-1002	47 PF	130-4705	15 PF	130-1505	68 PF	130-6805	22 PF	130-2205

(2) TABLE II (CONT'D)

ASSEMBLY 108141 VERSION NO.	VERSION CHARACTER-ISTIC	L4, 5		L6, 7				R30		R31, 32		R36		R48		R78, 84		
		VALUE	PART NO.	VALUE	PART NO.			VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	
-01	2200 BPI/ 1500 RPM	43 UH	515-4305	24 UH	515-2405			1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	4.64K	107-4641	
-02	2200 BPI/ 2400 RPM	27 UH	515-2705	15 UH	515-1505			1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	5.62K	107-5621	

REFERENCE DESIGNATIONS	
NOT USED	DELETED
C13	

(4) TABLE IV

VOLTAGE AND GROUND PIN NO.				
TYPE	+5V	GND	+6.8V	-6.8V
NE592A			3	10
7416	14	7		
7400	14	7		
74S10	14	7		
74S74	14	7		
74LS00	14	7		
7402	14	7		
7404	14	7		
74LS20	14	7		
74LS74	14	7		
8T20B	16	8		
10116	16	8		
74123				

(5) TABLE V

SPARE LOGIC ELEMENTS	
TYPE	REFERENCE DESIGNATION
7416	U8F, U8A
74S74	U18B
7400	U10A
74S74	U5A
7404	U12E
74LS20	U11A

(12) TABLE VI

CONFIGURATION	JUMPERS
READ ALWAYS ENABLE	W7 + W9
SYNCHRONOUS READ ENABLE	W8 + W10
ASSYNCHRONOUS READ ENABLE	W9 + W10
PULSE DATA, PULSE CLOCK	W3 + W5
LEVEL CHANGE DATA, PULSE CLOCK	W3 + W6
COMPOSITE DATA ONLY	W4 + W5

(12) FOR JUMPER CONFIGURATIONS (REF J3(3)) REFER TO TABLE VI. FOR PROGRAMMING ARRAYS REFER TO 104134.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING WITH THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

10. DIODES ARE IN4448.

9. PNP TRANSISTORS ARE 2N4125.

8. NPN TRANSISTORS ARE 2N4123.

7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL 1% ARE 1/8W.

(5) FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

(4) FOR I.C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS. SEE TABLE IV.

3 (RESERVED)

(2) FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

(1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY DWG. NO. 108141

REFERENCE DRAWINGS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± ANGULAR ± 1/2°
XXX ±
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR.	1/14
CHK.	1/24
ENGR.	
PROJ. ENGR.	
MATL.	
FINISH.	

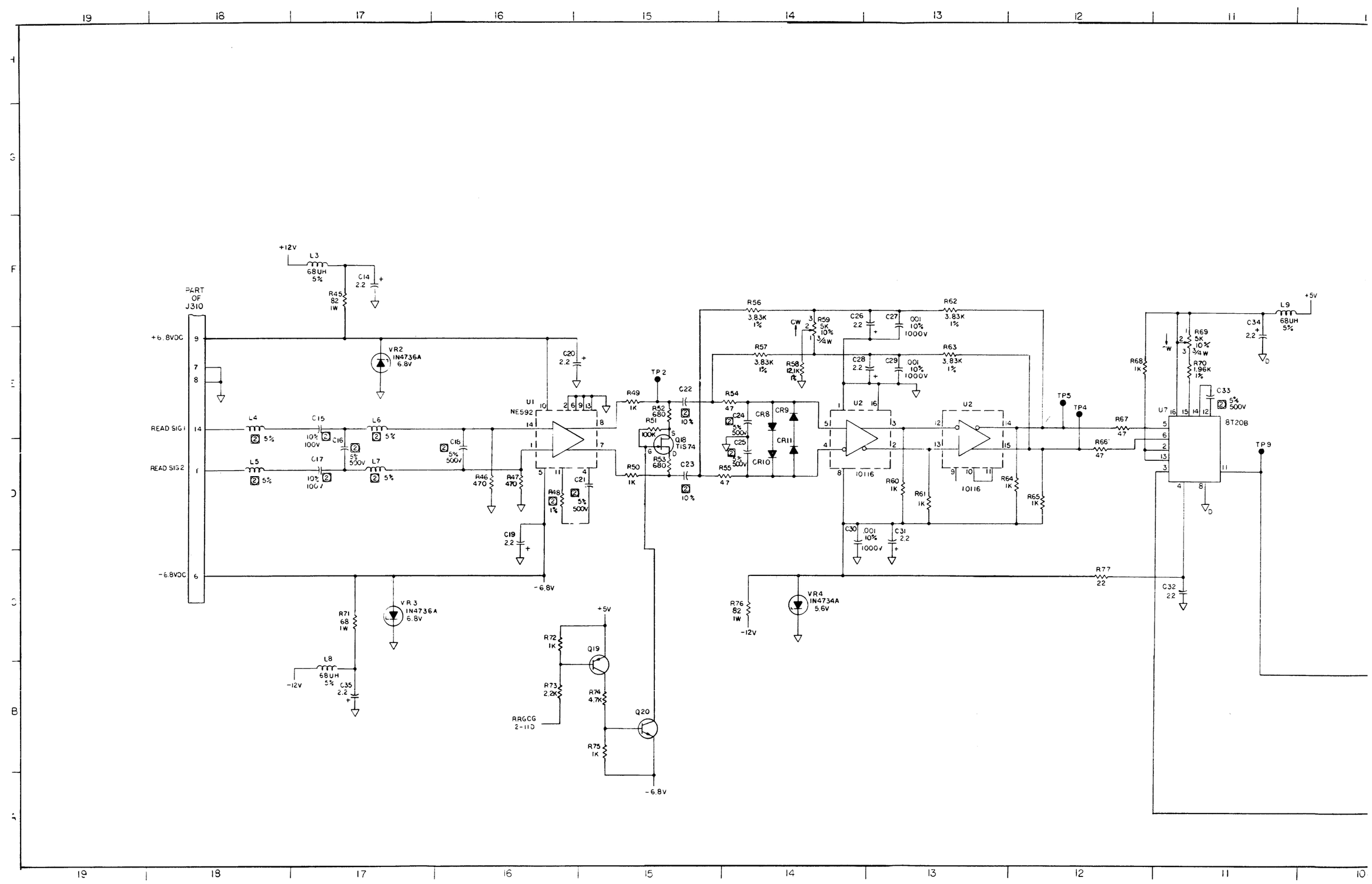
PERTEC PERIPHERAL EQUIPMENT DIVISION

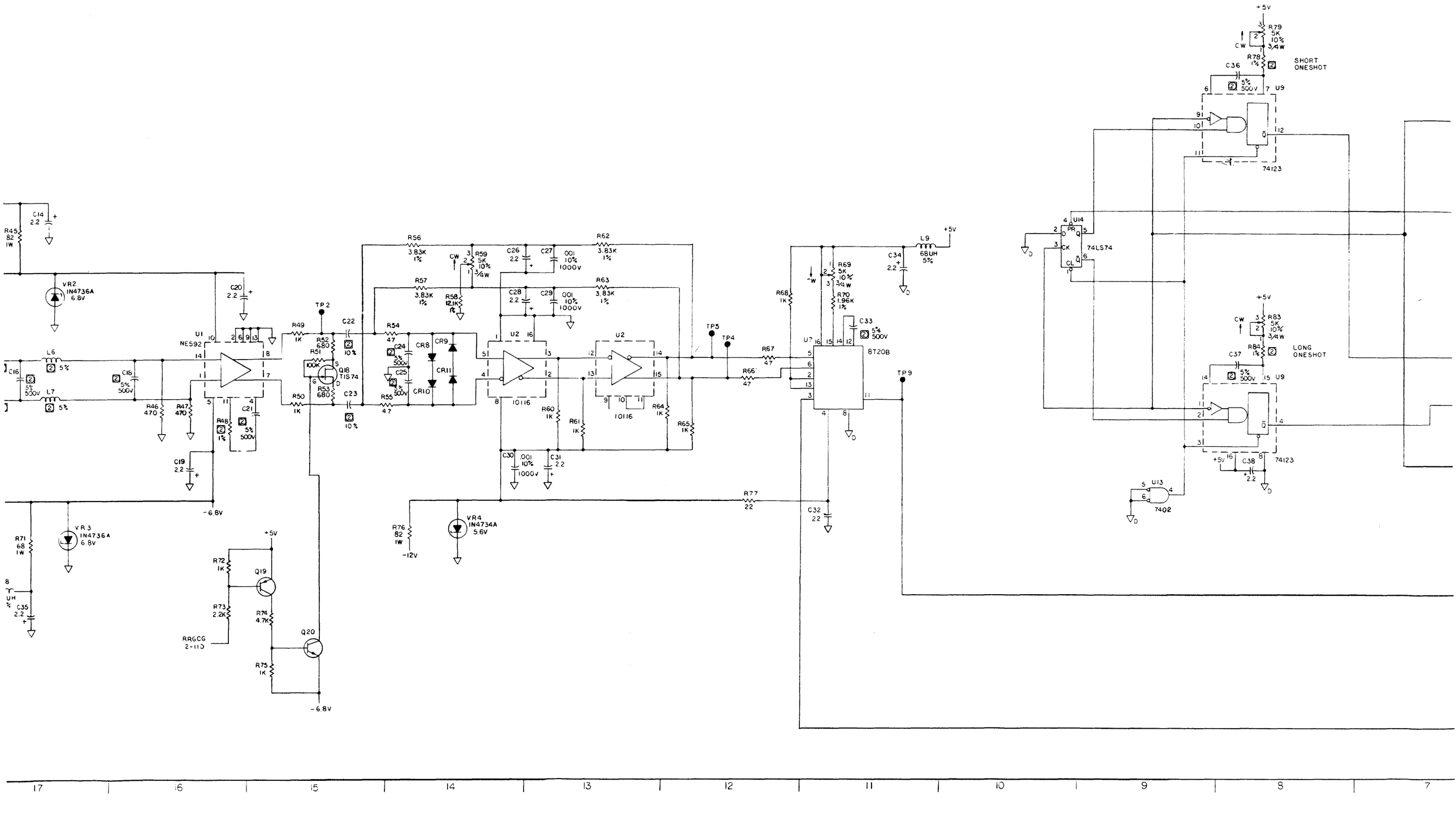
TITLE: SCHEMATIC READ/WRITE

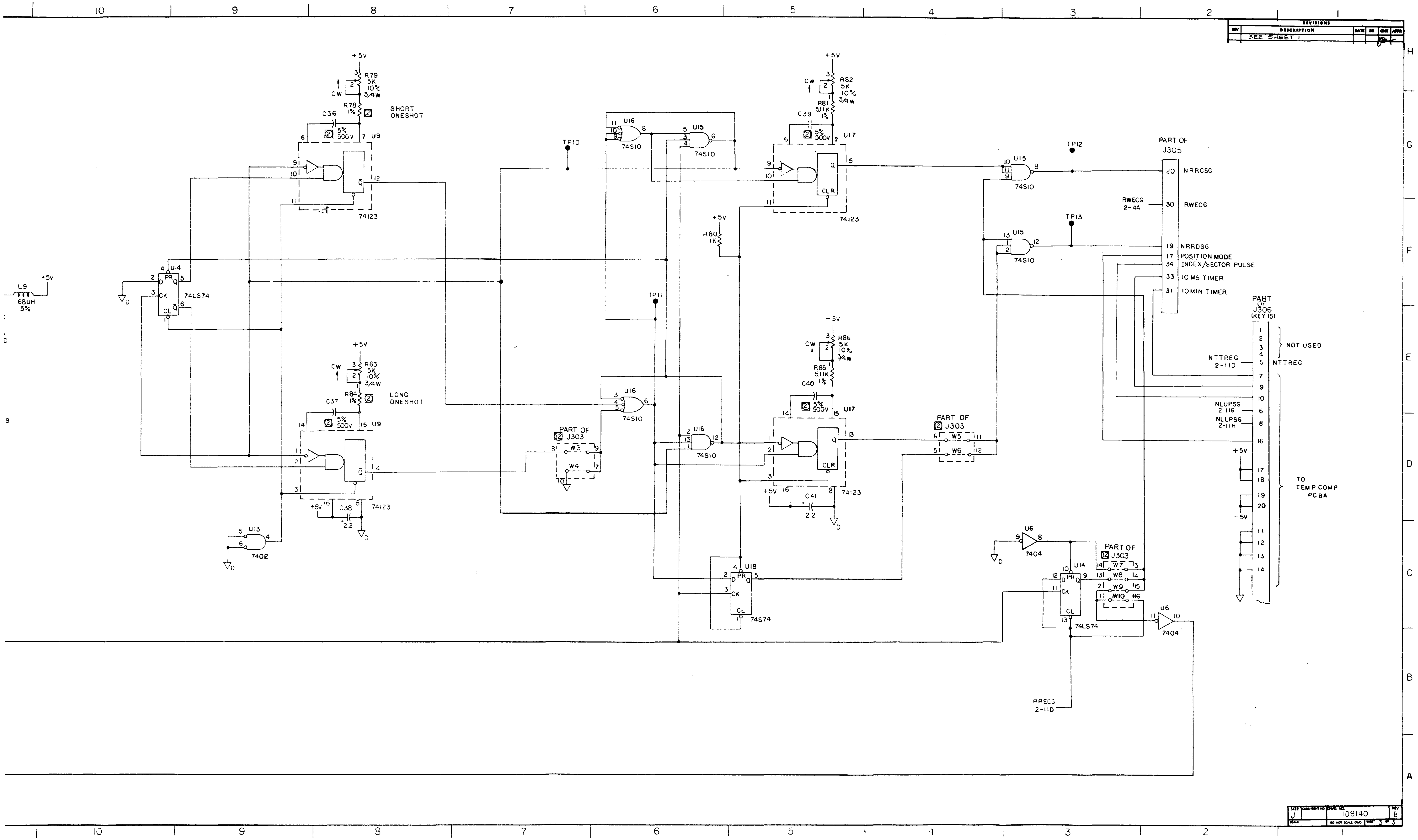
108141 NEXT ASSY	USED ON
APPLICATION	

SIZE J | CODE IDENT NO | DWG. NO. 108140 | REV B

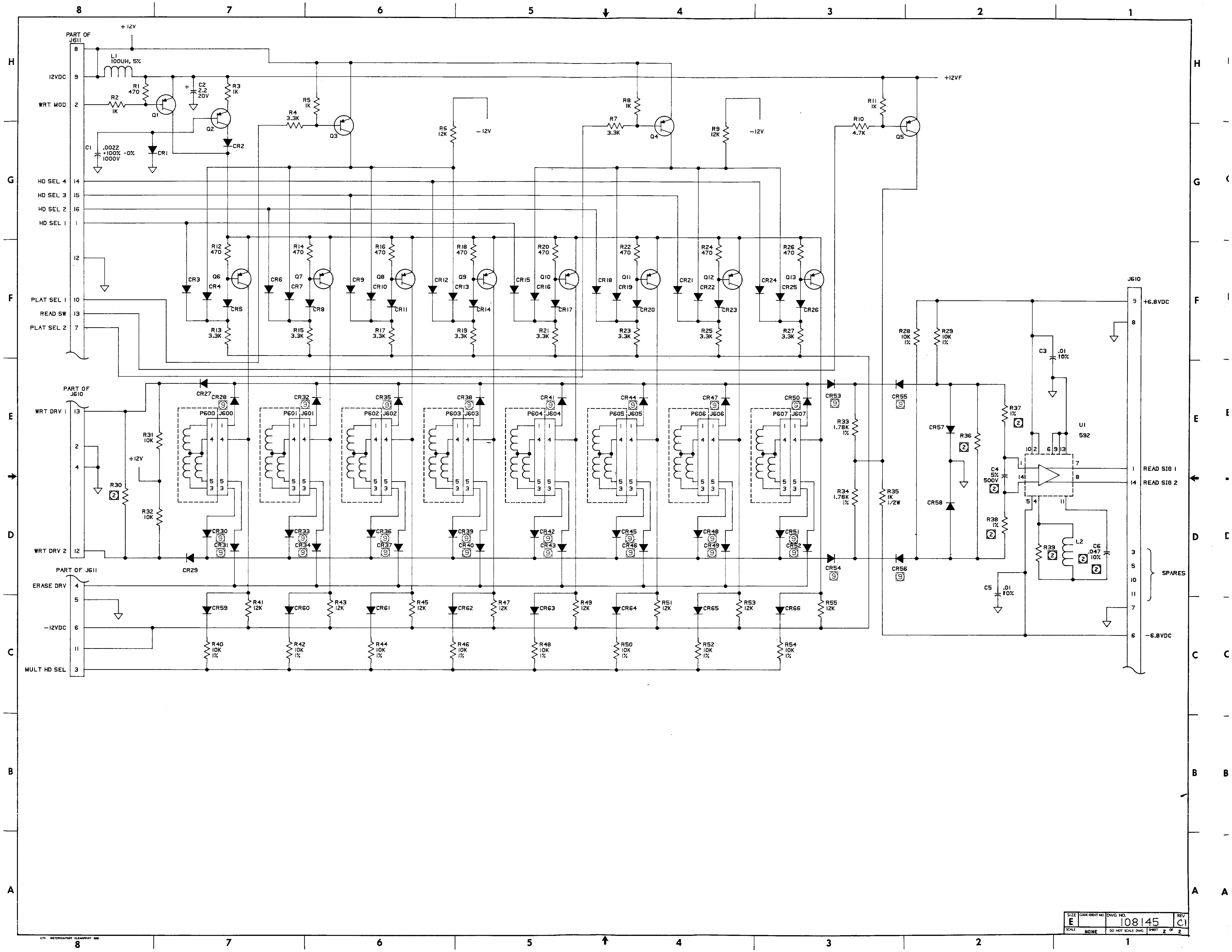
SCALE | DO NOT SCALE DWG. | SHEET 1 OF 5


+12V
L3
68UH
5%
C14
2.2
PART
OF
J310
+6.8VDC
R45
82
1W
VR2
IN4736A
6.8V
C20
2.2
U1
NE592
READ SIG 1
READ SIG 2
L4
L5
L6
L7
C15
C16
C17
C18
C19
2.2
C21
R46
470
R47
470
R48
1%
R49
1K
R50
1K
TP2
C22
R52
680
R51
100K
Q18
TIS74
R53
680
C23
R54
47
R55
47
C24
C25
CR8
CR9
CR10
CR11
R56
3.83K
1%
R57
3.83K
1%
R58
12.1K
1%
R59
5K
10%
3/4W
CW
R62
3.83K
1%
R63
3.83K
1%
C26
2.2
C27
001
10%
1000V
C28
2.2
C29
001
10%
1000V
U2
10116
R60
1K
R61
1K
R64
1K
R65
1K
C30
.001
10%
1000V
C31
2.2
TP5
TP4
R67
47
R66
47
+5V
L9
68UH
5%
C34
2.2
R68
1K
R69
5K
10%
3/4W
CW
R70
1.96K
1%
C33
5%
500V
U7
8T20B
TP9
R77
22
C32
22
-6.8VDC
-6.8V
VR3
IN4736A
6.8V
R71
68
1W
L8
68UH
5%
C35
2.2
-12V
+5V
R72
1K
Q19
R73
2.2K
R74
4.7K
RRGCG
2-11D
Q20
R75
1K
-6.8V
R76
82
1W
-12V
VR4
IN4734A
5.6V

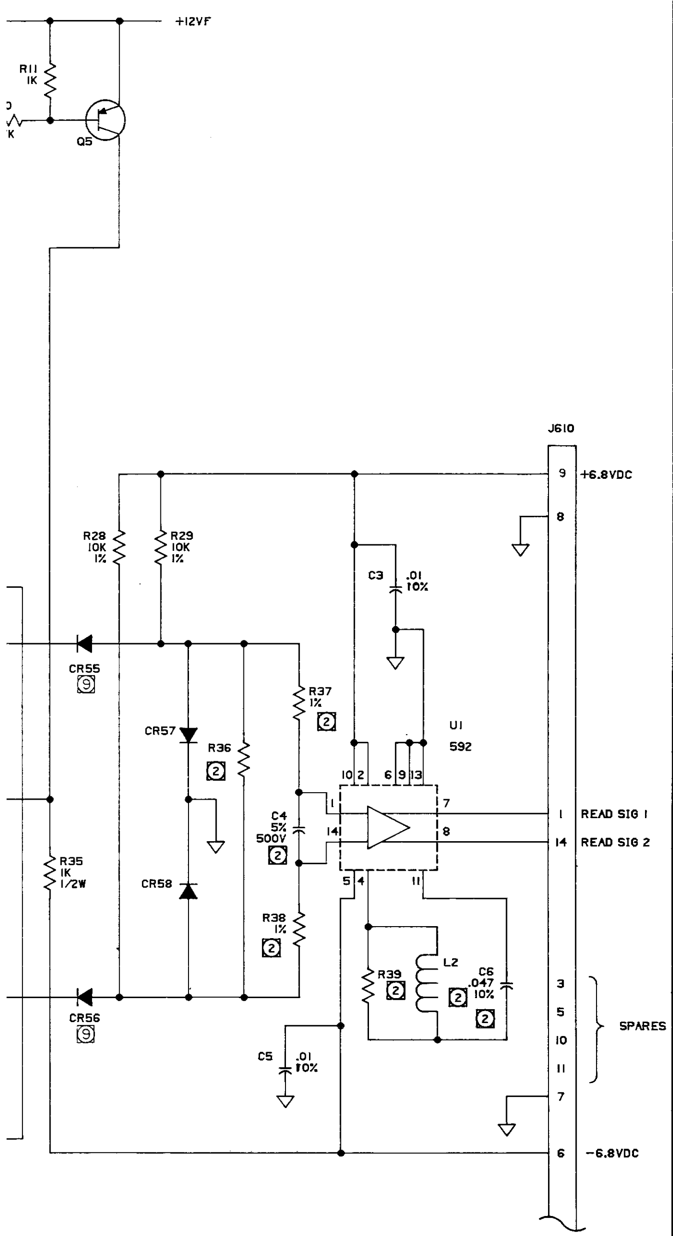

17
16
15
14
13
12
11
10
9
8
7
R45 82 1W
C14 2.2
VR2 IN4736A 6.8V
C20 2.2
L6 5%
L7 5%
C16 5% 500V
C18 5% 500V
R46 470
R47 470
C19 2.2
-6.8V
U1 NE592
R49 1K
TP2
C22 10%
R52 680
R51 100K
Q18 TIS74
R53 680
C23 10%
R50 1K
R48 1% 5% 500V
C21
R54 47
C24 5% 500V
C25 5% 500V
CR8
CR9
CR10
CR11
R55 47
R56 3.83K 1%
R57 3.83K 1%
R58 12.1K 1%
CW
R59 5K 10% 3/4W
C26 2.2
C27 001 10% 1000V
R62 3.83K 1%
C28 2.2
C29 001 10% 1000V
R63 3.83K 1%
U2
10116
R60 1K
R61 1K
R64 1K
R65 1K
C30 .001 10% 1000V
C31 2.2
TP5
TP4
R67 47
R66 47
R68 1K
R69 5K 10% 3/4W
R70 1.96K 1%
C33 5% 500V
U7 8T20B
L9 68UH 5%
C34 2.2
+5V
TP9
C32 22
R77 22
R76 82 1W
-12V
VR4 IN4734A 5.6V
VR3 IN4736A 6.8V
R71 68 1W
C35 2.2
R72 1K
Q19
R73 2.2K
R74 4.7K
Q20
R75 1K
RRGCG 2-110
U14 74LS74
SHORT ONESHOT
R79 5K 10% 3/4W
R78 1%
C36 5% 500V
U9 74123
LONG ONESHOT
R83 5K 10% 3/4W
R84 1%
C37 5% 500V
C38 2.2
U13 7402



SHORT ONESHOT
LONG ONESHOT
R79 5K 10% 3/4W
R78 1%
C36 5% 500V
R83 5K 10% 3/4W
R84 1%
C37 5% 500V
C38 2.2
U9 74123
U14 74LS74
L9 68UH 5%
U13 7402
TP10
TP11
TP12
TP13
U16 74S10
U15 74S10
R82 5K 10% 3/4W
R81 511K 1%
C39 5% 500V
U17 74123
R80 1K
R86 5K 10% 3/4W
R85 511K 1%
C40 5% 500V
C41 2.2
U18 74S74
PART OF J303
PART OF J305
20 NRRCSG
RWECG 2-4A
30 RWECG
19 NRRDSG
17 POSITION MODE
34 INDEX/SECTOR PULSE
33 10 MS TIMER
31 10 MIN TIMER
PART OF J306 (KEY 15)
NOT USED
NTTREG 2-11D
NTTREG
NLUPSG 2-11G
NLLPSG 2-11H
TO TEMP COMP PCBA
U6 7404
U14 74LS74
RRECG 2-11D
REVISIONS
REV DESCRIPTION DATE DR CHK APPR
SEE SHEET 1
SIZE J
DWG NO. 108140
REV E
SHEET 3 OF 3



PART OF J611
+12V
L1 100UH, 5%
12VDC
WRT MOD
R1 470
R2 1K
C2 2.2 20V
R3 1K
Q1
Q2
CR1
CR2
C1 .0022 +100% -0% 1000V
R4 3.3K
R5 1K
Q3
R6 12K
-12V
R7 3.3K
R8 1K
Q4
R9 12K
R10 4.7K
R11 1K
Q5
+12VF
HD SEL 4
HD SEL 3
HD SEL 2
HD SEL 1
PLAT SEL 1
READ SW
PLAT SEL 2
PART OF J610
WRT DRV 1
WRT DRV 2
R30
R31 10K
R32 10K
PART OF J611
ERASE DRV
-12VDC
MULT HD SEL
P600 J600
P601 J601
P602 J602
P603 J603
P604 J604
P605 J605
P606 J606
P607 J607
R33 1.78K 1%
R34 1.78K 1%
R35 1K 1/2W
R28 10K 1%
R29 10K 1%
C3 .01 10%
R36
R37 1%
R38 1%
C4 5% 500V
U1 592
R39
L2
C6 .047 10%
C5 .01 10%
J610
+6.8VDC
READ SIG 1
READ SIG 2
SPARES
-6.8VDC
SIZE E
DWG NO. 108145
REV C1
SCALE NONE
DO NOT SCALE DWG
SHEET 2 OF 2



SIZE	CODE IDENT NO.	DWG NO.	REV
E		108145	C1
SCALE NONE		DO NOT SCALE DWG	SHEET 2 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-3P PRE PROD RELEASE				
B	ECN 10107	5-21-77			
	ERN 9-TS PROD. RELEASE	5/31/77			
C	ECN 7419		SK		
C1	ECN 13153	6/6/79	MP		

TABLE I [1]

PART NO.	REFERENCE DESIGNATION
100-1025	R2, 3, 5, 8, 11
100-1035	R31, 32
100-1235	R6, 9, 41, 43, 45, 47, 49, 51, 53, 55
100-3325	R4, 7, 13, 15, 17, 19, 21, 23, 25, 27
100-4715	R1, 12, 14, 16, 18, 20, 22, 24, 26
100-4725	R10
101-1025	R35
107-1002	R28, 29, 40, 42, 44, 46, 48, 50, 52, 54
107-1781	R33, 34
135-1031	C3, 5
135-2272	C1
139-2244	C2
200-4402	Q1 THRU Q13
300-4446	CR1 THRU 27,29,57 THRU 66
300-0115	CR28,30 THRU 56
400-0592	U1
515-1015	L1

TABLE II [2]

VERSION NUMBER	VERSION CHARACTERISTIC	C4		C6	R30		R36	R37, 38		R39				L2			
		VALUE	PART NO.	135-4731	VALUE	PART NO.		VALUE	PART NO.	VALUE	PART NO.			VALUE	TOL	PART NO.	
-01	2200 BPI / 1500 RPM	22PF	130-2205	USE	1.0K	100-1025	OMIT	422	107-4220	68	100-6805			33UH	5 %	515-3305	
-02	2200 BPI / 2400 RPM	OMIT	OMIT	USE	1.0K	100-1025	OMIT	422	107-4220	68	100-6805			15UH	10 %	515-1500	
-03																	
-04																	

REFERENCE DESIGNATIONS

LAST USED	DELETED
C6	
CR66	
L2	
Q13	
R55	
U1	

[9] CR28,30 THRU 56 ARE PERTEC P/N 300-0115.

8. ALL DIODES ARE 1N4446.
7. (RESERVED)
6. ALL TRANSISTORS ARE 2N4402.
5. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 100V.
4. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL 1% RESISTORS ARE 1/8W.
3. (RESERVED)

[2] FOR VALUE, PART NO. AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II

[1] FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

PCBA NO: 108146

REFERENCE DWGS:

NOTES: UNLESS OTHERWISE SPECIFIED

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± X/X ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. R. SORG	12/10/76
CHK	
DES	
ENGR	12/21/76
PROJ. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE SCHEMATIC, R/W SELECT. MATRIX & PREAMP

108146	D36 EXT
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL:

SIZE	CODE IDENT NO.	DWG NO.	REV
E		108145	C1
SCALE NONE		DO NOT SCALE DWG	SHEET 1 OF 2

REV C1 DWG NO. 108145

APPENDIX B
FAULT-ISOLATION PROCEDURES

B1 GENERAL

Appendix B contains troubleshooting procedures which can be used as an aid in fault isolation. The required test equipment for use with these troubleshooting procedures is listed in Paragraph B2. The Troubleshooting Procedure chart appears in Paragraph B3 as Table B-2.

All references to paragraph numbers preceded by the letter B refer to paragraphs in this Appendix, as do references to figures and tables. All references to the manual refer to PCC PD Manual No. 108116, Models D3300 and D3400 Disk Drives. Table B-1 is a Trouble Location Guide listing specific problems and their location, by problem number, in the Troubleshooting Procedure chart.

Table B-1
Trouble Location Guide

Operational Problems	Table B-2 Reference
Emergency Unload NOTE: An emergency unload is one of the following: a. The positioner retracts during operation. b. Pressing the RUN/STOP pushbutton does not start the disk drive motor. c. The positioner does not load the heads.	Problems 13—22 which provide instructions for locating specific cause of trouble.
Specific Problems:	
1. SAFE lamp does not light.	Problem 1
2. Pressing RUN/STOP pushbutton does not start motor.	Problem 2
3. Emergency Unload relay, K1 on Servo PCBA, does not engage.	Problem 3
4. Spindle speed does not change to purge cycle during startup.	Problem 4
5. Heads do not load properly.	Problem 5
6. Disk Drive does not go into ready state.	Problem 6
7. READY lamp lights but positioner does not seek.	Problem 7
8. Heads unload when trying to write.	Problem 8
9. Disk Drive does not read data properly.	Problem 9
10. Disk drive has incorrect sector count.	Problem 10
11. Positioner seeks to wrong track location.	Problem 11
12. Heads crash.	Problem 12

B2 TEST EQUIPMENT REQUIRED

Test equipment required for testing and troubleshooting are:

(1) Oscilloscope, dual trace, with at least 100 MHz bandwidth and a horizontal module with a Delayed Sweep mode.

Minimum sweep rate: ≤50 ns/division.

Vertical and horizontal sensitivity: ± 3 percent accuracy.

(2) Three calibrated X10 test probes with ground clips.

(3) One X1 test probe with ground clip.

(4) Digital Multimeter, Fluke Model 8030A-01 (± 0.1 percent specified accuracy) or equivalent, with test leads.

(5) PCC PD Hand-Held Disk Exerciser, Model TE-D02.

(6) PCC PD Emergency Unload Status Monitor, Part No. 895490-01.

B3 TROUBLESHOOTING PROCEDURE CHART

Table B-2, Troubleshooting Procedure Chart, lists common problems, probable causes, and recommended repairs.

B4 POWER SUPPLY FAULT-ISLOATION PROCEDURE

This section will aid the technician in pinpointing power supply faults down to the specific component.

(1) Check fuses F1, F2, F3, and F4. Refer to Power Supply assembly drawing 108151 for fuse locations.

(2) Refer to Servo PCBA drawing number 108130 for test point locations. Use an oscilloscope or digital multimeter to check voltages as follows.

Test Point	Voltage
TP24	+ 5v dc ± 0.25v dc
TP7	– 5v dc ± 0.25v dc
TP20	+ 10v dc ± 0.8v dc
TP17	– 10v dc ± 0.8v dc

(3) If voltage at TP24 is incorrect, adjust variable resistor R30.

(4) If any voltage cannot be correctly adjusted, check the input voltages at J212, as follows.

J212-8	+ 10v dc	– 0.5 + 5v dc
J212-11	+ 25v dc	– 3.0 + 5v dc
J212-3	– 25v dc	– 5.0 + 3v dc

(5) If any voltage specified in Step (4) is not present, replace the power supply; otherwise, go to Step (6).

(6) If one of the voltages is not correct, disconnect all boards that are powered from the Servo PCBA. If voltages are correct after the boards are disconnected, begin reconnecting boards one at a time until an incorrect voltage is measured. Replace the board that caused the incorrect voltage to appear.

(7) If voltage at any test point is incorrect after the preceding tests, refer to Figure B-1 and continue troubleshooting procedure.

- If voltage at TP20 is incorrect, check Q1 on the heatsink. If Q1 is defective, replace it. If Q1 checks good, replace the Servo PCBA.
- If voltage at TP17 is incorrect, check Q2. If Q2 is defective, replace it. If Q2 checks good, replace the Servo PCBA.
- If voltage at TP24 is incorrect, check Q3. If the transistor is defective, replace it. If the transistor checks good, replace the Servo PCBA.
- If voltage at TP7 is incorrect, replace the Servo PCBA.

B5 READ/WRITE TROUBLESHOOTING GUIDE

Read/Write errors are indicated by a computer printout (or other output indication) specifying this type of error. Use the PCC PD Model TE-D02 Disk Exerciser to locate the Read/Write error source. Insert the exerciser plug into J102 (Logic PCBA); refer to the PCC PD Model TE-D02 Disk Exerciser manual (PCC PD Part No. 895321) for exerciser switch settings and test instructions. (If an exerciser is not available, use the computer to provide the required test signals.)

Read/Write problems in the disk drive normally originate from three sources. These are the heads, the disk, or the Read/Write PCBA. Refer to Paragraph 6.12 in the manual, Read Decode Circuit Adjustments. If the Read/Write problem is an error occurring on one track location on the same disk surface, the disk surface is defective. Replace the disk. If adjustments cannot be made properly, replace the Read/Write PCBA.

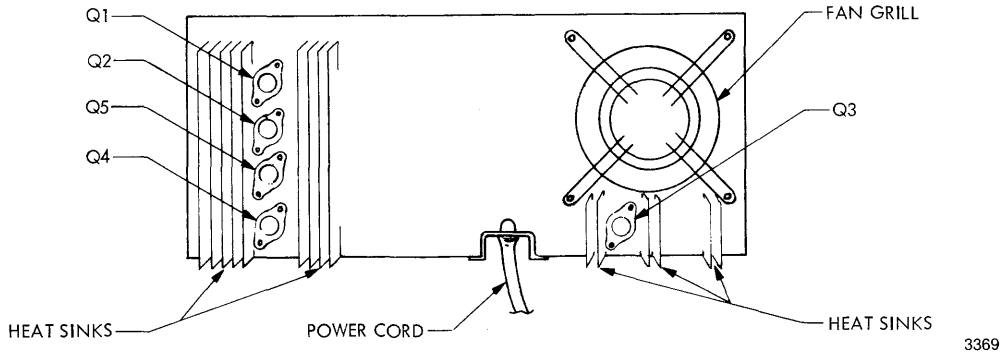


Figure B-1. Rear View of Disk Drive

Table B-2
Troubleshooting Procedure Chart

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
1. SAFE lamp does not light.	1. Defective lamp.	1. Replace lamp.
	2. Positioner has moved out, away from fully retracted position.	2. Push positioner back to fully retracted position.
	3. Power supply voltages not within tolerances.	3. Refer to Power Supply Fault Isolation Procedure, Paragraph B4.
	4. Disk rotation detector counter circuitry (on Logic PCBA) continues to indicate rotation after disk has stopped.	4. Check U283-15 on Logic PCBA. If U283-15 is low when the disk has stopped rotating, and U284-2 is also low, replace the Logic PCBA. If U283-15 is low and U284-2 is high, refer to Recommended Repair column, Problem 21.
	5. Brake cycle enable flip-flop U384-15 on Logic PCBA does not go high; therefore, the brake cycle enable circuit is not enabling the safe mode.	5. If U384-15 is low when U384-3 is high, replace Logic PCBA.
2. Pressing RUN/STOP pushbutton does not start motor.	1. Cartridge interlock switch is defective or other problem exists in interlock system.	1. Check cartridge interlock switch; check cartridge interlock system. Refer to Paragraph 6.15 in manual, Cartridge Interlock System —Front Load models; or Paragraph 6.16 for Top Load. Check logic level at J109-2 (Logic PCBA). If low, replace Logic PCBA. If high, replace the RUN/STOP pushbutton.
	2. Emergency unload abort.	2. Check logic level at U306-8 on Logic PCBA. If high, see Recommended Repair column, Problem 14. A low at U306-8 indicates an absence of the emergency unload condition.
	3. RUN/STOP pushbutton does not set U364-15 high.	3. Check logic level at U447-13 while pressing RUN/STOP pushbutton. If U447-13 stays high, replace RUN/STOP pushbutton. Replace the Logic PCBA if the following conditions occur simultaneously: a. U447-13 is low (Logic PCBA). b. U364-15 stays low (Logic PCBA). c. An emergency unload is not present. d. The SAFE lamp is lit.

Table B-2

Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
3. Emergency unload relay, K1, on Servo PCBA, does not engage.	1. Emergency unload condition being activated prevents K1 relay (Servo PCBA) from engaging during purge cycle.	1. Refer to Recommended Repair column, Problem 14.
	2. Defective relay or defective relay engage circuit.	2. Replace relay K1 (Servo PCBA). If still not engaging, check logic level at J202-32. If low, relay driver circuit is defective; replace the Servo PCBA. If J202-32 is high and does not go low when going into purge cycle, replace the Logic PCBA.
	3. – 20v dc at J212-3 (Servo PCBA) out of tolerance.	3. Refer to Power Supply Fault Isolation Procedure, Paragraph B4.
4. Spindle speed does not change to purge cycle during startup.	1. Lower magnetic transducer misaligned.	1. Refer to Paragraph 6.18.2 in manual for alignment instructions for Front Load and Top Load models. NOTE: Purge cycle refers to a 10% increase in spindle speed within 25 seconds after startup. To see if disk drive goes into purge cycle, check the waveform at TP3 (Logic PCBA) with oscilloscope. 1500 rpm = 40 msec between pulses Purge cycle = 36 msec between pulses 2400 rpm = 25 msec between pulses Purge cycle = 22.5 msec between pulses. (Spindle speed returns to normal after heads are loaded and before READY lamp lights.)
	2. Lower magnetic transducer output out of tolerance.	2. Check magnetic transducer voltage waveform on oscilloscope at U408-2 (Logic PCBA). Positive swing must be + 600 mv or more positive. Negative swing must be – 400 mv or more negative. If the output is out of tolerance (output too low), replace magnetic transducer assembly.
	3. Purge cycle flip-flop U344-15 on Logic PCBA stays low beyond 25 seconds.	3. If run flip-flop U364-15 (Logic PCBA) goes high and U344-15 stays low for more than 25 seconds, replace the Logic PCBA.
5. Heads do not load properly.	1. Positioner shipping restraint is not removed.	1. Remove shipping restraint.
	2. Positioner is not adjusted correctly.	2. Adjust positioner. Refer to Paragraph 6.8 in manual, Static Positioner Adjustments.
	3. Emergency unload.	3. Refer to Recommended Repair column, Problem 3.

Table B-2
Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
6. Disk drive READY lamp does not light.	1. Defective READY lamp.	1. Replace READY lamp.
	2. Defective ready circuit on Logic PCBA.	2. Replace Logic PCBA.
7. READY lamp lights but positioner does not seek.	1. Disk drive thumbwheel Unit Select Switch is not set on proper unit number.	1. Rotate Unit Select Switch to proper setting. Setting number must match computer select interface line number. (If the TE-D02 Exerciser is used, unit 1 is automatically selected.)
	2. Disk drive is not selected although Unit Select Switch is set to the correct number.	2. If the Unit Select Switch is set correctly and U49-8 is low (Logic PCBA), replace Unit Select Switch. If problem remains, replace Logic PCBA.
	3. Busy logic circuit (Logic PCBA) does not go into non-busy state.	3. Check logic level at U126-8 (Logic PCBA). If low, the drive is constantly busy. Therefore, the exerciser is not allowed to send new track information to the drive. This causes the positioner to stop seeking. Replace the Logic PCBA.
8. Heads unload when trying to write.	1. Write emergency condition when going into Write mode.	1. Replace the head that is selected when drive unloads. Refer to Paragraph 6.22 in manual for head replacement instructions. If problem persists, replace the Read/Write PCBA.
9. Drive does not read data properly.	1. If Exerciser Model TE-D02 is used, exerciser switches set to wrong values.	1. Set exerciser switches to 1500 rpm and 2200 bpi, or to 2400 rpm and 2200 bpi.
	2. Read/Write PCBA misaligned.	2. Refer to Paragraph 6.12 in manual, Read Decode Adjustments.
	3. Defective circuit on Read/Write PCBA.	3. Replace Read/Write PCBA.
	4. Incorrect index and sectoring.	4. Check for index indication and correct number of sectors. Set exerciser switch to select upper disk. On Logic PCBA, check index indication at TP7. Correct 1500 rpm indication is one pulse per 40 msec, correct 2400 rpm indication is * pulses per 25 msec. Check sector count at TP8. Correct 1500 rpm sector count is * pulses per 40 msec, correct 2400 rpm sector count is * pulses per 25 msec. If the wrong number of sectors is observed, check output waveform of upper photoelectric transducer for possible out-of-tolerance output. Positive swing shall be + 1.5v or more positive. Negative swing shall be – 1.0v or more negative. If output is out of tolerance, replace transducer. If output is within tolerance but trouble persists, replace Logic PCBA.

*Number of pulses is the same as the sector count for the unit used.

Table B-2
Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
9. Drive does not read data properly. (Continued)		Set exerciser switch to select lower disk. Check index indication at TP7. Correct 1500 rpm indication is one pulse per 40 msec, correct 2400 rpm indication is one pulse per 25 msec. Check sector count at TP8. Correct 1500 rpm sector count is * pulses per 40 msec, correct 2400 rpm sector count is * pulses per 25 msec. If the wrong number of sectors is observed, check phase lock loop as instructed in Paragraph 6.11 in manual. If the phase lock loop cannot be adjusted, check the lower magnetic transducer output voltage waveform on oscilloscope. Positive swing must be +600 mv or more positive. Negative swing must be −400 mv or more negative. If output is out of tolerance, replace magnetic transducer assembly. If output is within tolerance but trouble persists, replace Logic PCBA.
	5. Defective Read channel.	5. Refer to Paragraph B5 — Read/Write Troubleshooting Guide.
10. Disk drive has incorrect sector count. Correct sector count is indicated by waveform at TP8 on Logic PCBA as follows: 1500 rpm = *pulses per 40 msec 2400 rpm = *pulses per 25 msec	1. Front Load Models — Upper photoelectric transducer has incorrect output.	1. Check upper photoelectric transducer output waveform at U429-6 on Logic PCBA. Positive swing shall be +1.5v or more positive. Negative swing shall be −1.0v or more negative. If output is out of tolerance, replace transducer. If output is within tolerance, replace Logic PCBA.
	Top Load Models — Upper magnetic transducer has incorrect output.	Check upper magnetic transducer output at U429-6. Positive swing shall be +1.5v or more positive. Negative swing shall be −1.0v or more negative. If output is out of tolerance, replace magnetic assembly.
	2. Sector electronics on Logic PCBA has malfunction.	2. Replace the Logic PCBA.
	3. Disk cartridge has defective sector ring.	3. If sector ring has scratches on outer edges, replace the disk cartridge.
	4. Lower magnetic transducer output out of tolerance.	4. Check the magnetic transducer voltage waveform on oscilloscope at U408-2. The positive swing must be +600 mv or more positive. Negative swing must be −400 mv or more negative. If the output is out of tolerance, replace magnetic transducer assembly.
	5. Defective sector phase lock loop (Logic PCBA).	5. Adjust phase lock loop as instructed in Paragraph 6.11 in manual. If the adjustment cannot be made, replace the Logic PCBA.

*Number of pulses is the same as the sector count for the unit used.

Table B-2
Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
11. Positioner seeks to wrong track location.	1. Positioner improperly adjusted on Servo PCBA.	1. Refer to Paragraph 6.7 in manual, Positioner Servo Calibration.
	2. Address logic on Logic PCBA does not count track location correctly.	2. Replace Logic PCBA.
12. Heads crash.	1. Dirty heads and/or dirty disk surfaces.	1. Clean heads and disk surfaces. Refer to Paragraph 6.4.1 in manual, Cleaning the Heads, and Paragraph 6.4.2, Cleaning the Fixed Disk. If heads cannot be cleaned, replace heads. If disk surfaces cannot be cleaned, replace disk.
13. Emergency unload caused by speed out-of-tolerance error.	1. Defective RUN/STOP push-button.	1. If logic level at U447-13 (Logic PCBA) is high, replace RUN/STOP pushbutton.
	2. Defective Logic PCBA.	2. If logic level at U447-13 is low, and logic level at U385-11 is low, replace Logic PCBA. If logic level at U447-13 is low, and U385-11 is high, and TP22 (Logic PCBA) is also high, replace Logic PCBA.
	3. Defective Servo PCBA.	3. If U447-13 is low, U385-11 is high, TP22 is low, and TP2 (Servo PCBA) is low, replace Servo PCBA.
	4. Defective Drive Motor and/or Motor Control PCBA.	4. If U447-13 is low, U385-11 is high, TP22 is low, and TP2 is high, and the drive belt is not binding, replace Motor Control PCBA. If problem persists, replace Drive Motor. If the drive belt binds, readjust it (refer to Paragraph 6.19 in manual).
14. Emergency unload caused by head loading error.	1. Plug P205 on Servo PCBA.	1. Check if P205 is properly connected to J205.
	2. Defective flex strip on positioner.	2. Replace flex strip.
	3. Defective Logic PCBA.	3. Press RUN/STOP pushbutton. If logic level at U364-15 on Logic PCBA is low, replace Logic PCBA. If logic level at U364-15 does not go high within 25 seconds after pressing RUN/STOP push-button, replace Logic PCBA.
	4. Positioner binding.	4. Free the binding positioner.

Table B-2
Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
15. Emergency unload caused by disk speed error (after drive is in Ready mode).	1. AC motor speed out of tolerance.	1. Adjust ac motor speed control (refer to Paragraph 6.6.3.3 in manual).
	2. Defective Logic PCBA.	2. Check transducer output at U408-2 on Logic PCBA. If output is +600 mv or more, or −400 mv or more negative, and pulse train is not present at TP22 (Logic PCBA), replace Logic PCBA.
	3. Defective Motor Control PCBA and/or Drive motor.	3. If pulse train is present on TP22, check pulse train at TP2 (Servo PCBA). This should be 100 Hz for 50 Hz units and 120 Hz for 60 Hz units. If observed pulses are correct, replace Motor Control PCBA. If trouble persists, replace Drive Motor.
	4. Defective Servo PCBA.	4. If observed pulses are not as stated above, replace Servo PCBA.
	5. Lower magnetic transducer gap out of tolerance.	5. If voltage at U408-2 is within tolerance, check that lower magnetic transducer gap is within tolerance (refer to Paragraph 6.18.2). If needed, set gap within tolerance according to Paragraph 6.18.2. If gap cannot be set properly, replace lower magnetic transducer.
	6. AC voltage output of magnetic pickup out of tolerance.	6. Check if speed control adjustment is within tolerance (refer to Paragraph 6.6.3 in manual). Readjust speed control (R201) on Servo PCBA according to Paragraph 6.6.3.3 if necessary.
	7. Defective Logic PCBA.	7. If speed control is within tolerance and the problem persists, replace Logic PCBA.
	8. Defective lower magnetic transducer.	8. Check if lower transducer gap is within tolerance (refer to Paragraph 6.18.2 in manual). If transducer gap cannot be set properly, replace lower magnetic transducer.
16. Emergency unload caused by Position Transducer Lamp failure.	1. Defective Logic PCBA.	1. Check logic level at U327-2. If low, replace Logic PCBA.
	2. Defective Servo PCBA.	2. Check Position Transducer Lamp. If lamp is lit, replace Servo PCBA.
	3. Defective Position Transducer Lamp and/or defective Power Supply.	3. If Position Transducer Lamp is not lit, check voltage on J203-10. If voltage is within +11.5v and −9.3v, replace transducer lamp. If voltage on J203-10 is not within tolerance, refer to the Recommended Repair column, Problem 3.

Table B-2
Troubleshooting Procedure Chart (Continued)

PROBLEM	PROBABLE CAUSE	RECOMMENDED REPAIR
17. Disk tries to write through two heads simultaneously.	1. Defective Read/Write PCBA or defective heads.	1. If a low logic level exists at U306-12, check heads for shorts or opens. If heads are good, replace the Read/Write PCBA.
18. Write or erase current is on but not enabled.	1. Defective Read/Write PCBA or defective heads.	1. Check heads for shorts or opens. If heads are good, replace the Read/Write PCBA.
19. To determine if an emergency unload is internal or external to the disk.	1. Computer/compiler, external to disk, defective.	1. Check logic level at U50-13 (Logic PCBA). If U50-13 is low, trouble is in the external device.
	2. Defective Logic PCBA.	2. If U50-13 remains high while U306-3 (Logic PCBA) is low, replace the Logic PCBA.
20. Positioner takes longer than 200 msec to complete a seek to a new track location (Seek Time Error).	1. Foreign matter on voice coil and/or scale.	1. Remove foreign matter from voice coil and/or scale.
	2. Defective bearing on Positioner Assembly or defective Logic PCBA.	2. Check for any obstruction that would prevent free movement of carriage. If problem persists, replace Logic PCBA.
21. Loss of power (power clear emergency unload).	1. + 5v dc and ± 20v dc out of tolerance.	1. If U286-8 (Logic PCBA) is high, determine whether the + 5v and ± 20v dc are within tolerance (refer to Paragraph 6.6.2 in manual). If voltages are out of tolerance, refer to Recommended Repair column, Problem 3. If voltages are within tolerance, the Power Clear circuit is malfunctioning. Replace the Servo PCBA.
22. Emergency unload caused by Position Limit error.	1. Misadjusted index balance, defective Servo PCBA, or defective Transducer Assembly.	1. Check that a low level exists on TP3 from tracks 0—406. Adjust Index balance according to Paragraph 6.8.5. If Index balance cannot be achieved, replace Servo PCBA. If Index cannot be adjusted, replace Position Transducer Assembly.
	2. Defective Positioner Scale.	2. If a high level exists on TP27 from tracks 0—406, check to see if scale is scratched. Replace scale according to Paragraph 6.7 in manual.
	3. Defective Q4/Q5.	3. Connect jumper from Grd to U423-3 on Logic PCBA (this locks positioner into Position Mode). If positioner does not lock, check Q4 and Q5 on the heat sink. If either Q4 or Q5 is defective, replace it. If Q4 and Q5 check good, replace the Servo PCBA.

14 | 13 | 12 | 11 | 10 | 9

H

G

F

E

D

C

B

A

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
100-0895	R176
100-1005	R173, 174, 204, 258
100-1015	R16, 61, 70, 78, 83, 86, 91, 94, 147, 150, 187, 238
100-1025	R79, 80, 81, 87, 88, 89, 122, 154, 170, 182, 183, 185, R193, 200, 222, 230, 232, 241, R243, 255, 256
100-1035	R45, 130, 194, 210, 226, 227, 242,
100-1055	R85
100-1235	R55, 132
100-1515	R155, 171, 179
100-1525	R54, 131
100-2255	R77
100-2265	R160
100-2215	R121, 157, 167, 191, 246, 260
100-2225	R115, 117, 128, 159, 221
100-2235	R233
100-3305	R5, 6, 19, 20, 21, 22, 32, 33
100-3315	R229, 236, 245, 265
100-3325	R92
100-3335	R59, 68
100-3345	R84
100-3915	R202
100-4705	R166
100-4715	R8, 24, 39, 56, 62, 64, 71, 73, 82, 90, 175, 205, 199, 212, R251, 262, 263, 264
100-4725	R101, 107, 109, 111, 133, 135, 138, 198, 206, 211
100-4735	R190, 197, 209
100-4745	R76
100-6805	R231, 234, 237
100-6815	R153, 169, 223, 224
100-6825	R158
100-8235	R129
101-1015	R261
101-0125	R3, 4, 10, 11
101-0335	R18, 93
101-0565	R14, 15
101-1025	R161, 259
101-1525	R151, 152, 165, 166, 225, 239
101-1815	R7
101-2225	R240
101-3315	R23
101-4705	R27, 38
101-6805	R180
104-1960	R34, 35
104-3480	R13
107-1000	R42, 65, 74
107-1001	R37, 43, 63, 72, 113
107-1002	R44, 46, 99, 100, 103, 104, 126, 127, 186
107-1003	R116, 125, 143, 144
107-1101	R105
107-1331	R41
107-1471	R31, 162
107-1473	R120
107-1961	R196, 208, 228
107-1962	R148, 149, 188, 195, 207
107-1963	R96
107-2151	R189
107-3161	R114, 203
107-3481	R184
107-3482	R97
107-4221	R244
107-4222	R124
107-5111	R119
107-5112	R95
107-5113	R58, 67

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
107-5620	R106
107-6810	R192
107-6811	R98
107-6812	R123
107-9091	R118
107-9093	R146
109-0002	R1, 9
109-0003	R156, 172
109-2715	R181
110-0011	R164
121-1020	R30, 163
121-1030	R57, 66, 75, 145
121-2041	R60, 69
121-5020	R201
130-1005	C26, 29
130-1015	C31, 33
130-3305	C25, 28
130-4715	C27, 30, 32, 36
130-7515	C38
131-1030	C42, 57, 61
131-2220	C19, 41
131-4720	C37
131-4730	C46, 103
131-6820	C45, 47
132-1041	C10, 14, 58, 59, 62
132-1062	C39, 40
132-2262	C56, 65, 68, ..75
132-2752	C54, 55, 70, 76 THRU 98, 100, 101, 48, 104
135-1002	C102
135-4742	C21, 51, 52, 59, 60, 66, 74
139-2261	C13, 20
139-4751	C63
139-6845	C2, 4, 5, 8, 9, 18
142-1070	C1, 15
200-1460	Q2
200-4037	Q6
200-4123	Q15, 18, 26 THRU 31
200-4125	Q9, 10, 12, 13, 16, 17, 24, 35
200-4400	Q20, 21, 36
200-4402	Q1, 3, 4, 5, 8, 19, 25, 34
200-5323	Q33
201-0126	SCR1, 2, 3
204-0074	Q11, 14
205-4010	SCR5

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
300-4002	CR25, 26, 28, 47
300-4446	CR5 THRU 24, 27, 30 THRU 42
330-0565	VR4, 7
330-0685	VR1, 2, 5, 6
330-1001	VR17
330-1205	VR20
331-0275	VR19
331-0335	VR12
331-0395	VR8, 9, 16
331-0512	VR3
331-0605	VR10, 11, 13
331-0825	VR14
400-0207	U13
400-0301	U33, 34
400-0305	U21
400-0307	U8, 11, 14, 15, 16, 17, 22, 27, 30, 37, 38
400-0326	U18
400-5558	U12
403-0002	U23, 26
502-1243	K1
515-1015	L1
700-5107	U1, 6, 19, 20
700-7404	U9, 25, 32
700-7416	U24
700-7438	U10
700-7450	U31
710-4164	U35, 36
710-7400	U28, 40, 44
710-7402	U42
710-7404	U39
710-7474	U41, 43
710-7486	U29

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	C3	
		VALUE	PART NO.
-01	BASIC	--	OMIT

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	R2	
		VALUE	PART NO.
-01	BASIC	--	OMIT

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	R112		
		VALUE	PART NO.	VA
-01	BASIC	90.9K	107-9092	9

[13] TABLE VI

PART NO.	REFERENCE DESIGNATIONS
200-3055	Q1, 2
200-6051	Q4
200-6058	Q3, 5

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-WF PRE PROD. RELEASE	9/15/76			
B	ECN 9246	11/29/76	SK		
C	ERN 9522	1/25/77	RJ		CL
D	ECN 9821A				CL
E	ECN 9900	4-26-77	RJ		CL
	ERN 9-TT PROD. RELEASE	5/31/77			CL
F	ECN 10315	7/13/77			
G	ECN 10484	8-22-77	DP		CL
H	ECN 10534	10-5-77			CL
J	ECN 11817	9/2/78	HM		
K	ECN 11947	10/30/78	HM		
L	ECN 12465	12/6/78			
M	ECN 12828	3/21/79		BB	mm

(2) TABLE II

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	C3		C6		C7		C11		C12		C16		C17		C24		C43		C44		C67		C69	
		VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	BASIC	--	OMIT	--	OMIT	--	OMIT	--	OMIT	--	OMIT	.0047	131-4720	.001	131-1020	--	OMIT	.001	131-1020	--	OMIT	---	OMIT	--	OMIT

(2) TABLE II (CONTD)

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	R2		R12		R17		R25		R26		R28		R29		R40		R47	
		VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	BASIC	--	OMIT	--	OMIT	--	OMIT	10	100-1005	470	101-4715	.15	118-0013	14.7	104-0147	5.11K	107-5111	6.81K	107-6811

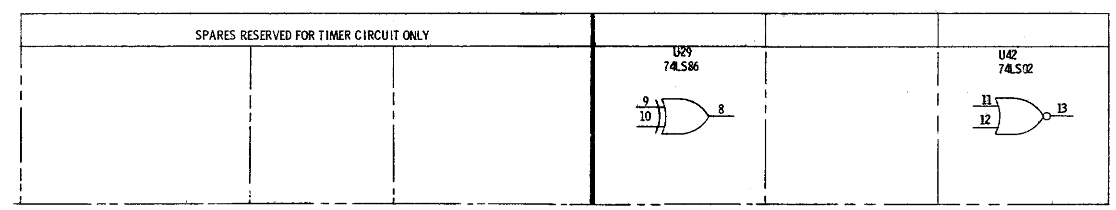
ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	R48		R49		R50		R51		R52		R53		R102		R108		R110	
		VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	BASIC	10K	107-1002	16.2K	107-1622	19.6K	107-1962	34.8K	107-3842	61.9K	107-6192	90.9K	107-9092	100K	107-1003	100K	107-1003	90.9K	107-9092

(2) TABLE II (CONTD)

ASSEMBLY 108131 VERSION NO.	VERSION CHARACTERISTIC	R112		R134		R136		R137		R139		R140		R141		R142		R235						VR15		VR18	
		VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.					VALUE	PART NO.	VALUE	PART NO.
-01	BASIC	90.9K	107-9092	9.09K	107-9091	2K	121-2020	8.25K	107-8251	9.09K	107-9091	68.1K	107-6812	--	OMIT	56.2K	107-5622	100	100-1015					16.0V	331-1605	16.0V	331-1605

(5) TABLE V

SPARE LOGIC ELEMENTS

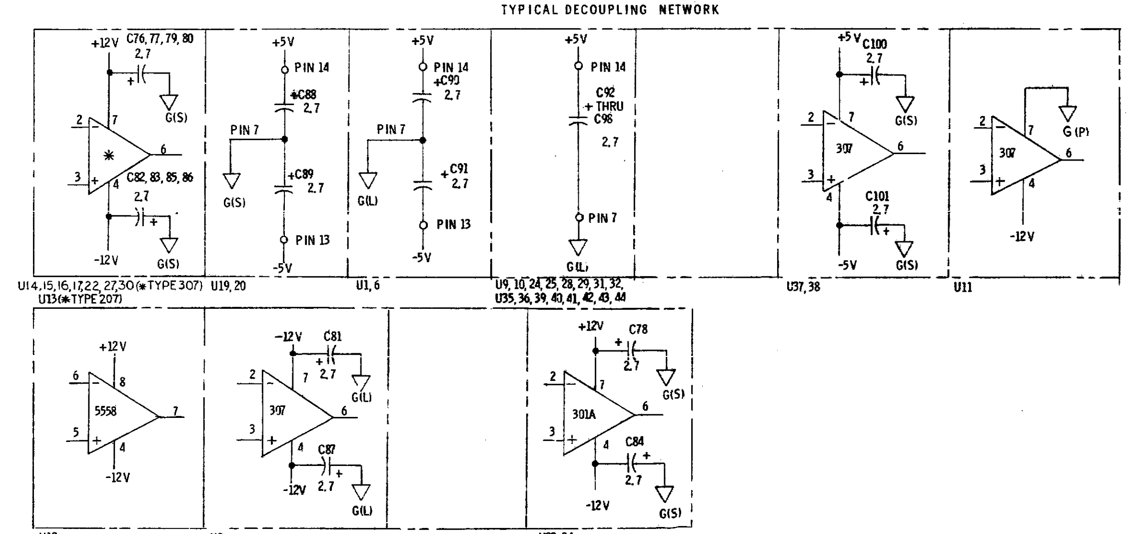


(13) TABLE VI

PART NO.	REFERENCE DESIGNATIONS
200-3055	Q1, 2
200-6051	Q4
200-6058	Q3, 5

REFERENCE DESIGNATIONS					
LAST USED		NOT USED		DELETED	
BASIC	(13)	BASIC	(13)	BASIC	(13)
C104		C34, 35		(14)	
CR47				(14)	
K1					
L1					
Q36	Q5			(14)	
R265				(14)	
SCR5				SCR4	
TP30				TP1,3,25	
U44	U1			(14)	U1
VR20					
W14				(14)	
XK1					

TYPICAL DECOUPLING NETWORK



(14) CR1 THRU CR4, 29; R177, 178, 213, 214, 215, 216, 217, 218, 219, 220; W1 THRU W4; CR43,44,45,46; C22,23;C49,50,64,71,72,73,99;Q7,22,23,32: R36,247. 248,249,250,251,252, 253,R254; U2,3,4,5,7.

(13) FOR PART NO. OF COMPONENTS MOUNTED EXTERNAL TO PCBA, SEE TABLE VI.

12. (RESERVED)

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

10. DIODES ARE 1N4446.

9. PNP TRANSISTORS ARE 2N4125.

8. NPN TRANSISTORS ARE 2N4123.

7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 35V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W, (1% TOL ARE 1/8W).

(5) FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

4 (RESERVED)

3. (RESERVED)

(2) FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER. SEE TABLE II.

(1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER. SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NUMBER 108131

REFERENCE DRAWING

108131	D3600 EXT
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. T. Walton	9-15-76
CHK	
DES	
ENGR AK DESAI	10-1-76
PROJ. ENGR AK DESAI	10-1-76

FINISH:

MATL:

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE SCHEMATIC, SERVO BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
J		108130	M

SCALE —— DO NOT SCALE DWG SHEET 1 OF 4

18-02

POWER SUPPLY REGULATORS

PART OF J201 — 7 — +25V R/W SUPPLY

FROM POWER SUPPLY

(KEY 1,5,8) J212 — 25VAC (PK) — 25VAC(PK) -1

(KEY 2,4,6) PART OF J209 — W5, W6 — +25 VUR OR +20 VUR — R258 10

C1 100, +75%-10%, 30V — 6 (P)

R2 — C3 [2] — PART OF J204 P204 — Q1 2N3055 [13]

+25VDC(RAW) 11, 12 — R1 2 3% 5W — C2 6.8 10%

TP26 TP29 — G (L) G (P) G (S) — MAIN GROUND 4, 5, 2 — SHIELD

+12V REGULATOR — U18 326 (+B, +CS, N.C., +CL, VIN, NC, VIN, GND, -CL, REF, -CS, NC, -VO, -B)

R3 1.2 1/2W — R4 1.2 1/2W — C5 6.8 10% — C6 [2] — C4 6.8 10%

C7 [2] — R12 [2] — C8 6.8 10% — C9 6.8 10%

R10 1.2 1/2W — R11 1.2 1/2W — -12V REGULATOR

TP20

R5 33 — R6 33 — Q1 2N4402 — VR1 IN4736A 6.8V 1W — VR2 IN4736A 6.8V 1W — R7 180 1/2W — R8 470 — C10 1 10% — SCR1 2N6394 OR TIC126F

VR3 IN5231 5.1V 2% — C11 [2] — -5V REGULATOR — U11 307 — R16 100 — Q3 2N4402 — C12 [2] — R13 348, 1%, 1/4W — R14 5.6 1/2W — R15 5.6 1/2W — R17 [2] — Q2 TIP146 — R18 3.3 1/2W

C13 22 10% 15V — R19 33 — Q4 2N4402 — R20 33 — R21 33 — R22 33 — Q5 2N4402 — VR4 IN4734A 5.6V, 1W — VR5 IN4736A 6.8, 1W — VR6 IN4736A 6.8, 1W — R23 330 1/2W — R24 470 — C14 1 10% — SCR2 2N6394 OR TIC126F

TP7 — TP17

PART OF J209 — W9 — +12V

PART OF J211 — W13, W14 — -5V — -12V

J210 (KEY 1,3,5)
- 3 +12V
- 1 GND
- NC 9 -5V SENSE
- 6 -5V
- 12 -12V

TO LOGIC BOARD

-25VDC(RAW) 3, 6 — R9 2 3% 5W

PART OF J211 (KEY 2,5,6) — W11, W12 — C15 100, +75%-10% 30V — 5 (P) — -25VUR OR -20VUR

(KEY 1,4,5) J208 P208 — Q2 [13] 2N3055 — Q3 2N6058 [13] — OR — PART OF P208 — Q3 [13] 2N3055 2N3771

R25 C16 — R26 ½W — R27 47 1/2W

+10VDC(RAW) 8, 9

Q6 2N4037 — C17 [2] — R28 3% [2] 10W — +5V REGULATOR

R29 1% 1/4W [2] — R30 1K, 10%, 3/4W CW — R31 1.47K 1% — U21 305A (BO, CS, VO, VIN, COMP, GND, RB, FBK) — C19 .0022, 10%, 100V

C18 6.8 10% — C20 22 15V

R34 196, 1%, 1/4W — R35 196, 1%, 1/4W — R37 1K 1%

R32 33 — R33 33 — Q8 2N4402 — R38 47 1/2W — R39 470 — C21 47, 50V — SCR3 2N6394 OR TIC126F — VR7 IN4734A 5.6 1W

TP24 — PART OF J209 — W7, W8 — +5V

J217 — +5V(AUX) TO LOGIC BOARD

J210
- NC 2 +5V SENSE
- 7, 8, 10 +5V
- NC 11 GND SENSE
- 4, 5 GND

G (L)

MAIN GROUND 10, 7

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				

PART OF J201
+25V R/W SUPPLY

PART OF J09
+12V
J210
(KEY1,3,5)
3 +12V
1 GND
NC 9 -5V SENSE
6 -5V
12 -12V
-5V
-12V

TO LOGIC BOARD

J217
+5V(AUX) TO LOGIC BOARD

PART OF J09
+5V
NC 2 +5V SENSE
7
8 +5V
10
NC 11 GND SENSE
G(L)
4
5 GND

PART OF J201 (KEY 34)

NLAD6G 32 — U44 13,12,11 74LS00 — U39 5,6 74LS04 — CR5 — R40 1% — CR6
NLAD7G 31
15
16
NLAD6G 33 — U44 2,1,3 74LS00 — U39 3,4 74LS04 — CR7 — R47 2 1% — CR8
13
NLAD5G 30 — U44 4,5,6 74LS00 — U39 1,2 74LS04 — CR9 — R48 2 1% — CR10
12
NLAD4G 29 — U44 10,9,8 74LS00 — U39 13,12 74LS04 — CR11 — R49 2 1% — CR12
11
NLAD3G 28 — U40 2,1,3 74LS00 — U39 11,10 74LS04 — CR13 — R50 2 1% — CR14
10
NLAD2G 27 — U40 9,10,8 74LS00 — U39 9,8 74LS04 — CR15 — R51 2 1% — CR16
1
SPARE 8 — U40 5,4,6 74LS00 — CR17 — R52 2 1% — CR18
NLADIG 18
2
NLADOG 19 — NC
R53 2 1%
LFDX1 21 — U42 2,3,1 74LS02 — U40 13,12,11 74LS00 — CR19 — Q10 — CR20 — Q11 TIS-74 D,S,6
3
PART OF J202 G(L)

+12V
R41 1.33K 1%
Q9
R42 100 1%
G(S)
R43 1K 1% — C24 2 10% 100V
U30 307 2,3,6
R44 10K 1%
R45 10K
U27 307 2,3,6
R46 10K 1%
TP18
SVRVA 13-8G1 (VEL REF VEL MODE)

VELOCITY REFERENCE CIRCUIT

+5V
R54 1.5K
R55 12K — -12V
G(S)

+5V
R56 470
U32 11,10 7404
SC036 3-13B

ELECTRONIC VELOCITY FEEDBACK POLARITY GENERATOR

SL116 3-13B
U32 1,2 7404 — G(L)
SPQCG 3-15F
U41 74LS74 PR,D,CK,CL,Q,Q
U42 6,5,4 74LS02
U42 9,8,10 74LS02
SPCXA 4-7D — U29 4,5,6 74LS86 — G(L)
SPCXG 3-14C
SPRCG 3-15H
U32 13,12 7404
U31 7450 2,3,4,5,6
U31 7450 13,1,10,9,8
U28 74LS00 1,2,3
U28 74LS00 4,5,6
SFWDG 13-11B1

SIZE	CODE IDENT NO.	DWG NO.	REV
J		108130	M
SCALE —	DO NOT SCALE DWG	SHEET 2 OF 4	

POSITION TRANSDUCER SIGNAL CONDITIONERS

ELECTRONIC VELOCITY FEEDBACK (POSITION MODE)

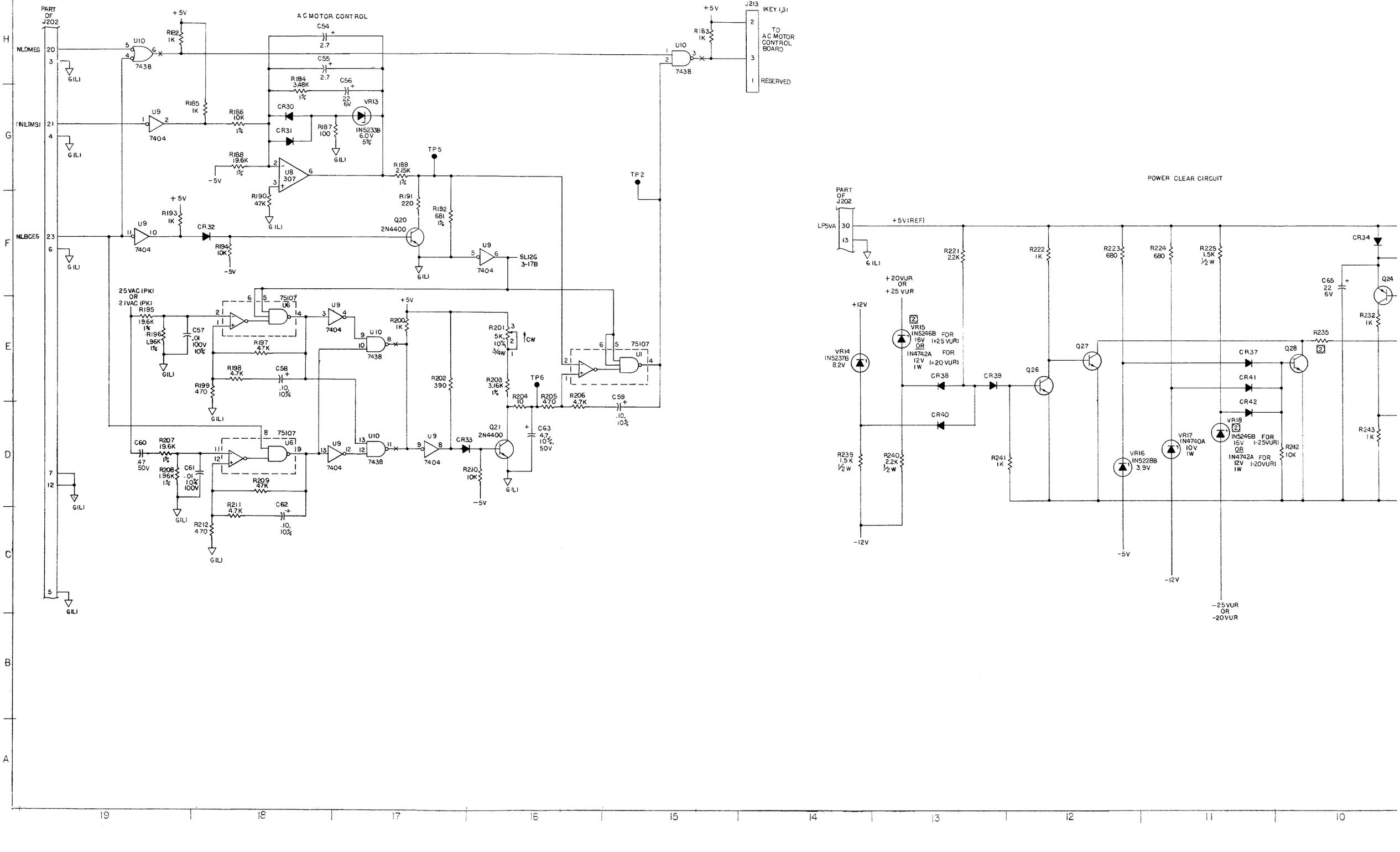
MODE CONTROL

ELECTRONIC VELOCITY FEEDBACK (VELOCITY MODE)

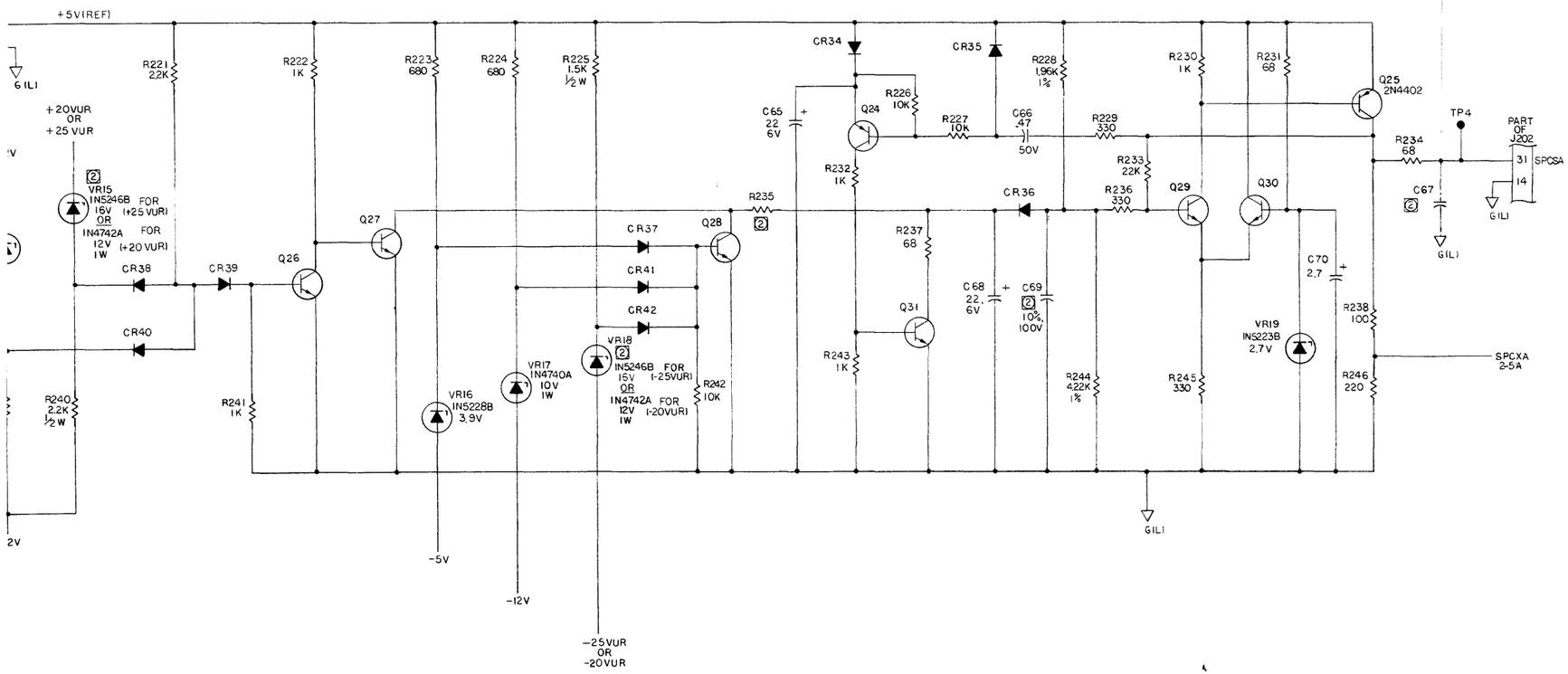
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				

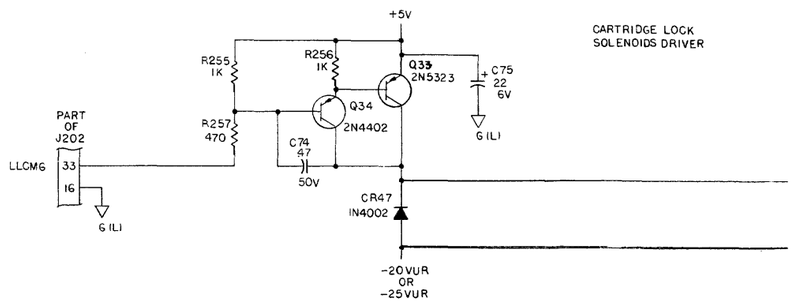
R100 10K 1%
R103 10K 1%
R104 10K 1%
R105 1.1K 1%
R106 562 1% GISI
C39 10, 10V
C40 10, + 10V
U12 5558
U24 7416
+5V
PART OF J201
NLVREG 20
LPMXG 22
R133 4.7K
R135 4.7K
R138 4.7K
R134 1% SVRVA 2-16 (VEL. REF. VEL. MODE)
R136 10% 3/4W
R137 1%
R139 1%
R140 1%
R141 1%
R142 1%
J215 (KEY 2,4,6)
FROM TEMP COMP BOARD
SPARE
(RESERVED)
U23 5012
VELOCITY/POSITION MODE CONTROL
TP11
TP9
R143 100K 1%
C43 10% 100V
R144 100K 1%
+12V
R145 10K, 10%, 3/4W
R146 309K, 1%
-12V
CR23
CR24
VR10 VR11 IN5233B 6V
R147 100
U16 307
R158 6.8K
TP10
POSITIONER POWER AMPLIFIER
R148 19.6K 1%
R149 19.6K 1%
C44 10% 100V
U14 307
R150 100
R159 2.2K
R162 1.47K 1%
R164 0.10, 3% 10W
R163 1K, 10%, 3/4W
TP30
+25VUR OR +20 VUR
-20VUR OR -25VUR
R153 680
R154 1K
R156 0.10, 3% 5.5W
R155 150
CR25 IN4002
Q16
R151 1.5K 1/2W
R152 1.5K 1/2W
C45 .0068, 10% 100V
R157 220
Q15
R160 22
R161 1K 1/2W
Q17
R165 1.5K 1/2W
R166 1.5K 1/2W
C47 .0068, 10% 100V
R167 220
Q18
R169 680
R171 150
R170 1K
R172 0.10, 3% 5.5W
CR26 IN4002
TP22
C46 .047 10% 100V
R168 47
PART OF J204 P204 (KEY 1,2,4)
Q4 2N6051
Q5 2N6058
J214
EMERGENCY UNL DRIVER
EMERGENCY UNL CAPACITOR
POSITIONER CURRENT SENSE
R173 10
C51 47, 50V
C52 47, 50V
R174 10
SCR5
Q35
Q36 2N4400
R260 220
R265 330
R261 100 1/2W
C102 .001 10% 1000V
R262 470
R263 470
C103 .047 10% 100V
R264 470
L1 100UH 5%
C53 47 50V
PART OF J202 (KEY 24)
S10SS
J205 (KEY 1)
TO POSITIONER
-12V OR -10V
NC
K1
CR28 IN4002
R180 68 1/2W -12V
PART OF J202
LEUEG 32
15
CR27
VR12 IN5226B 3.3V
R175 470
R176 3.9
R179 150
Q19 2N4402
C48 2.7
C104 2.7
EMERGENCY UNLOAD RELAY DRIVER
J206 (KEY 1,2)
TO EMERGENCY UNLOAD CAPACITOR
R259 1K 1/2W
VR20 IN4742A 12V 1W
R181 270 5W -25V
R125 100K 1%
C41 .0022, 10%, 100V
R123 68.1K
R124 42.2K 1%
R128 2.2K
C42 .01, 10%, 100V
R129 82K
R126 10K 1%
R130 10K
R127 10K 1%
TP12
U17 307
U15 307
Q12
+5V
R131 1.5K
CR21
Q13
CR22
Q14 TIS74
R132 12K
-12V
GISI
GILI
GIPI

SIZE	CODE IDENT NO.	DWG NO.	REV
J		108130	M
SCALE —	DO NOT SCALE DWG.	SHEET 3 OF 4	

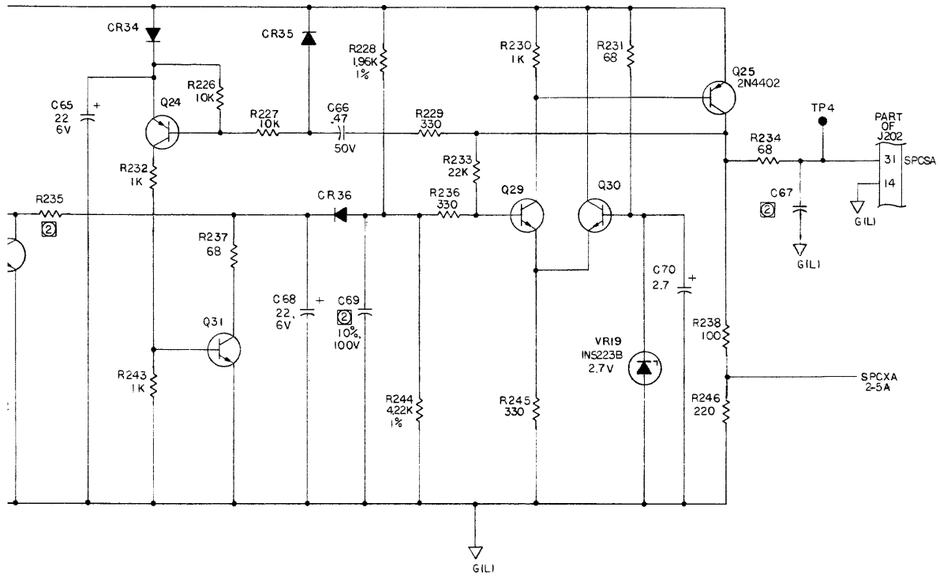

AC MOTOR CONTROL
PART OF J202
NLDMEG
NLITMSI
NLBCES
+5V
-5V
G(L)
U10
7438
U9
7404
U8
307
R182 1K
R183 1K
R184 348K 1%
R185 1K
R186 10K 1%
R187 100
R188 19.6K 1%
R189 2.15K 1%
R190 47K
R191 220
R192 681 1%
R193 1K
R194 10K
C54 2.7
C55 2.7
C56 22 6V
CR30
CR31
VR13 IN5233B 6.0V 5%
CR32
Q20 2N4400
TP2
TP5
SL12G 3-17B
J213 (KEY 1,31)
TO AC MOTOR CONTROL BOARD
RESERVED
25 VAC (PK) OR 21 VAC (PK)
R195 19.6K 1%
R196 1.96K 1%
R197 47K
R198 4.7K
R199 470
C57 .01 100V 10%
C58 .10 10%
75107 U6
U11
R200 1K
R201 5K 10% 3/4W CW
R202 390
R203 3.16K 1%
R204 10
R205 470
R206 4.7K
C59 .10 10%
TP6
C63 4.7 10% 50V
Q21 2N4400
CR33
R210 10K
C60 .47 50V
R207 19.6K 1%
R208 1.96K 1%
C61 .01 10% 100V
R209 47K
R211 4.7K
C62 .10 10%
R212 470
POWER CLEAR CIRCUIT
LPSVA
+5V(REF)
+20VUR OR +25 VUR
+12V
VR14 IN5237B 8.2V
VR15 IN5246B 16V (+25 VUR) FOR OR IN4742A 12V (+20 VUR) 1W
R221 2.2K
R222 1K
R223 680
R224 680
R225 1.5K 1/2W
R235
CR34
C65 22 6V
Q24
R232 1K
Q26
Q27
Q28
CR37
CR38
CR39
CR40
CR41
CR42
VR16 IN5228B 3.9V
VR17 IN4740A 10V 1W
VR18 IN5246B 15V (-25VUR) FOR OR IN4742A 12V (-20VUR) 1W
R239 1.5K 1/2W
R240 2.2K 1/2W
R241 1K
R242 10K
R243 1K
-12V
-25VUR OR -20VUR

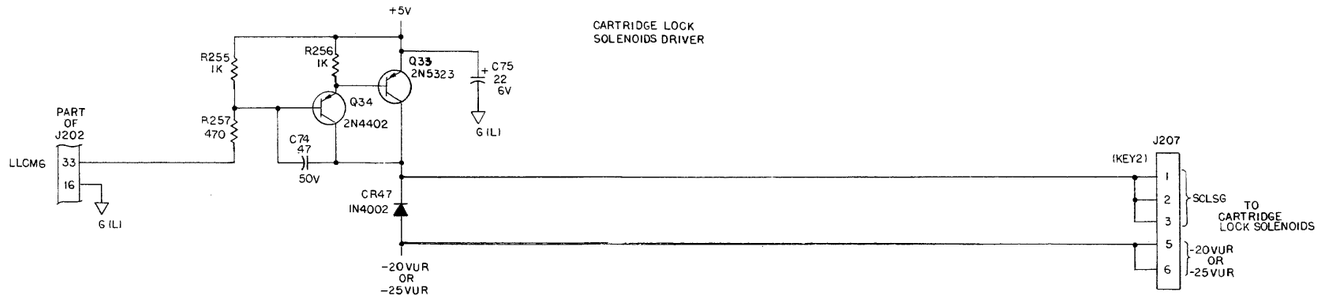
POWER CLEAR CIRCUIT





REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				





SIZE	CODE IDENT NO.	DWG NO.	REV
J		108130	M
SCALE ——	DO NOT SCALE DWG	SHEET 4 OF 4	

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-DK 108 PROD RELEASE	5/6	RM	[illegible]
B	ECN 0220	5/27	RJ	[illegible]
	ERN 9-TR PROD REL	6/7	CJ	-	-

[2] TABLE II

C16		C18		C21		C22, 23		C24, 25		C33		C36, 37		C39, 40	
VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.
68 PF	130-6805	39 PF	130-3905	39 PF	130-3905	.0022 100V	131-2220	68 PF	130-6805	22 PF	130-2205	150 PF	130-1515	33 PF	130-3305
39 PF	130-3905	15 PF	130-1505	22 PF	130-2205	.001 1 KV	135-1002	47 PF	130-4705	15 PF	130-1505	68 PF	130-6805	22 PF	130-2205

[2] TABLE II (CONT'D)

R30		R31, 32		R36		R48		R78, 84		
VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	VALUE	PART NO.	
1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	4.64K	107-4641	
1.21K	104-1211	147	104-1470	560	102-5615	1K	107-1001	5.62K	107-5621	

[4] TABLE IV

VOLTAGE AND GROUND PIN NO.			
	GND	+6.8V	-6.8V
		3	10
	7		
	7		
	7		
	7		
	7		
	7		
	7		
	7		
	7		
	8		
	8		

[5] TABLE V

SPARE LOGIC ELEMENTS	
TYPE	REFERENCE DESIGNATION
7416	U8F, U8A
74S74	U18B
7400	U10A
74S74	U5A
7404	U12E
74LS20	U11A

[12] TABLE VI

CONFIGURATION	JUMPERS
READ ALWAYS ENABLE	W7 + W9
SYNCHRONOUS READ ENABLE	W8 + W10
ASSYNCHRONOUS READ ENABLE	W9 + W10
PULSE DATA, PULSE CLOCK	W3 + W5
LEVEL CHANGE DATA, PULSE CLOCK	W3 + W6
COMPOSITE DATA ONLY	W4 + W5

[12] FOR JUMPER CONFIGURATIONS (REF J303) REFER TO TABLE VI. FOR PROGRAMMING ARRAYS REFER TO 104134.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING WITH THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS TIME ZONE NO.

10. DIODES ARE 1N4448.

9. PNP TRANSISTORS ARE 2N4125.

8. NPN TRANSISTORS ARE 2N4123.

7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL 1% ARE 1/8W.

[5] FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

[4] FOR I.C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS. SEE TABLE IV.

3. (RESERVED)

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY DWG. NO. 108141

REFERENCE DRAWINGS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. [illegible]	5/16
CHK. [illegible]	5/26
ENG.	
MNGR. [illegible]	5/26
PROJ. MGR.	

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE: SCHEMATIC READ/WRITE

108-4	DOCUMENT
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH: MATL:

SIZE J | CODE IDENT NO | DWG. NO. 108140 | REV B
SCALE | DO NOT SCALE DWG | SHEET 1 OF 3

PART OF J305 (KEY 15)

HEAD SELECT

NLLPSG 32

NLLPSG 3-20

TP6

TP8

NLUPSG 3-2E

NLUPSG 24

NLUHSG 25

NLWDFT 27

NLWMXG 28

LDAMG 21

NLECEG 29

NTLOMG 23

NTLOPG 22

NLRECG 18

NTTREG 3-2E

SPCSA 26

RRGCG 3-16B

RRECG 3-3B

U3 7416

U6 7404

U4 74LS00

U8 7416

U13 7402

U12 7404

U10 7400

U5 74S74

+12V

+5V

-12V

R1 1K

R2 4.7K

R3 1K

R4 4.7K

R5 1K

R6 4.7K

R7 1K

R8 4.7K

Q1

Q2

Q3

Q4

R9 47

R10 47

R11 47

R12 47

R13 150

R14 330

R15 1K

R16 1K

C1 2.2

R17 110 1%

R18 150

R19 1K

R20 422 1%

R21 422 1%

C2 2.2

Q5

Q6

Q7 2N2219A

Q8 2N2219A

CR1

VR1 IN4740A

CR2

CR3

CR4

W

W2

PART OF J310

WRT DRV1

WRT DRV2

PART OF J311

PLAT SEL2

PLAT SEL

+12VDC

-12VDC

HEAD SEL1

HEAD SEL2

HEAD SEL3

HEAD SEL4

WRT MODE

READ SW

ERASE DRV

MULT HD SEL

J304 (KEY 1,5,8,10)

-12V

S12SS

-5V

+12V

GND

+5V

L1 68UH 5%

L2 68UH 5%

C7 2.2

C8 2.2

C9 70 +100 -10%

R22 10

TP1

TP7

C10 22

C11 2.2

C12 2.2

R23 1.5K

CR5

R24 1K

R25 1K

R26 390

Q13

Q14

R27 1K

R28 1.5K

Q9

R29 1K

R30 1%

Q10

R31 1%

R32 1%

R33 1K

R34 470

Q11

R35 470

R36 1W

C3

Q12 2N4400

TP3

R37 1K

CR6

R38 470

Q15 2N3053

C4 .01 10% 100V

R39 1K

C5 .01 10%, 100V

Q16 2N4400

R40 1K

R41 5.6K

C42 .001 10% 1KV

R42 100

R43 7.5K 1%

Q17

CR7

R44 1K

C6 .047 10% 50V

U11 74LS20

RWECG 3-3F

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

PART OF J311

7 PLAT SEL2
10 PLAT SEL1
5
12
8
+12VIFB 9 +12VDC
6
-12VIFB 11 -12VDC
1 HEAD SEL1
16 HEAD SEL2
15 HEAD SEL3
14 HEAD SEL4
2 WRT MODE
13 READ SW
4 ERASE DRV
3 MULT HD SEL

PART OF J310

13 WRT DRV1
2
4
12 WRT DRV2

+12V
R1 1K
R2 4.7K
Q1
R3 1K
R4 4.7K
Q2
R5 1K
R6 4.7K
Q3
R7 1K
R8 4.7K
Q4
R12 47
R11 47
R10 47
R9 47
U8 7416
U8 7416
+5V
R16 1K
C1 2.2
R17 110 1%
Q5
R18 150
Q7 2N2219A
CR1
VR1 IN4740A
CR3
CR4
CR2
R20 422 1%
C2 2.2
R21 422 1%
Q6
Q8 2N2219A
-12V
W1
W2
R27 1K
R28 1.5K
Q9
R30 2 1%
Q10
R31 2 1%
R32 2 1%
R29 1K
R33 1K
R34 470
Q11
R36 2 1W
C3 2
Q12 2N4400
R35 470
TP3
R37 1K
R38 470
+5V
Q15 2N3053
C4 .01 10% 100V
CR6
U6 7404
R39 1K
C5 .01 10% 100V
Q16 2N4400
R40 1K
U10 7400
U8 7416
C6 .047 10% 50V
+5V
R41 5.6K
C42 .001 10% 1KV
R42 100
Q17
CR7
R43 7.5K 1%
-12V
+5V
R44 1K
U11 74LS20
U10 7400
RWECG 3-3F

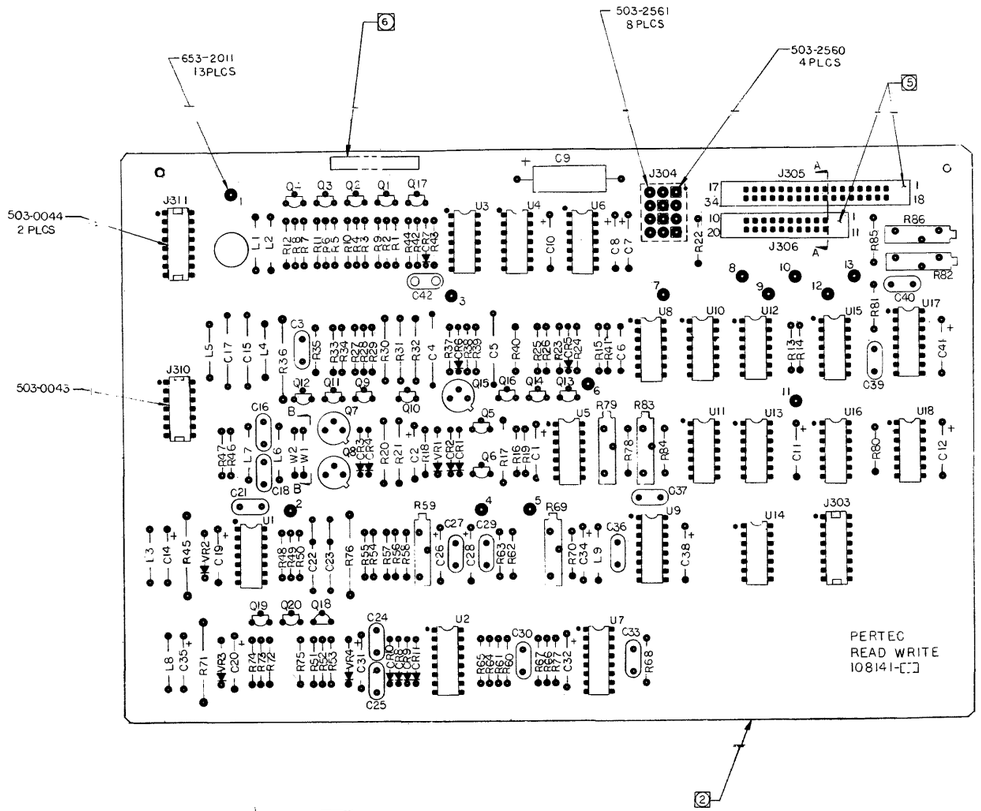
SIZE	CODE IDENT NO.	DWG. NO.	REV
J		108140	G
SCALE	DO NOT SCALE DWG.	SHEET 2 OF 3	

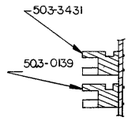
REVISIONS				
REV	DESCRIPTION	DATE	BR.	CHK. APPR.
	SEE SHEET 1			

+5V
R79 5K 10% 3/4W
CW
R78 1%
C36 5% 500V
SHORT ONESHOT
U9
74123
74LS74
U14
74S10
U16
U15
TP10
+5V
R82 5K 10% 3/4W
R81 511K 1%
C39 5% 500V
U17
74123
R80 1K
TP11
TP12
TP13
PART OF J305
20 NRRCSG
RWECG 2-4A
30 RWECG
19 NRRDSG
17 POSITION MODE
34 INDEX/SECTOR PULSE
33 10 MS TIMER
31 10MIN TIMER
PART OF J306 (KEY 15)
1
2
3
4
NOT USED
NTTREG 2-11D
5 NTTREG
7
9
10
NLUPSG 2-11G
6
NLLPSG 2-11H
8
16
+5V
17
18
19
20
-5V
11
12
13
14
TO TEMP COMP PCBA
R83 5K 10% 3/4W
R84 1%
C37 5% 500V
LONG ONESHOT
U9
74123
C38 2.2
7402
U13
R86 5K 10% 3/4W
R85 511K 1%
C40 5% 500V
U17
74123
C41 2.2
PART OF J303
W3
W4
W5
W6
W7
W8
W9
W10
U16
74S10
U18
74S74
7404
U6
74LS74
U14
RRECG 2-11D

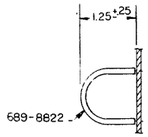
SIZE	CODE IDENT NO.	DWG NO.	REV
J		108140	E
SCALE	DO NOT SCALE DWG.	SHEET 3 OF 3	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-DK PRE PROD. RELEASE	4/4/86	SEN		
B	ECN 9806	5/5/87	RJ		
	ERN 9-TR PROD RELEASE	6/2/87			
C	ECN 11480	5/3/89			
C1	ECN 12494	1/19/90	L-R		
D	ECN 13745	3/4/92	LM		
D1	ECN 14810	10/6/92			

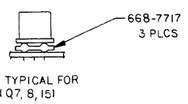




SECTION A-A
MTG DETAIL FOR J305 AND J306



SECTION B-B
W1 AND W2



TYPICAL FOR
1 Q7, 8, 151

SCHEMATIC: 108140
REF DRWG:

6 MARK WITH PART NO. 108141, VERSION NO. 3 AND VERSION ISSUE LETTER IN NOTED AREA.

5 REMOVE PIN 15 FOR J305 AND J306 CONNECTOR KEYING.

4.

3.

2 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 108142-01 REV B AND SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

PART NO. 108141-01 REV C1

LIST OF MATERIAL

QTY. MOD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± ANGULAR ± 1/2°
XXX ±
X ±
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. T. MORTON	3/4/92
CHK. Dennis Bean	3-4-92
DES.	
ENGR. [illegible]	[illegible]
PROJ. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
READ/WRITE

NEXT ASSY	USED ON
APPLICATION	03400EXT

FINISH:

MATL: SEE L/M

SIZE E | CODE IDENT NO | DWG NO. 108141 | REV D1

SCALE 2/1 | DO NOT SCALE DWG | SHEET | OF 1

DWG NO. 108141 REV D1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-75 PRE PROD RELEASE	7/75	RW	RB	RB
B	ECN 10107	10/75	LT	RB	RB
	ERN 9-75 PROD RELEASE	10/75	LT	RB	RB
C	ECN 11419	5/77	LT	RB	RB
C1	ECN 13153	5/78	MP	RB	RB

TABLE I (1)

PART NO.	REFERENCE DESIGNATION
100-1025	R2, 3, 5, 8, 11
100-1035	R31, 32
100-1235	R6, 9, 41, 43, 45, 47, 49, 51, 53, 55
100-3325	R4, 7, 13, 15, 17, 19, 21, 23, 25, 27
100-4715	R1, 12, 14, 16, 18, 20, 22, 24, 26
100-4725	R10
101-1025	R35
107-1002	R28, 29, 40, 42, 44, 46, 48, 50, 52, 54
107-1781	R33, 34
135-1031	C3, 5
135-2272	C1
139-2244	C2
200-4402	Q1 THRU Q13
300-4446	CR1 THRU 27,29,57 THRU 66
300-0115	CR28,30 THRU 56
400-0592	U1
515-1015	L1

TABLE II (2)

VERSION NUMBER	VERSION CHARACTERISTIC	C4		C6	R30		R36	R37, 38		R39				L2			
		VALUE	PART NO.	135-4731	VALUE	PART NO.		VALUE	PART NO.	VALUE	PART NO.			VALUE	TOL	PART NO.	
-01	2200 BPI / 1500 RPM	22PF	130-2205	USE	1.0K	100-1025	OMIT	422	107-4220	68	100-6805			33UH	5 %	515-3305	
-02	2200 BPI / 2400 RPM	OMIT	OMIT	USE	1.0K	100-1025	OMIT	422	107-4220	68	100-6805			15UH	10 %	515-1500	
-03																	
-04																	

REFERENCE DESIGNATIONS

LAST USED	DELETED
C6	
CR66	
L2	
Q13	
R55	
U1	

(3) CR28,30 THRU 56 ARE PERTEC P/N 300-0115.

8. ALL DIODES ARE IN4446.
7. (RESERVED)
6. ALL TRANSISTORS ARE 2N4402.
5. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 100V.
4. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL 1% RESISTORS ARE 1/8W.
3. (RESERVED)

(2) FOR VALUE, PART NO. AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II

(1) FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

PCBA NO: 108146

REFERENCE DWGS:

QTY. REQD	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX = ±
XXX = ±
X = °
MACHINED ± 1/2°
BREAK ALL SHARP CORNERS
.XX = .010

SIGNATURES	DATE
DR. R. SORG	12/19/75
CHK. R. Bruce	12/26/75
DES.	
ENGR. M. Bisconti	10/6/76
PROJ. ENGR.	

PERTEC PERIPHERAL EQUIPMENT

TITLE: SCHEMATIC, R/W SELECT. MATRIX & PREAMP

108146	D36 EXT
NEXT ASSY	HIT USED ON
APPLICATION	

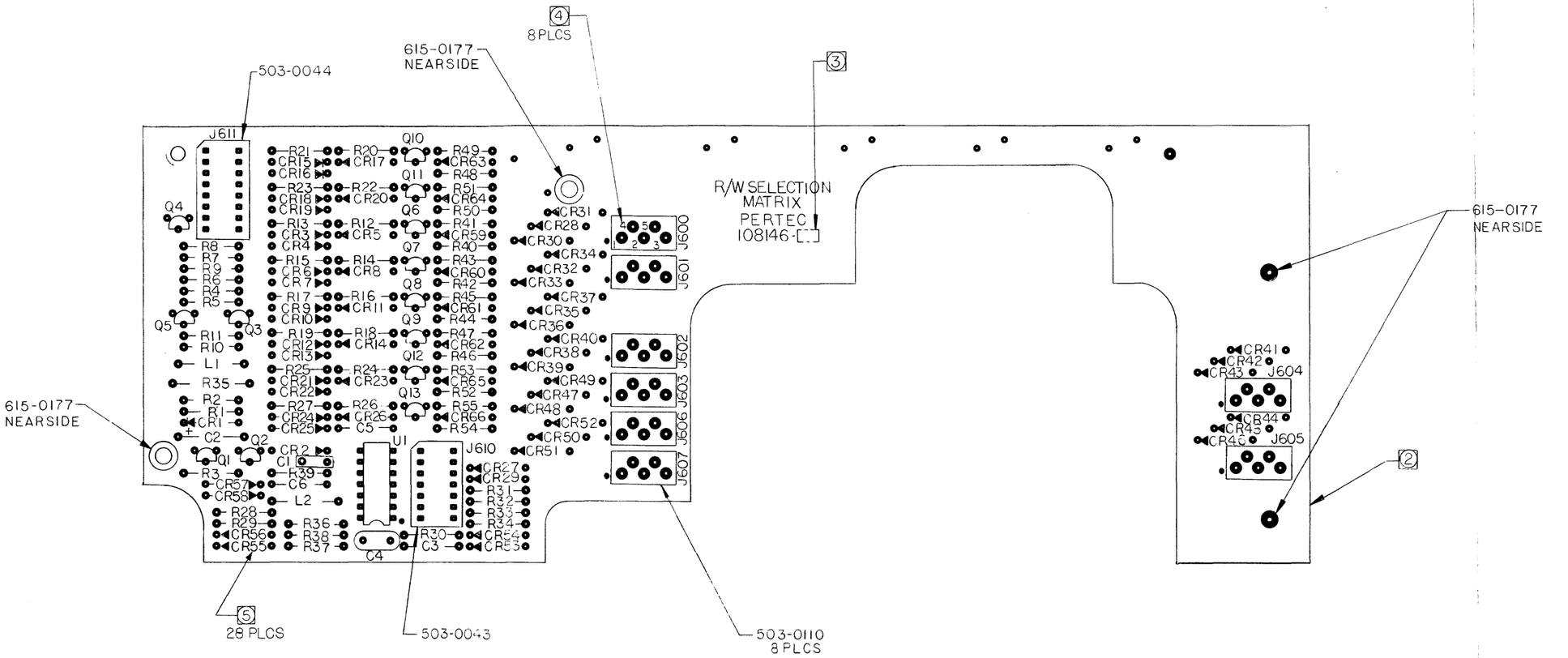
FINISH: | MATL:

SIZE	CODE IDENT NO.	DWG NO.	REV
E		108145	C1
SCALE NONE	DO NOT SCALE DWG	SHEET 1 OF 2	

DWG NO. 108145 REV C1

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-DP PRE PROD. RELEASE	7/1/76	TWM	[illegible]	[illegible]
B	ECN 9650	2/11/77	RJ	[illegible]	[illegible]
C	ECN 9719	3/1/77	SMP	[illegible]	[illegible]
D	ECN 9981	5/4/77	SM	[illegible]	[illegible]
	ERN 9-TS PROD. RELEASE	6/1/77	SM	[illegible]	[illegible]
E	ECN 10419	9/1/77	BK	[illegible]	[illegible]



SCHEMATIC: 108145
REF DWG:

PART NO. 108146-01 REV F

5 ALTERNATE DIODE P/N 300-4446 MAY BE SUBSTITUTED FOR P/N 300-0115 ONLY WITH PRE-WRITTEN ENGINEERING APPROVAL.

4 HEAD CONNECTOR NUMBERING IS SHOWN FOR REF ONLY.

3 MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 108147-01 REV D. AND SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR. TWM	11/1/76
CHK Jim Brown	12/2/76
DES	
ENGR E. Barnwell	11/10/76
PROJ. ENGR	

NEXT ASSY	D3400EXT
APPLICATION	1ST USED ON

FINISH:
MATL: SEE L M[illegible]

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
PCBA
R/W SELECTION MATRIX
AND PREAMP

SIZE	CODE IDENT NO.	DWG NO.	REV
D	32097	108146	E

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1

DWG. NO. 108146 REV. E

PRINTED ON DIETRICH-POST SLEAFPRINT 1120

TABLE I [1]

PART NO.	REFERENCE DESIGNATION
100-1025	R3, 5, 6, 7, 8, 9, 12, 13, 15 THRU 20, 57, 68
100-1035	R54
100-1515	R1
100-1525	R64
100-1545	R62
100-1815	R10, 11
100-1825	R66
100-2715	R55, 63
100-3315	R67
100-3325	R36, 56
100-4715	R50, 61
100-4725	R58, 65
100-5625	R2, 4
100-6805	R40,46
101-1825	R14
101-6805	R59, 60
102-1015	R37
104-5112	R5
104-5113	R52, 53
107-1000	R47
107-1001	R21, 28, 31, 32, 34
107-1960	R43
107-2150	R38, 45
107-3481	R22, 30
107-4221	R23, 29
107-4223	R34
107-4640	R26, 27
107-4642	R24, 33
107-5110	R49
107-6810	R41, 48
107-7500	R39
107-7502	R25
107-9092	R35
121-5010	R42
130-1005	C22
130-1515	C16
130-4705	C26, 29
130-4715	C1, 2
130-7515	C15, 17
131-1020	C27
132-1062	C5, 6
132-2752	C8, 9, 12, 13, 18, 19, 20, 21, 24, 25, 28, 30 THRU 44

TABLE I [1]

PART NO.	REFERENCE DESIGNATION
135-1031	C7, 10, 46 THRU 70
135-4731	C71 THRU 97
135-4742	C4, 11, 23
137-2230	C3
139-2262	C14
200-4125	Q1
300-4002	CR1, 2, 3, 4
300-4446	CR5
330-0475	VR1
400-0307	U169, 209
400-0318	U429
400-2741	U389
402-1003	Y1
700-4112	U143, 207
710-4158	U104, 105 [18]
700-4161	U1, 41, 61, 106, 121, 124, 125, 144, 145, 146, 161, 164, 166, 181, 184, 202, 205, 221, 241, 283
700-4164	U109
700-4393	U285
700-5107	U268, 408
700-5452	U64
700-5453	U362
700-7400	U49, 86, 87, 165, 282, 328, 343, 385, 403
700-7402	U48, 82, 122, 126, 127, 183, 263, 284, 327, 445
700-7404	U51, 81, 85, 123, 162, 185, 186, 222, 224, 227, 303, 348, 363, 365, 407, 423, 444, 448
700-7405	U149, 401, 446, 447, 228
700-7408	U346
700-7410	U107, 404
700-7414	U50, 71, 72, 286
700-7419	U264, 287, 308, 322, 342, 381
700-7430	U442, 306
700-7450	U62, 89, 405
700-7476	U128, 163, 167, 203, 341, 344, 345, 364, 384
700-7486	U422, 441, 443
700-7496	U101, 108, 147, 182, 323
700-7545	U3, 44, 45, 46, 47, 64 THRU 70, 386, 406, 426
710-4112	U83, 129, 242, 243, 267
710-4164	U2, 22, 23, 43
710-4175	U244, 301, 321, 302, 347
710-4393	U305,325
710-7400	U84, 88, 247, 262, 304
710-7402	U63, 187, 324, 383
710-7404	U42, 102
710-7408	U223
710-7410	U261, 266, 361
710-7454	U326
710-7483	U382, 402, 421

TABLE V [5]

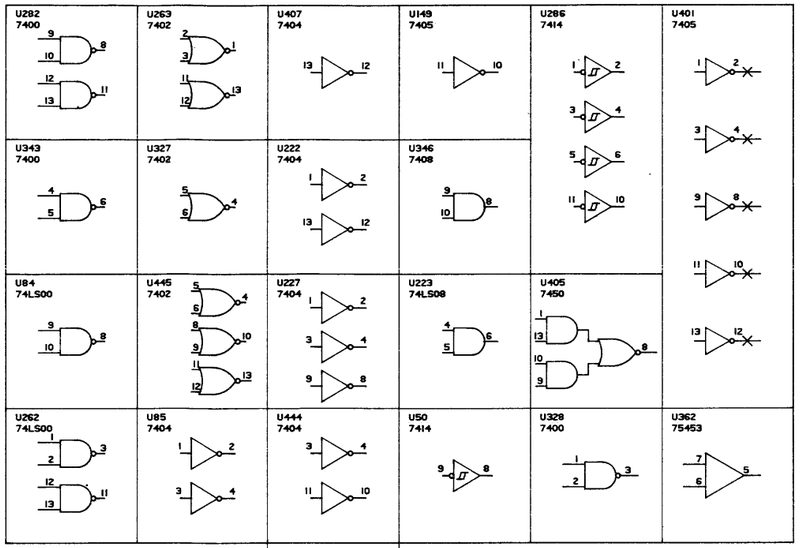


TABLE IV [4]
GND &VOLTAGES

I C TYPE	+5V	GND	-5V	+12V	-12V
LM307				7	4
LM318	7	3	4		
LM741	7		4		
7400	14	7			
7402	14	7			
7404	14	7			
7405	14	7			
7408	14	7			
7410	14	7			
7414	14	7			
7430	14	7			
7450	14	7			
7476	5	13			
7486	14	7			
7496	5	12			
74S05	14	7			
74S112	16	8			
74LS00	14	7			
74LS02	14	7			
74LS04	14	7			
74LS08	14	7			
74LS10	14	7			
74LS54	14	7			
74LS83	5	12			
74LS112	16	8			
74LS164	14	7			
74LS175	16	8			
74LS393	14	7			
74161	16	8			
74193	16	8			
74393	14	7			
75107	14	7			
75451	8	4			
75452	4	8			
75453	14	7			
74LS158	16	8			

REFERENCE DESIGNATIONS

LAST USED	NOT USED	DELETED
C97	C45	
CR5		
J127		
Q1		
R68		
TP30		
U448	13	
VR1		
Y1		
W26		

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-MR PRE PROD RELEASE	4/4/77	TKM	TH	JF
B	ECN 10110 ERN 9-TP PRODUCTION RELEASE	12 Apr 77	SOL		
C	ECN 10330	7/6/77	CJ		
D	ECN 10546	9/8/77	SOL		
E	ECN 10545	9/19/77	RS		
F	ECN 10681	10/31/77	KSR		
G	ECN 10934	11/28/77	KSR		
H	ECN 11034	1/3/78	KSR		
J	ECN 11126	2/10/78	KSR		
J1	ECN. 11143	2/17/78	KSR		
K	ECN 11161	3/6/78	KSR		
K1	ECN 11421	5/19/78	KSR		
K2	ECN 11511	5/24/78	HM		
K3	ECN 11951	7/9/78	HM		
K4	ECN 12335	9/27/78	HM		
L	ECN 12948	11/20/78	MP		
L1	ECN 13156	3/6/79	MP		

[18] APPROVED ALTERNATE PART IS 700-4158 (74158) WHEN SUBSTITUTED AS A GROUP; i.e.USE ALL 710-4158 (74LS158) OR ALL 700-4158(74158). DO NOT INTERMIX ON SAME PCBA.

[17] SEE TABLE VI (DIGIT 1) - I/O = QUAD; UNIT = SPLIT QUAD (DUAL UNIT EMULATE)

[16] J126 IS NOT REQUIRED WHEN MECHANICAL SECTORING IS USED.

15. J128 IS USED FOR TEST PURPOSES ONLY.

[14] FOR 1001 OPTION (SOFT SECTORED FORMAT), CONFIGURATION IS AS SHOWN FOR 1016.

[13] THE FOLLOWING REFERENCE DESIGNATIONS ARE NOT USED: U4 THRU 21, U24 THRU 40, U52 THRU 60, U73 THRU 80, U90 THRU 100, U103, U110 THRU 120, U121, U130 THRU 142, U148, U150 THRU 160, U168, U170 THRU 180, U188 THRU 201, U204, U206, U208, U210 THRU 220, U225, U226, U229 THRU 240, U245, U246, U248 THRU 260, U265, U269 THRU 281, U288 THRU 300, U307, U309 THRU 320, U329 THRU 340, U349 THRU 360, U366 THRU 380, U387, U388, U390 THRU 400, U409, U410 THRU 420, U424, U425, U427, U428, U430 THRU 440, U449 &U450.

[12] FOR LOCATION OF OPTION JUMPERS REFER TO TABLES XI, VII AND VIII.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

10. DIODES ARE IN4002.

9. PNP TRANSISTORS ARE 2N4125.

8. (RESERVED)

7. CAPACITOR VALUES ARE IN MICROFARADS, 10%, 100V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 W. ALL 1% ARE 1/8 W.

[5] FOR SPARE LOGIC ELEMENTS SEE TABLE V.

[4] FOR I.C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS. SEE TABLE IV.

3. (RESERVED)

2. (RESERVED)

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS:
ASSEMBLY DWG 108166
SPECIFICATION 108169
JUMPER OPTION LOCATOR 108234

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± ANGULAR ± 1/2°
.XXX ±
REMOVE ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR.	4/4/77
CHK.	4/4/77
DES.	
ENGR.	
PROJ. ENGR.	
MATL	
FINISH:	

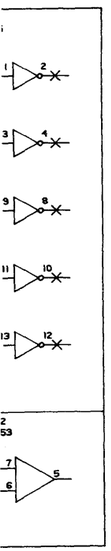
NEXT ASSY | APPLICATION | USED ON

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
SCHEMATIC, D3000 EXTENSION LOGIC BOARD

SIZE D | CODE IDENT NO. | DWG. NO. 108165 | REV L1
SCALE NONE | DO NOT SCALE DWG. | SHEET 1 OF 12

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-MR PRE PROD RELEASE	4/24/77	TGM	PL	JF
B	ECN 10140 ERN 9-TP PRODUCTION RELEASE	5/20/77	SDL	PL	JF
C	ECN 10330	6/8/77	CJ	[illegible]	[illegible]
D	ECN 10546	7/14/77	SDL	[illegible]	[illegible]
E	ECN 10565	7/19/77	JLS	[illegible]	[illegible]
F	ECN 10685	8/8/77	JSB	[illegible]	[illegible]
G	ECN 2nd [illegible]	8/24/77	JSB	[illegible]	[illegible]
H	ECN 11034	9/7/77	[illegible]	[illegible]	[illegible]
J	ECN 11126	9/28/77	JSB	[illegible]	[illegible]
J1	ECN 11143	10/7/77	JSB	[illegible]	[illegible]
K	ECN 11161	10/14/77	SDL	[illegible]	[illegible]
L	ECN 11421	11/15/77	JSB	[illegible]	[illegible]
K2	ECN 11511	12/14/77	MM	[illegible]	[illegible]
K3	ECN 11951	1/30/78	MM	[illegible]	[illegible]
K4	ECN 12335	4/11/78	MM	[illegible]	[illegible]
L	ECN 12948	8/24/78	MP	[illegible]	[illegible]
L1	ECN 13156	10/24/78	MP	[illegible]	[illegible]



[18] APPROVED ALTERNATE PART IS 700-4158 (74158) WHEN SUBSTITUTED AS A GROUP; i.e. USE ALL 710-4158 (74LS158) OR ALL 700-4158(74158). DO NOT INTERMIX ON SAME PCBA.

[17] SEE TABLE XI (DIGIT 1) - I/O = QUAD; UNIT = SPLIT QUAD (DUAL UNIT EMULATE)

[16] J126 IS NOT REQUIRED WHEN MECHANICAL SECTORING IS USED.

15. J128 IS USED FOR TEST PURPOSES ONLY.

[14] FOR 1001 OPTION (SOFT SECTORED FORMAT), CONFIGURATION IS AS SHOWN FOR 1016.

[13] THE FOLLOWING REFERENCE DESIGNATIONS ARE NOT USED: U4 THRU 21, U24 THRU 40, U52 THRU 60, U73 THRU 80, U90 THRU 100, U103, U110 THRU 120, U121, U130 THRU 142, U148, U150 THRU 160, U168, U170 THRU 180, U188 THRU 201, U204, U206, U208, U210 THRU 220, U225, U226, U229 THRU 240, U245, U246, U248 THRU 260, U265, U269 THRU 281, U288 THRU 300, U307, U309 THRU 320, U329 THRU 340, U349 THRU 360, U366 THRU 380, U387, U388, U390 THRU 400, U409, U410 THRU 420, U424, U425, U427, U428, U430 THRU 440, U449 &U450.

[12] FOR LOCATION OF OPTION JUMPERS REFER TO TABLES VI, VII AND VIII.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

10. DIODES ARE IN4002.

9. PNP TRANSISTORS ARE 2N4125.

8. (RESERVED)

7. CAPACITOR VALUES ARE IN MICROFARADS, 10%, 100V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 W. ALL 1% ARE 1/8 W.

[5] FOR SPARE LOGIC ELEMENTS SEE TABLE V.

[4] FOR I.C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS. SEE TABLE IV.

3. (RESERVED)

2. (RESERVED)

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE 1.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS:
ASSEMBLY DWG 108166
SPECIFICATION 108169
JUMPER OPTION LOCATOR 108234

TABLE VI [12]
PERTEC CONFIGURATION DIGIT 1

	I/O	UNIT	1&2	3&4	YES	NO	W2	W3	W6	W10	W11	W12	W13	W14	W15	W18	W20	W22	W23	W24	W25	W26
A	X					X		X			X			X		X	X	X			X	X	X
B		X	X			X		X				X		X	X	X	X				X	X	X
C		X		X		X		X			X		X		X		X	X		X	X	X	X
D	X				X			X	X		X			X		X	X	X			X		
E		X	X		X			X	X			X		X	X		X	X	X		X		
F		X		X	X			X	X		X		X		X		X	X		X		X	X
H																							
I																							
J																							
K																							
L																							
M																							
N		X	X	X		X		X				X	X		X		X	X	X	X	X	X	X
P		X	X	X	X				X	X			X	X		X		X	X	X	X		
Q																							
R																							

TABLE VII [12]
PERTEC CONFIGURATION DIGIT 2

	YES	NO	NONE	SAFE	RUN	YES	NO	W1	W7	W8	W9	W16	W17
A	X		X				X					X	
B		X	X				X						X
C	X			X			X	X		X		X	
D		X		X			X	X		X			X
E	X				X		X	X			X	X	
F		X			X		X	X			X		X
H	X		X			X			X			X	
I		X	X			X			X				X
J	X			X		X		X	X	X		X	
K		X		X		X		X	X	X			X
L	X				X	X		X	X		X	X	
M		X			X	X		X	X		X		X

TABLE VIII [12]
PERTEC CONFIGURATION DIGIT 3

	YES	NO	W4	W5
A		X		X
B	X		X	

INPUT/OUTPUT INTERFACE CONFIGURATION OPTIONS
NO. OF SECTORS

D3XXX-XXXX-XXX-XXXAAX

- SECTOR CONFIGURATION
- 1=1500 RPM, 2=2400 RPM
- 5=5440 DUAL, 6=5440 QUAD, 7=2315 DUAL, 8=2315 QUAD
- 4=2200 BPI 200 TPI, 6=4400 BPI 200 TPI
- DIGIT 6
- DIGIT 5
- DIGIT 4
- DIGIT 3
- DIGIT 2
- DIGIT 1

PROGRAMMING ARRAY INSTALLATION [16]

J121 TIME DEMULTIPLEXER & SPEED OPTION				J122 SPEED COUNT		J123 SECTOR PLL		J125 SECTORING SELECTION					J126 (UPPER PLATTER) J127 (LOWER PLATTER)	
SECTOR CONFIG.	RPM	SECTORS	USE ARRAY NO.	RPM	USE ARRAY NO.	RPM	USE ARRAY NO.	SECTORS [14]	CONFIGURATION [17]	SECTOR CONFIGURATION		USE ARRAY NO.	SECTOR	USE ARRAY NO.
MECHANICAL	1500	≤32	103611-01	1500	103612-01	1500	103613-01					108195-01	8	103616-01
	1500	>32 ≤48	-02	2400	103612-02	2400	103613-02					-02	10	-03
	1500	>48 ≤64	-03									-03	12	-04
	2400	≤24	-04									-04	14	-05
	2400	>24≤32	-05									-05	16	-06
	2400	>32 ≤48	-06									-06	18	-07
	2400	>48 ≤64	103611-07					6 OR 8	SPLIT QUAD		MECHANICAL	-07	20	-08
ELECTRONIC OR INDEX	1500	——	103611-01					6 OR 8	SPLIT QUAD	INDEX ONLY	ELECTRONIC	-08	24	-09
	2400	——	103611-04					6 OR 8	SPLIT QUAD	MULTI-NOTCH	ELECTRONIC	-09	28	-10
								≥10	SPLIT QUAD		MECHANICAL	-10	30	-11
								≥10	SPLIT QUAD	INDEX ONLY	ELECTRONIC	-11	32	-12
								≥10	SPLIT QUAD	MULTI-NOTCH	ELECTRONIC	-12	36	-13
								6 OR 8	QUAD		MECHANICAL	-13	40	-14
								6 OR 8	QUAD	INDEX ONLY	ELECTRONIC	-14	42	-15
								6 OR 8	QUAD	MULTI-NOTCH	ELECTRONIC	-15	48	-16
								≥10	QUAD		MECHANICAL	-16	56	-17
								≥10	QUAD	INDEX ONLY	ELECTRONIC	-17	60	-18
								≥10	QUAD	MULTI-NOTCH	ELECTRONIC	108195-18	64	103616-19

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± ANGULAR
.XXX ± ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010
FINISH:
MATL:

SIGNATURES	DATE
DR. [illegible]	4/24/77
CHK. [illegible]	5/20/77
ENG.	
PROJ. ENGR.	

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
SCHEMATIC,
D3000 EXTENSION
LOGIC BOARD

SIZE	CODE IDENT NO.	DWG. NO.	REV
D		108165	L1

SCALE NONE DO NOT SCALE DWG. SHEET 1 OF 12

SIZE	CODE IDENT NO.	DWG. NO.	REV
D		108165	L1

SCALE NONE DO NOT SCALE DWG. SHEET 2 OF 12

SPEED COUNT RESET
LSCZ0 4-1E
LOAD · PURGE
LNLP0 4-2F 3-6E
LLPX0 4-2F 3-6E
LLNP0 4-2E 3-6E
LRSC0 4-2F 3-6E
LC2IF 6-2B
·2 SEC
U325 74LS393
DELAY COUNTER DECODER
U326 74LS54
U365 7404
U346 7408
LLOL3 6-2A
U345 7476
LSTPF 3-6D
TP21
NLSTPF 4-8E
NLC0U0 4-7G
SEQUENCE TIMING PULSE
J103
SPSCA
U447 7405
LEUF0
NLC0S0 4-6F
J105
U446 7405
LEUE0
EMERGENCY UNLOAD F/F
LPCX0 4-5G
U284 7402
U363 7404
NLRFFF 4-5G
U304 74LS00
U345 7476
LEUFF 5-4D
NLPCFF 4-4H
NLEUFF 4-5A
U303 7404
LLOL2 4-4E
J105
J128-12
SPSCA
POWER CLEAR
U286 7414
R1 150
U303 7404
NLPCX0 4-8D
DISK ROTATION DETECTOR COUNTER
U283 74161
LC20F 6-1C
NLDRX0 4-5A
U284 7402
LLDP0 11-5D
U303 7404
NLPMX0 5-5E
U266 74LS10
J128-3
J128-5
LLPX0 4-2F
LNLP0 4-2F
LSOTF 7-2F
LSTPF 3-3H
J128-2
POSITION TRANSDUCER FAILURE
J128-14
SPTF0
U327 7402
J128-13
J103
RWEC0
NLEOF0
READY LOGIC
U365 7404
NLESD0 4-4B
U407 7404
U406 75451
J111
NLRLDT (READY LAMP)
NLRXX0 5-5F
LRXX0 9-6E
+5V
R2 5.6K
J101
J102
U50 7414
U50 7414
U149 7405
U286 7414
J128-4
U306 7430
J128-16
LAEX0
IAEUR
ISSDR
C1 470PF 5% 500V
POSITION LIMIT ERROR
J128-15
NLPLE0 9-5B
U385 7400
U365 7404
NLSARG 5-7F
LSARG 5-5C
EMERGENCY UNLOAD LOGIC
W17
W16
U447 7405
R4 5.6K
C2 470PF 5% 500V
U448 7404
LDRC0 5-4E
TESTER POWER
R3 1K
W7
U49 7400
LSXX0 6-4G
DISK SPEED ERROR
J128-6
NLDSE0 7-2G
J128-1
NLSTE0 9-6C
J128-7
J128-8
U85 7404
U362 75453
J128-9
J128-10
U444 7404
U401 7405
NLRSSS 4-8C
GND
+5V

SIZE	CODE IDENT NO.	DWG NO	REV
		108165	L
SCALE NONE	DO NOT SCALE DWG	SHEET 2 OF 12	

CARTRIDGE INSERTED LATCH

+5V

R5 1K

R6 1K

J109

NCCSIS 2

CCSIS 3

U447 7405

LCCIG

U346 7408

NLCOUG 3-8G

U363 7404

RUN F/F U364 7476

END OF RUN F/F U364 7476

LRFFF

LRERG 4-3D
LPCXG 3-6F

U284 7402

PURGE CYCLE F/F U344 7476

LPCFF 7-8E

NLPCFF 3-3F 7-8E

LOAD HEADS F/F U344 7476

LLHFF 9-3E

NLLHFF 9-4D

NLRFFF 5-4B 3-4F

NLWDEG 5-5E

U304 74LS00

SEQUENCE CONTROL LOGIC

U324 74LS02

U303 7404

NLLPNG 9-6A

LNLPG 3-8H

LLPXG 3-8H

LLNPG 3-8G

U363 7404

U304 74LS00

LSCZG 3-8H

NLCSFF

LC09F 6-3C

U365 7404

NLC09G 3-8F 9-3C

SHRXG 8-7B

U304 74LS00

U363 7404

SEQUENCE CONTROL F/F

U383 74LS02

U384 7476

LL0L2 6-4B

BRAKE CYCLE ENABLE F/F

U384 7476

J105

U445 7402

NLBCEG

NLSTPF 3-3B

NLPCXG 3-6E

NLDRXG 3-2E

DISK ROTATING

U383 74LS02

LLCMG 5-4B

LRERG 4-5G

FUNCTION CONTROL LOGIC

U385 7400

U365 7404

U404 7410

NLBCFF

U363 7404

LLCMG

NLLCMG

J111

U406 75451

NLSLDT

U386 75451

NLRXDG

NLSNHG

NLHRXG 3-2E

HEAD RETRACTED

U385 7400

LOMEG 7-7C

U404 7410

LRSCG 3-8G

NLRSSS (3-5A)

J105 NLRSSS 19

J110 NCRSSS 2

CRSSS 3

+5V

R7 1K

R8 1K

U447 7405

U328 7400

U347 74LS175

U266 74LS10

NLSDMG 7-3G

U346 7408

LRPXG

LC09F 6-3C

NLPCXG 3-6E 3-8D

START/STOP PULSE REGISTER

U404 7410

LLHFF 4-3H 9-3E

NLEUFF 3-2E

ENABLE SELECTED DRIVE

NLESDG 3-4D

U365 7404

LESDG 7-2G

U386 75451

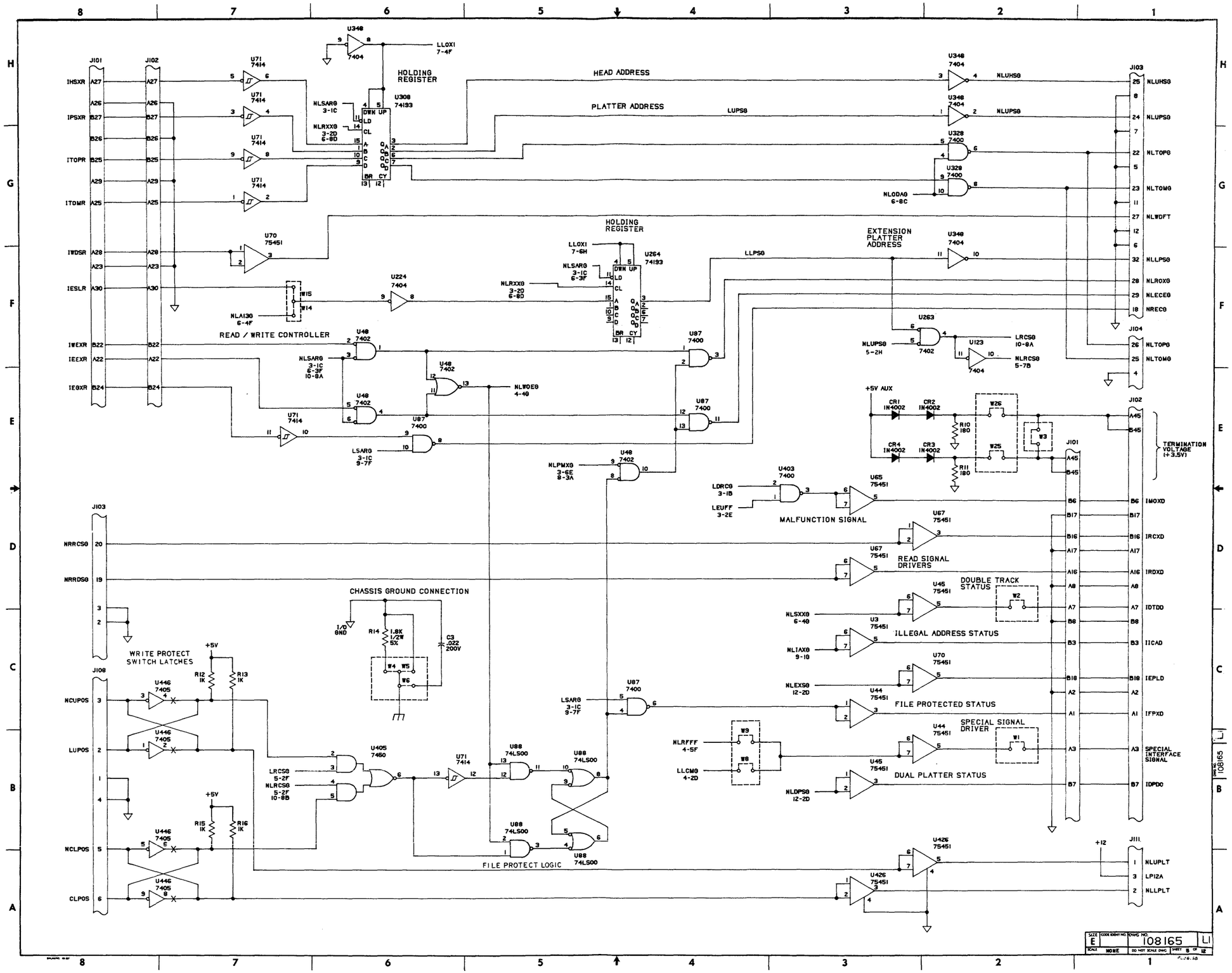
+5V

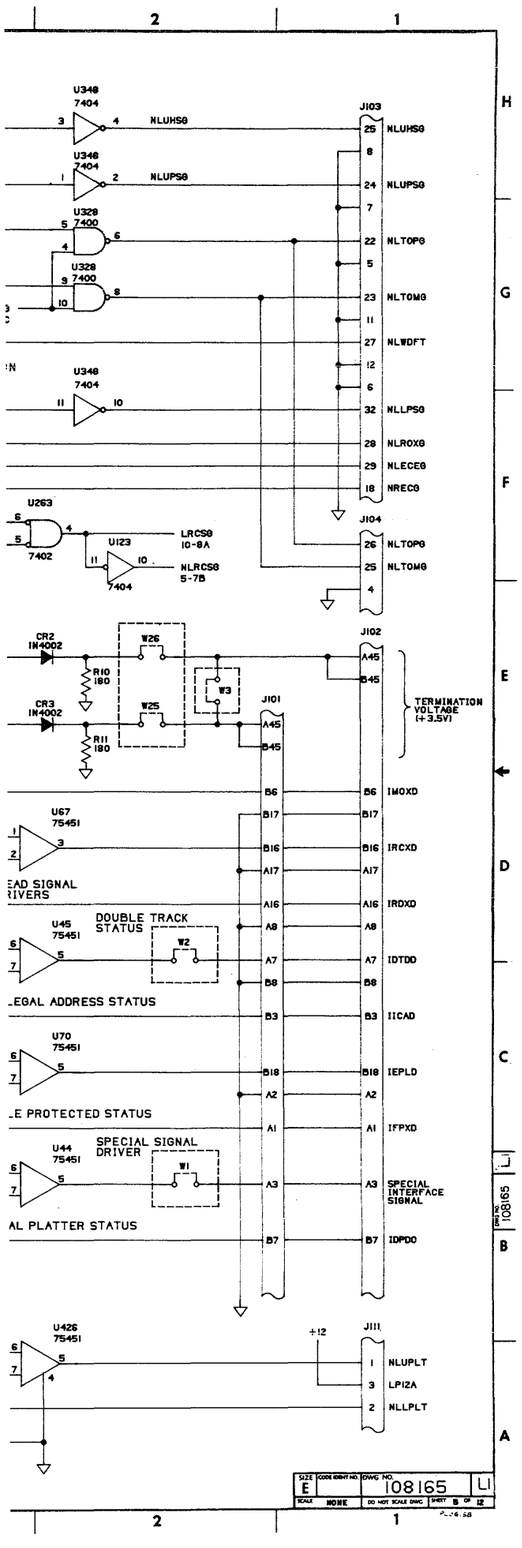
R9 1K

NLRLDT

SIZE	CODE IDENT NO	DWG NO	REV
E		108165	LJ
SCALE NONE		DO NOT SCALE DWG	SHEET 4 OF 12

108165 LJ


HOLDING REGISTER
HEAD ADDRESS
PLATTER ADDRESS
LUPS0
NLUHS0
NLUPS0
NLODA0
6-8C
NLTOP0
NLTOM0
NLWDFT
NLLPS0
NLROXG
NLECE0
NRREC0
EXTENSION PLATTER ADDRESS
LLPS0
LLOXI 7-6H
NLSAR0 3-1C 6-3F
NLRXX0 3-2D 6-8D
NLAI3G 6-4F
READ / WRITE CONTROLLER
NLWDE0 4-4G
LSAR0 3-1C 9-7F
NLPMX0 3-6E 8-3A
LRCS0 10-8A
NLRCS0 5-7B
NLUPS0 5-2H
LLOXI 7-4F
LDRC0 3-1B
LEUFF 3-2E
MALFUNCTION SIGNAL
+5V AUX
TERMINATION VOLTAGE (+3.5V)
NRRCS0
NRRDS0
READ SIGNAL DRIVERS
CHASSIS GROUND CONNECTION
I/O GND
R14 1.8K 1/2W 5%
C3 .022 200V
DOUBLE TRACK STATUS
NLSXX0 6-4G
ILLEGAL ADDRESS STATUS
NLIAX0 9-1G
NLEXS0 12-2D
FILE PROTECTED STATUS
SPECIAL SIGNAL DRIVER
NLRFFF 4-5F
LLCM0 4-2D
DUAL PLATTER STATUS
NLDPS0 12-2D
WRITE PROTECT SWITCH LATCHES
NCUPOS
LUPOS
NCLPOS
CLPOS
LRCS0 5-2F
NLRCS0 5-2F 10-8B
LSAR0 3-1C 9-7F
FILE PROTECT LOGIC
+12
NLUPLT
LPI2A
NLLPLT
IMOXD
IRCXD
IRDXD
IDTDO
IICAD
IEPLD
IFPXD
SPECIAL INTERFACE SIGNAL
IDPDO
SIZE E
CODE IDENT NO.
DWG NO. 108165
SCALE NONE
DO NOT SCALE DWG.
SHEET 5 OF 12
REV LI
108165 B


U348 7404
NLUHS0
NLUPS0
U328 7400
NLTOP0
NLTOM0
NLWDFT
U346 7404
NLLPS0
NLROX0
NLECE0
NREC0
J103
J104
U263 7402
U123 7404
LRCS0 10-8A
NLRCS0 5-7B
CR2 IN4002
CR3 IN4002
R10 180
R11 180
W26
W25
W3
J102
J101
TERMINATION VOLTAGE (+3.5V)
IMOXD
IRCXD
IRDXD
IDTDD
IICAD
IEPLD
IFPXD
SPECIAL INTERFACE SIGNAL
IDPDD
U67 75451
EAD SIGNAL RIVERS
DOUBLE TRACK STATUS
W2
U45 75451
EGAL ADDRESS STATUS
U70 75451
E PROTECTED STATUS
SPECIAL SIGNAL DRIVER
W1
U44 75451
AL PLATTER STATUS
U426 75451
+12
J111
NLUPLT
LPI2A
NLLPLT
J101
J102
IUS1R
IUS2R
IUS3R
IUS4R
U51 7404
U89 7450
UNIT SELECT LOGIC
U49 7400
U126 7402
LSXX0 3-7E 4-4C
NLSXX0 5-3C
W11
W10
W12
W13
NLAI3G 5-7F
+5V
R17 1K
R18 1K
R19 1K
R20 1K
J110
NCUS1S
NCUS2S
NCUS3S
NCUS4S
W22
W23
U448 7404
U86 7400
NLBSX0 9-3E
NLRXX0 5-6B
J103
NLDISG
NLDIDG
U327 7402
U348 7404
NLBRG 10-2B
NLODA8 5-3B
LBTFF 9-4F
CLOCK OSCILLATOR
Y1 X1115A
U186 7404
TP14
U205 74161
LC04F 7-8B
LLOL3 3-3H
READY DRIVER
BUSY SEEKING
NLSARG 5-6E 10-8A
U3 75451
U69 75451
U68 75451
IRXX0
IBS10
IBS20
IBS30
IBS40
CLOCK COUNTDOWN
U285 74393
U305 74LS393
LC08F 11-4C
LC09F 4-8F 4-7B 11-4F
LC10F 11-4F
LC13F 9-3B
LC17F 9-7C
LC20F 3-3D
U224 7404
LLOL2 4-4E
U267 74LS112
LC21F 3-8B
LC01F 9-7H
LC02F 7-8B
LC03F 8-2C
U444 7404
J105
29

SPEED CONTROL PROGRAMMING

PART OF J121

LC02F 6-5A

LC03F 8-7D

LC04F 6-5B 10-8B

U224 7404

U224 7404

SPEED CONTROL COUNTER

U223 74LS08

U223 74LS08

U202 74161

U221 74161

U241 74161

U222 7404

U222 7404

LPCFF 4-4H

NLPCFF 4-4G

DISK SPEED COUNT PROGRAMMING J122

U244 74LS175

NLSCRG (SPEED COUNT RESET)

U165 7400

SPEED SEQUENCE REGISTER

LTSCG (TRANSFER SPEED COUNT)

U223 74LS08

LPLFF 10-7H

J106

TP30

+5V

GND

TP17

-5V

-5V SENSE

+12V

-12V

LDMEG 4-3B 11-7C

C28, 32 THRU 44 2.7 35V

+5V DISTRIBUTION BUS

TP2, 15, 28, 29

GROUND BUS

C46 THRU C70 .01 10%, 100V

C71 THRU C97 .047 20%, 50V

+5V

+12V

-12V

C4 0.47 20%

J105

S12SS

J104

+25V UNREG

POWER DISTRIBUTION AND FEED THRU

SPEED HIGH LIMIT F/F

U143 74S112

DISK SPEED LOW F/F

U242 74LS112

SPEED LOW LIMIT F/F

U242 74LS112

LLOXI 5-5F

U262 74LS00

INCREASE MOTOR SPEED F/F

NLSDMG 4-5C

U243 74LS112

U303 7404

TP22

J105

NL1MSI

LESDG 4-2A

U262 74LS00

NLDSEG 3-6B

U243 74LS112

LSOTF 3-6D

SPEED OUT OF TOLERANCE F/F

U224 7404

J107

+5V

GND

-5V

+12V

-12V

S12SS

+25V UNREG

J105

LPSVA

J101

J102

ICDER A33 B33

ICD7R B34 A34

ICD6R A34 B34

ICD5R B36 A36

B35 A35

ICD4R A36 B36

A35 B35

ICD3R B37 A37

B38 A38

ICD2R A37 B37

A38 B38

ICD1R B39 A39

ICD0R A39 B39

U50 7414

U72 7414

U72 7414

U72 7414

U72 7414

U72 7414

U72 7414

U51 7404

U72 7414

U51 7404

NLLAXG 9-2H

U303 7404

LDACG 9-2D

POSITION REFERENCE CLOCK

POSITION TRANSDUCER INDEX

POSITION QUADRATURE CLOCK

HEADS RETRACTED

J105

SPRCG 26

SPTIG 25

SPQCG 27

SHRXG 28

SPTIG 8-9B

SHRXG 4-8E 9-8A

SPQCG 9-3D

LC03F 7-8G

NLAD7G 8-2H

NLAD6G 8-2G

NLAD5G 8-2G

NLAD4G 8-2G

NLAD3G 8-2G

NLAD2G 8-2F

NLAD1G

NLAD0G 8-2F

REV LJ

DWG NO 108165

SIZE	CODE IDENT NO	DWG NO	REV
E		108165	LJ
SCALE NONE	DO NOT SCALE DWG	SHEET 7 OF 12	

LOAD ADDRESS LOGIC AND BUSY LOGIC

LC01F 6-5A
LAVC0 8-5D
U127 7402
U107 7410
NLLAX0 8-8E
LSAR0 5-6E
NLIAX0 5-3C
J101
J102
ICASR B33
A32
B32
IRICR A31
U50 7414
TP6
U108 7496
HOLD BUSY TIME F-F
U128 7476
LL0X5 8-2C
U49 7400
U167 7476
ILLEGAL ADDRESS F/F
HOLD DELAY SHIFT REGISTER
BUSY TIME F-F
LBTFF 6-7C
TP10
U147 7496
NLB5X0 6-8D
LRXX0 3-3C
NLBTFF
STROBE SHIFT REGISTER
LPMX0 8-2B
LC13F 6-2C
U109 74164
LLHFF 4-5B
U186 7404
FORWARD SLOW MODE F-F
NLLHFF 4-3B
U187 74LS02
SPQC0 8-7B
U165 7400
LDAC0 8-8E
U423 7404
TP23
NLFSMI
LAPX0
U49 7400
U207 74S112
TP24
NLRSMI
NLC096 4-6F
REVERSE SLOW MODE F-F
SEEK TIME ERROR CHECK COUNTER
U267 74193
LC17F 6-1C
NLSTE0 3-6B
LROFF
U247 74LS00
POSITION LIMIT MONITOR F-F
U227 7404
LL0X5 8-2D
SPTI0 8-7C
NLPLE0 3-6B
NLLPN0 4-2F
U267 74LS112
SHRX0 8-7B
ERROR CHECK LOGIC
NLHRX0 4-5B
NLROFF
RESTORE OPERATION F-F

SIZE E | CODE IDENT NO. | DWG NO. 108165 | REV L
SCALE | DO NOT SCALE DWG | SHEET 9 OF 12

108165 | L | 11

PHASE LOCK LOOP

PHASE COMPARATOR AND FILTER

SUM AND DIFFERENCE AMPLIFIER

SECTOR PHASE LOCK LOOP

SECTOR VOLTAGE CONTROL OSCILLATOR

SECTOR COUNTDOWN DIVIDER

SECTOR PLL COUNTDOWN COUNTER

LLOXX

SECTOR PULSE MULTIPLEXER

UPPER SECTOR PULSE FORMER

LOWER SECTOR PULSE FORMER

UPPER INDEX PULSE FORMER

LOWER INDEX PULSE FORMER

INDEX PULSE MULTIPLEXER

MULTIPLEXER CONTROL LOGIC

ILLEGAL ADDRESS F/F

FORWARD SLOW MODE F-F

REVERSE SLOW MODE F-F

TORE ATION -F

LSAR0 5-6E

NLIAX0 5-3C

LLOX5 8-2C 9-5D

LLOL6 11-4D

LVSC0 11-2C

LPLFF 7-8D

LLOL6 11-4D

LSCKF

LLSCK 12-2F

LUSCK 11-1E 12-7D

LLICK 11-1C 12-8B

LU1CK 11-1E 12-8B

LC04F 7-8B

NLRCS0 5-2F

LRCS0 5-2F

NLSAR0 6-3F 12-3A

LLWE0 12-3D

LVCO0 11-4B

NLBR0 6-7C

NLISM0

NLFSM1

NLRSM1

LDAC0 8-8E

ISPXD

IIPXD

SIZE	CODE IDENT NO.	DWG. NO.	REV
E		108165	L1
SCALE	NONE	DO NOT SCALE DWG.	SHEET 10 OF 12

UPPER TIME DEMULTIPLEXER CIRCUITRY

UPPER SENSOR DETECTOR

LOWER SENSOR DETECTOR

UPPER DEMUX CONTROL F/F

UPPER DEMUX GATE F/F

UPPER DEMUX COUNTER

LOWER TIME DEMULTIPLEXER CIRCUITRY

SECTOR SELECTION PROGRAMMING

DEMUX SECTOR OR INDEX ONLY

DEMUX INDEX

ELECTRONIC SECTOR

LOWER DEMUX CONTROL F-F

LOWER DEMUX GATE F-F

LOWER DEMUX COUNTER

VCO DIVIDER

UPPER SYNCHRONIZER REGISTER

LOWER SYNCHRONIZATION REGISTER

UPPER COUNT CONTROL F-F

LOWER COUNT CONTROL F-F

SIZE	CODE IDENT NO	DWG NO	REV
E		108165	L1
SCALE	NONE	DO NOT SCALE DWG	SHEET 11 OF 18

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
—	A ERN 9-MR; B ECN 10110 & ERN 9-TP; C ECN 10330	—	—	—	—
D	ECN 10565	7/24/79	RAS	AEK	GL
E	ECN 11034	7/24/79	RAS	AEK	GL
F	ECN 11126	2-3-80	RAS	AEK	GL
G	ECN 11196	5/5/80	RAS	AEK	GL
H	ECN 11161	5/30/80	SDL	AEK	GL
J	ECN 11837	7/22/80	SDL	AEK	GL
J1	ECN 11951	9/4/80	HM	AEK	GL
K	ECN 12948	3/3/81	MP	AEK	GL
L	ECN 14165	12/16/81	SDL	AEK	GL
M	ECN 14446	7/30/82	SDL	AEK	GL

615-6822
2 REQD

108108-01

600-2606
605-0600

108271-01

108108-02

1 REQD
2 PLCS
102709-02
605-0800
606-0800
600-0805

108112-03

615-0135
2 REQD
2 PLCS

DENOTES PIN NO. 1

503-0278

503-2560(-01)
503-2562(-02)
21 PLCS

503-2561(-01)
503-2563(-02)
48 PLCS

108108-04
2 PLCS

102681-01
2 PLCS

600-0405
606-0400
604-2400

503-0101
2 REQD

108108-02
6 PLCS

108112-04
2 PLCS

600-0405
606-0400
604-2400

103593-01

600-2606
604-2600

669-0118

108112-02

600-0405
604-2400

503-7545

615-0125

102697-01

600-0805
604-2800

102747-01

503-3431

SCHEMATIC: 108165 REV
REF DWGS:

PART NO. 108166-01 REV M

5 FOR USE AND LOCATION OF PROGRAMMING JUMPERS (503-0138) SEE JUMPER OPTION LOCATOR DWG 108234 REF.

4 KEY CONNECTOR BY REMOVING DESIGNATED PIN.

3 MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 108167-01 REV E AND SUBSEQUENT.

1. ASSEMBLE USING STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

503-0138 5

SECTION A-A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± .02
XXX ± .010
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX .015

SIGNATURES	DATE
DR. CADDS	7/31/79
CHK.	
DES.	
ENGR.	
PROJ. ENGR.	

PERTEC
a division of Pertec Computer Corporation

TITLE
PCBA
PERTEC LOGIC

NEXT ASSY IF USED ON	FINISH:	MATL:	SIZE	CODE IDENT NO.	DWG NO.	REV
D3000 EXT		SEE L/M	E	32097	108166	M
APPLICATION			SCALE 2:1	DO NOT SCALE DWG.	SHEET 1 OF 1	

CADDS

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APP
A	ERN 9-7A PRE PROD RELEASE	8/17	TOM	[illegible]	[illegible]
B	ECN 10104	9/17	[illegible]	[illegible]	[illegible]
	ERN 9-7U PROD. RELEASE	9/17	[illegible]	[illegible]	[illegible]
C	ECN 10901	11/18	[illegible]	[illegible]	[illegible]
D	ECN 11584	[illegible]	[illegible]	[illegible]	[illegible]
E	ECN 13451	9/20	[illegible]	[illegible]	[illegible]

TABLE I [1]

PART NO.	REFERENCE DESIGNATION
100-1015	R60
100-1025	R17,33,36,37,39,41,45,46,47,48,50,57
100-1035	R54
100-3335	R35
100-4725	R21,23,25,27,38,49,51
100-5615	R44
100-6815	R34
100-1006	R61
101-3915	R58
104-2870	R5
104-3480	R4
107-1001	R3,8,9
107-1002	R15,16,22,29,30,55
107-1003	R31,32
107-1212	R42,53
107-1471	R2
107-1473	R26
107-1620	R13,56
107-1961	R40
107-2613	R6
107-3161	R7,10,43
107-3163	R28
107-3832	R12,19
107-4222	R14,20
107-6812	R24
107-9093	R52
107-8252	R11,18
109-0003	R59
130-2215	C3,5,6
131-1020	C2
131-1030	C8
134-3360	C10

TABLE I (CONTINUED) [1]

PART NO.	REFERENCE DESIGNATION
135-4731	C20
139-1045	C4
139-2244	C1,9 11 THRU 19
139-8202	C7
200-1420	Q2
200-1470	Q3
200-4123	Q1
200-4125	Q4
300-4002	CR2
300-4446	CR1,3,4
331-0395	VR5
330-0515	VR3,4
331-0275	VR1,2
400-0307	U1,2,3
400-0555	U8
400-2741	U16
400-5558	U4,7
403-0002	U6
700-7400	U12
700-7404	U14
700-7405	U5,11
700-8020	U13
710-7402	U9,15
710-7493	U10

TABLE II [2]

ASSEMBLY 108156 VERSION NO.	VERSION CHARACTERISTIC	R1	W1
		121-1040	100-0005
-01		OMIT	USE

TABLE IV [8]

VOLTAGE AND GROUNDS						
TYPE	+5V	GND	-5V			
7400	14	7				
7404	14	7				
7405	14	7				
74LS02	14	7				
74LS93	4	11				
555	8	1				

TABLE V [5]

U5
7405

REFERENCE DESIGNATION		
LAST USED	NOT USED	DELETED
C20		
CR5		CR5
J506		
Q4		
R61		
TP13		
U16		
VR5		
W2		W2

[9] SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

[8] FOR IC GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NO.S SEE TABLE IV.

[7] DIODES ARE IN4446.

6. CAPACITOR VALUES ARE IN MICROFARADS, 10%, 35V.

[5] FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

4. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL IX ARE 1/8W.

3. (RESERVED)

[2] FOR VALUE, PART NO. AND USAGE OF COMPONENTS AFFECTED BY VERSION NO. SEE TABLE II.

[1] FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DWGS :

NOTES: UNLESS OTHERWISE SPECIFIED

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS .005 MAX.

SIGNATURES	DATE
DR. TJOSON	8/17
CHK. K. NOBLE	9/17
DES	
ENGR	
PROJ. ENGR. [illegible]	9/17

PERTEC PERIPHERAL EQUIPMENT

TITLE
SCHEMATIC
TEMP COMP

108176			
NEXT ASSY	USED ON	FINISH:	MATL:
APPLICATION			

SIZE	CODE IDENT NO.	DWG NO.	REV
E		108175	E
SCALE ——	DO NOT SCALE DWG.	SHEET 1 OF 4	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-JA PRE PROD RELEASE	9/11/81	TGM	EW	MCL
B	ECN 10104	10/19/82	TGM	EW	MCL
C	ECN 10901	11/18/82	TGM	EW	MCL
D	ECN 11584	7/12/83	MM	EW	MCL
E	ECN 13451	9/14/84	LG	EW	MCL

[9] SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

[8] FOR IC GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS SEE TABLE IV.

[7] DIODES ARE IN4446.

6. CAPACITOR VALUES ARE IN MICROFARADS, 10%, 35V.

[5] FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

4. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W. ALL 1% ARE 1/8W.

3. (RESERVED)

[2] FOR VALUE, PART NO. AND USAGE OF COMPONENTS AFFECTED BY VERSION NO. SEE TABLE II.

[1] FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DWGS :

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .01, .XXX ± .005, ANGULAR ± 1/2°, X ± , X ± , BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. TGM	9/11/81
CHK. E. NOBLE	9/14/81
DES	
ENGR	
PROJ. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE: SCHEMATIC TEMP COMP

NEXT ASSY USED ON: APPLICATION

FINISH: MATL:

SIZE E | CODE IDENT NO. | DWG NO. 108175 | REV E

SCALE — | DO NOT SCALE DWG | SHEET 1 OF 4

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				

SIZE E | CODE IDENT NO. | DWG NO. 108175 | REV E

SCALE NONE | DO NOT SCALE DWG | SHEET 2 OF 4

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				

PART OF J506
NLLPS6 8
NLUPS6 6
NLISM6 7
NLPMY6 16
+5V 17 18
GND 11 12 13 14 15
-5V 19 20
PART OF J502
NLRLDT 5

R36 1K
R37 1K
R38 4.7K
R39 1K
R40 1.96R 1%
R41 1K
R42 12.1K 1%
R43 3.16K 1%
R44 560
R45 1K
R46 1K
R47 1K
R48 1K
R49 4.7K
R50 1K
R51 4.7K
R52 909K 1%
R53 12.1K 1%

C3 220PF 5% 500V
C4 1UF 10% 35V
C5 220PF 5% 500V
C6 220PF 5% 500V
C7 82UF 10% 10V
C8 .01 10% 100V
C11,12,13 2.2
C20 .047 20% 50V

CR1

U5 7405
U8 555
U9 74LS02
U10 74LS93
U11 7405
U12 7400
U13 8T20
U14 7404
U15 74LS02

TP9
TP10
TP11
TP12
TP13

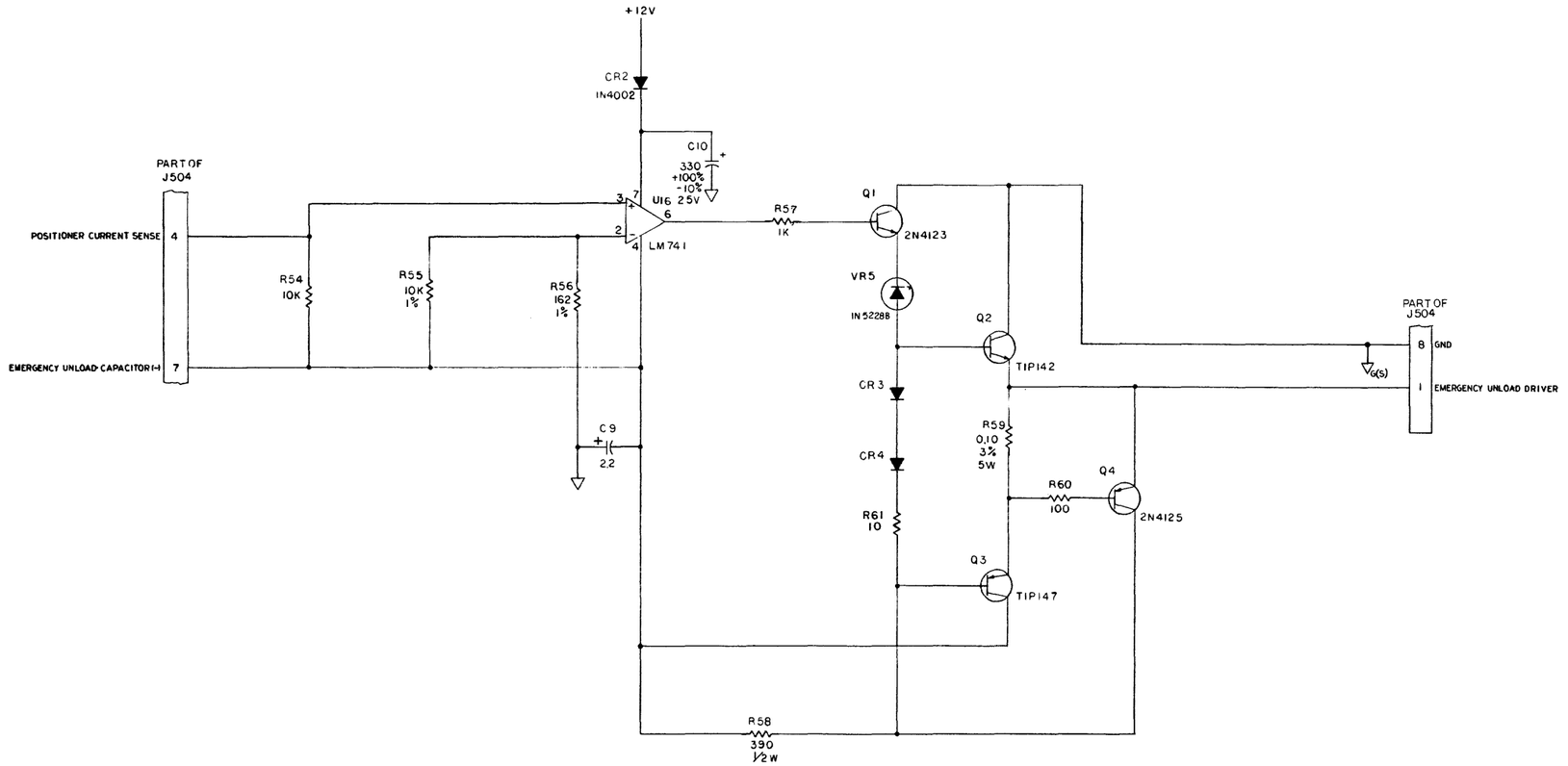
G(L)
-5V

PART OF J506
9 NLDIS6
5 NTTREG
NLTPC6 (2-8D)
10 NLDID6

PART OF J504
POSITIONER CURRENT SENSE 4
EMERGENCY UNLOAD CAPACITOR (-) 7

SIZE	CODE IDENT NO.	DWG NO.	REV
E		108175	E
SCALE	DO NOT SCALE DWG	SHEET 3 OF	

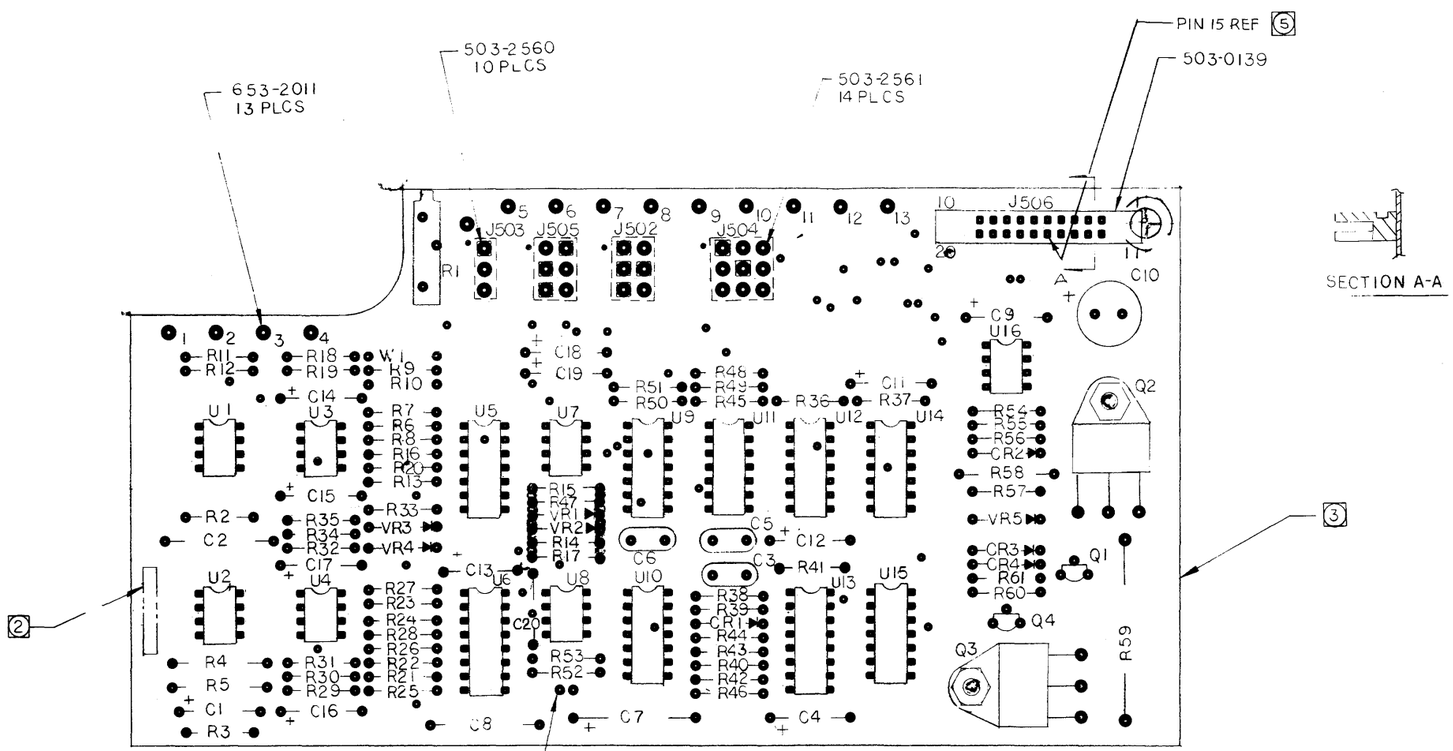
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT1				



SIZE	CODE IDENT NO.	DWG NO.	REV
E		108175	E
SCALE ——	DO NOT SCALE DWG	SHEET 4 OF	

DWG NO. 108175 REV E

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-JA PRE PROD RELEASE	9/11/77	TEM	RN	TL
B	ECN 10104	6/1/78	C.J.		TL
	ERN 9-TU PROD. RELEASE	9/1/77	GM		TL
C	ECN 10672	12/27/77	DP		TL
D	ECN 10901	1/11/78	S.		TL
E	ECN 13951	8/22/79	J.J.		
F	ECN 13748	6/2/80	C.J.	G.S.	



SECTION A-A

SCHEMATIC: 108175
REF DWGS

PART NO 108176-01 REV G

(5) REMOVE PIN 15 ON J506 FOR KEYING.

(4) (DELETED)

(3) THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 108177-01 REV D AND SUBSEQUENT.

(2) MARK VERSION NO. AND VERSION ISSUE LETTER.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR. T. MORTON	3/10/77
CHK R. NOBLE	3/17/77
DES	
ENGR	
PROJ. ENGR	3/18/77

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
PCBA
TEMP COMP

NEXT ASSY | 1RT USED ON
APPLICATION

FINISH:

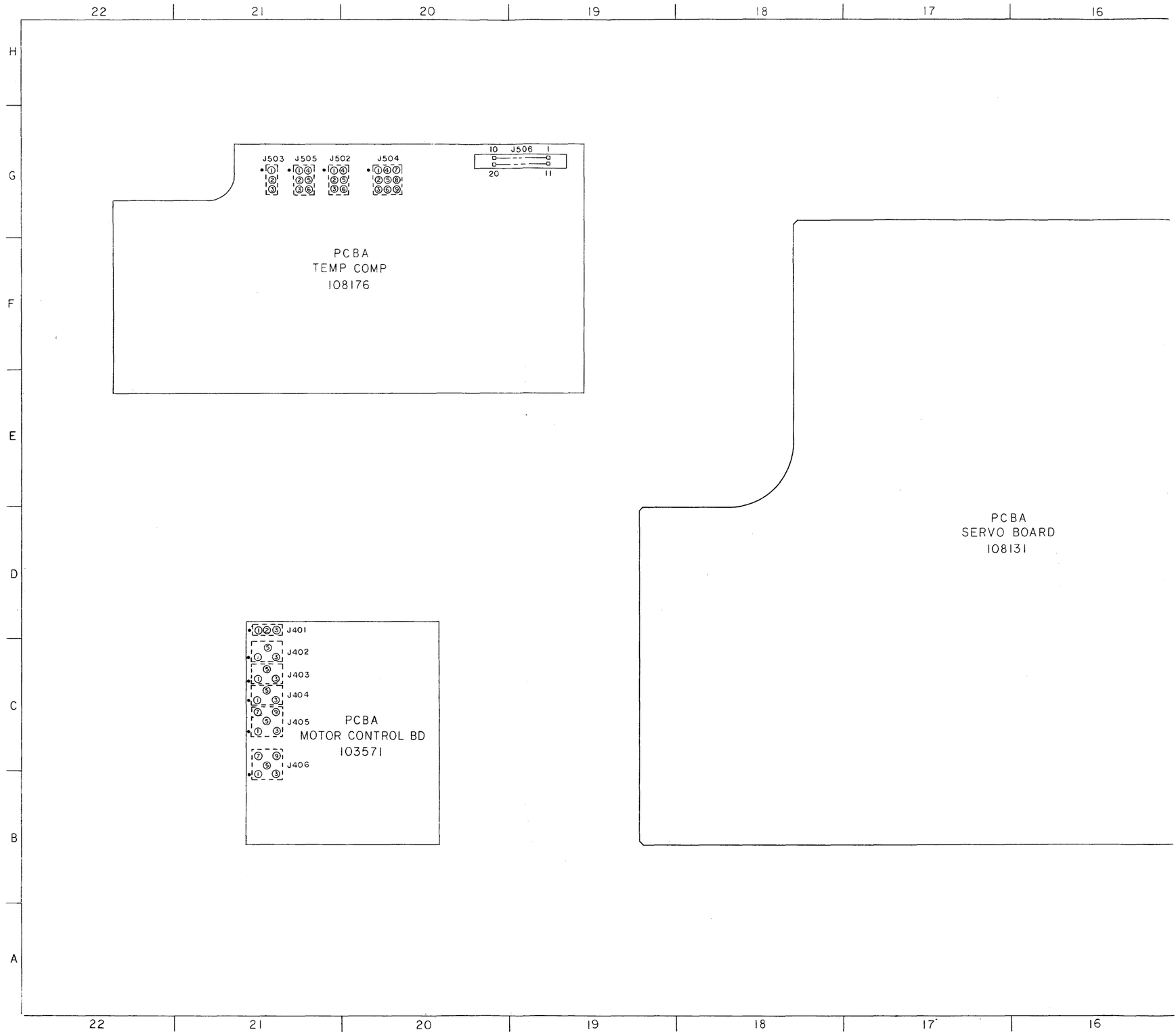
MATL: SEE L/M

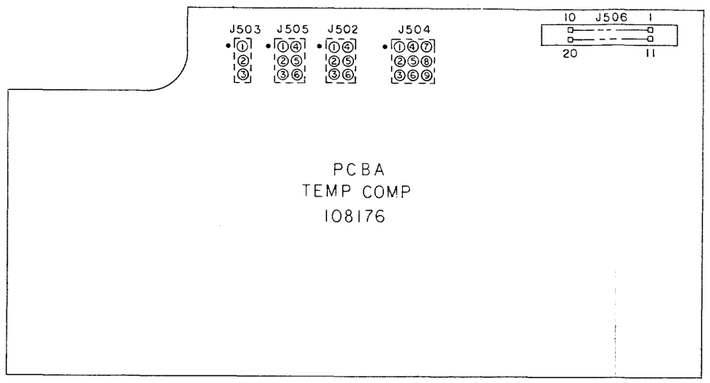
SIZE	CODE IDENT NO.	DWG NO.	REV
D	32097	108176	F

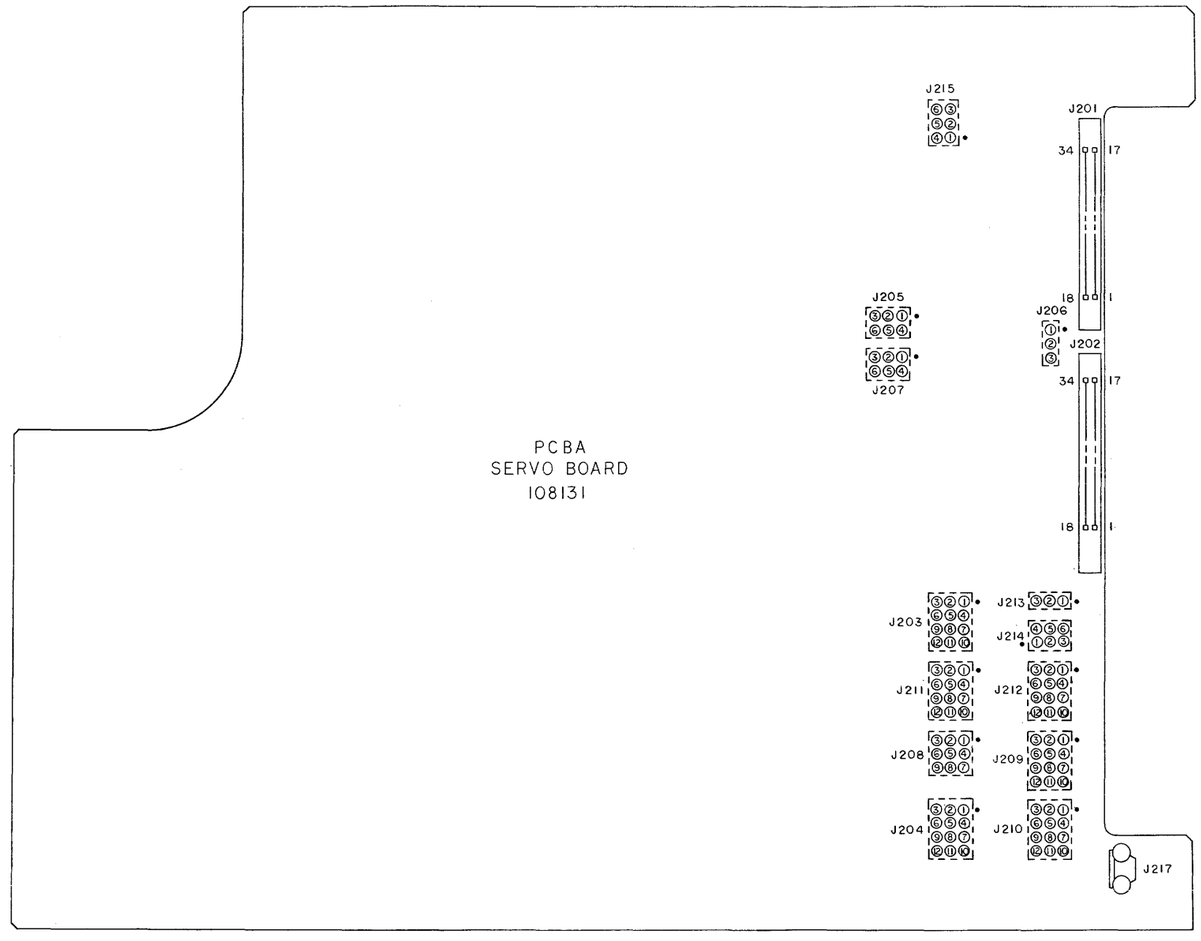
SCALE 2:1 | DO NOT SCALE DWG | SHEET OF

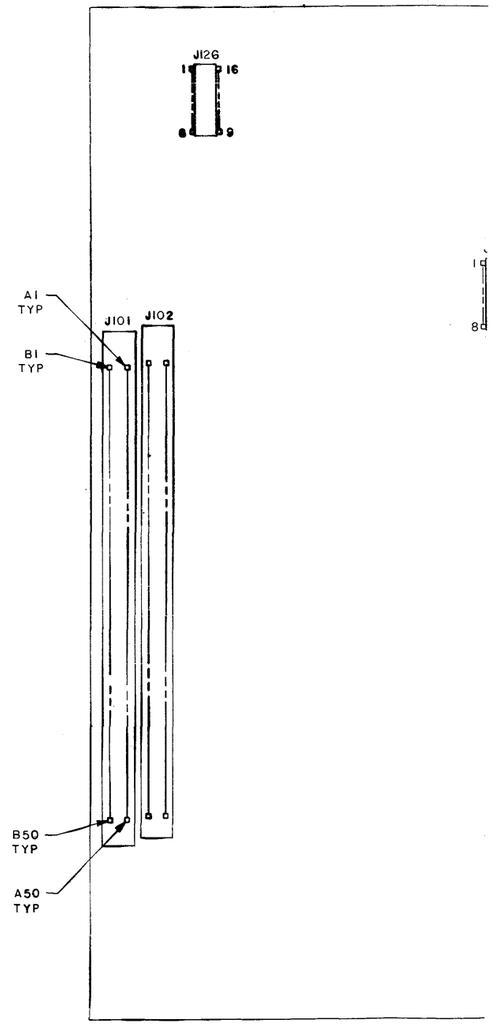
DWG NO. 108176 REV F

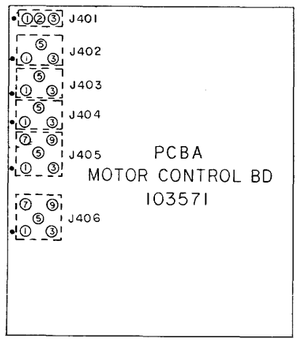
PRINTED ON DIETRICH-POST CLEARPRINT 1020


22
21
20
19
18
17
16
H
G
F
E
D
C
B
A
J503
J505
J502
J504
10 J506 1
20 11
PCBA
TEMP COMP
108176
PCBA
SERVO BOARD
108131
J401
J402
J403
J404
J405
J406
PCBA
MOTOR CONTROL BD
103571


J503
J505
J502
J504
10 J506 1
20 11
PCBA
TEMP COMP
108176


PCBA
SERVO BOARD
108131
J215
J201
34 17
J205
J206
J202
J207
34 17
18 1
J203
J213
J214
J211
J212
J208
J209
J204
J210
J217


J126
16
9
A1
TYP
J101
J102
B1
TYP
B50
TYP
A50
TYP


J401
J402
J403
J404
J405
J406
PCBA
MOTOR CONTROL BD
103571

18 17 16 15 14 13 12 11 10 9 8

PCBA
SERVO BOARD
108131

J215
J205
J207
J206
J201
34 17
18 1
J202
34 17
18 1
J203
J213
J214
J211
J212
J208
J209
J204
J210
J217

A1
TYP
B1
TYP
B50
TYP
A50
TYP

J101
J102

J126
1 16
8 9

J122
1 16
8 9

J127
1 16
8 9

J125
1 16
8 9

J121
1 16
8 9

PCBA
DIABLO LOGIC
108161

PCBA
PERTEC LOGIC
108166

J128
1 16
8 9

J123
9 8
16 1

J108
J109
J111
J110
J112

J106
J107
J103
18 34
1 17

18 17 16 15 14 13 12 11 10 9 8

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 9-76 PRE PROD REL	7/4/78	RJ	MM	[illegible]
A	ERN 10-CW PRODUCTION RELEASE	7/24/78	[illegible]	MM	[illegible]
B	ECN 11264	9/19/78	[illegible]	RD	[illegible]
C	E.C.N. 11538.	5/9/79	M.R.	RD	[illegible]

LOCATION OF J611 ON 4400 BPI

PIN ORIENTATION TYP FOR J600 THRU J607

J611 (1, 18, 8, 9)

J611 (1, 18, 8, 9)

J600 (1, 2, 3, 4, 5)

J601

J602

J603

J606

J607

J604

J605

PCBA
R/W SELECTION MATRIX
AND PREAMP
108146
(2200 BPI)
108171
(4400 BPI)

J610 (1, 14, 7, 8)

J114 (1, 2, 3)

J104 (1, 7, 18, 1)

J105 (34, 1, 7, 18, 1)

J128 (1, 16, 8, 9)

J108 (3, 2, 1, 6, 5, 4)

J109 (3, 2, 1, 6, 5, 4)

J111 (3, 2, 1, 6, 5, 4, 9, 8, 7)

J110 (6, 5, 4, 3, 2, 1, 9, 8, 7)

J112 (1, 4, 7, 9, 2, 5, 8, 0, 3, 6, 9, 12)

J106 (3, 2, 1, 6, 5, 4, 9, 8, 7, 12, 11, 10)

J107 (6, 5, 4, 3, 2, 1, 9, 8, 7, 12, 11, 10)

J103 (18, 1, 34, 17)

J311 (1, 16, 8, 9)

J310 (1, 14, 7, 8)

J304 (3, 2, 1, 6, 5, 4, 9, 8, 7, 12, 11, 10)

J305 (17, 34, 1, 18)

J306 (10, 20, 1, 11)

PCBA
READ/WRITE
108141
(2200 BPI)
108136
(4400 BPI)

USED ON 2200 BPI ONLY

J303 (1, 16, 8, 9)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± ANGULAR ± 1/2°; XXX ±
BREAK ALL SHARP CORNERS .XX MAX.

SIGNATURES	DATE
DR [illegible]	11/19/79
CHK [illegible]	11/19/79
ENG	
PROD [illegible]	5/14/79
PROJ [illegible]	5/24/79

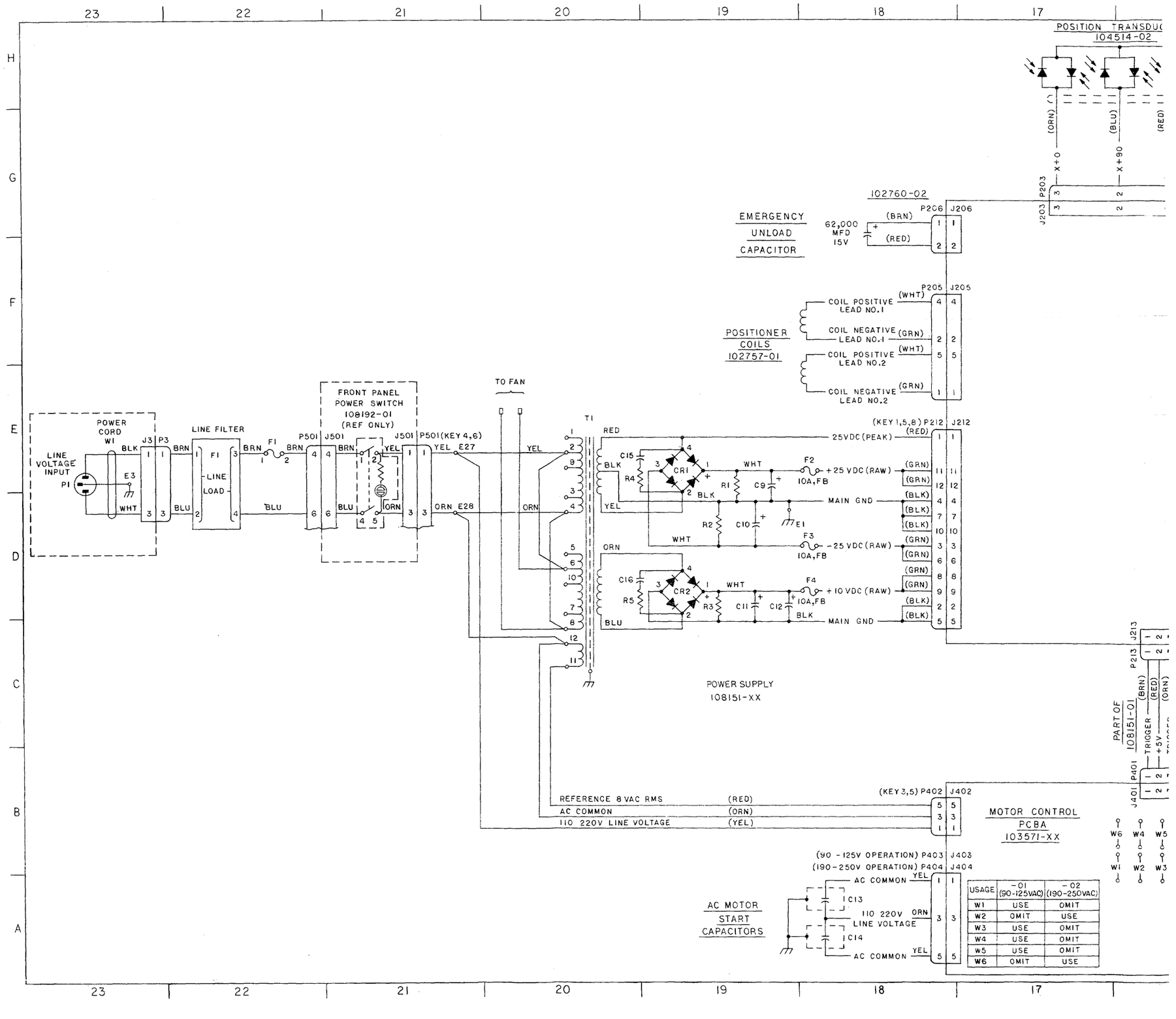
FINISH: MATL:

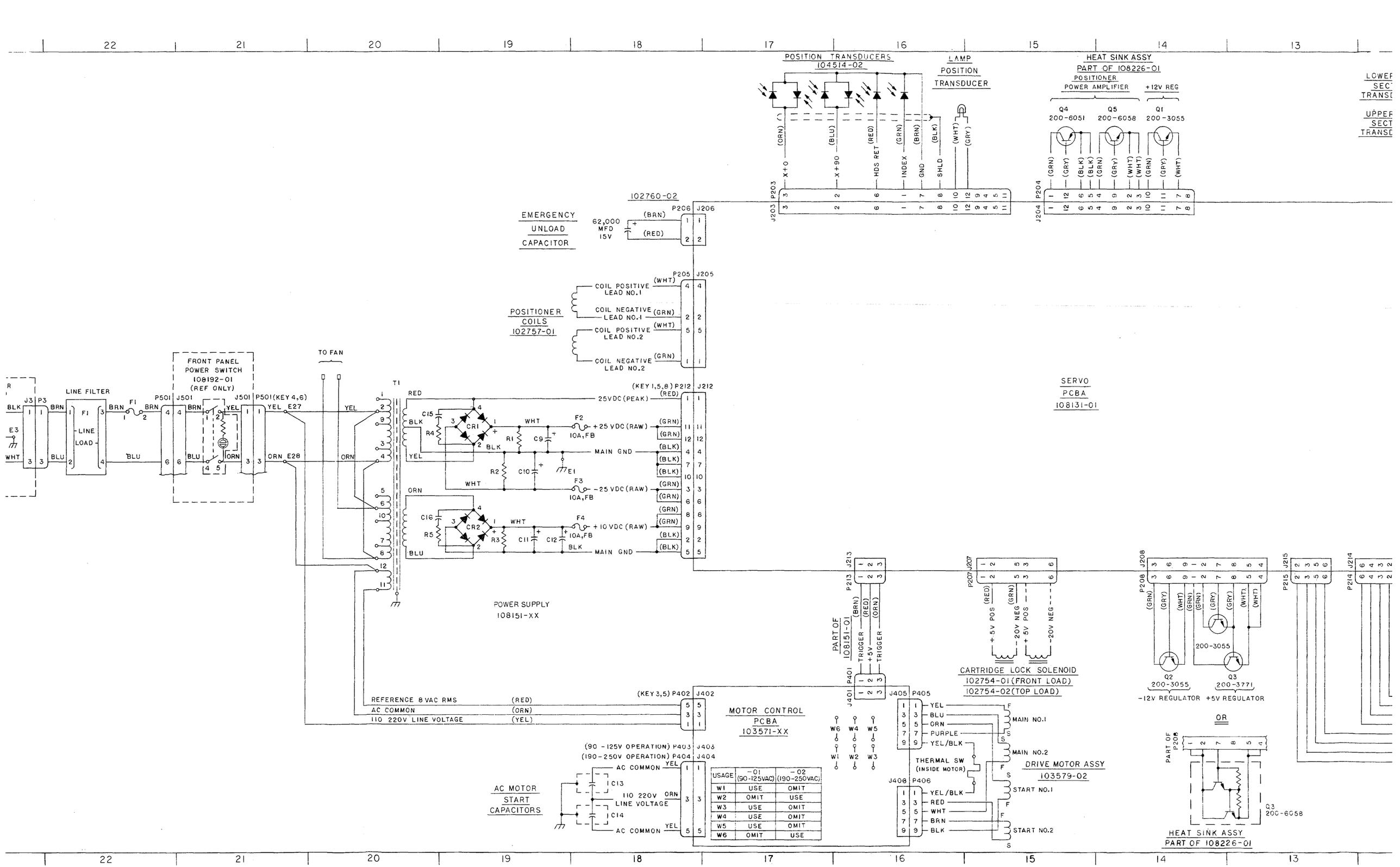
TOP ASSY D3 EXT
NEXT ASSY | 1ST USED ON
APPLICATION

PERTEC
PERIPHERAL EQUIPMENT DIVISION

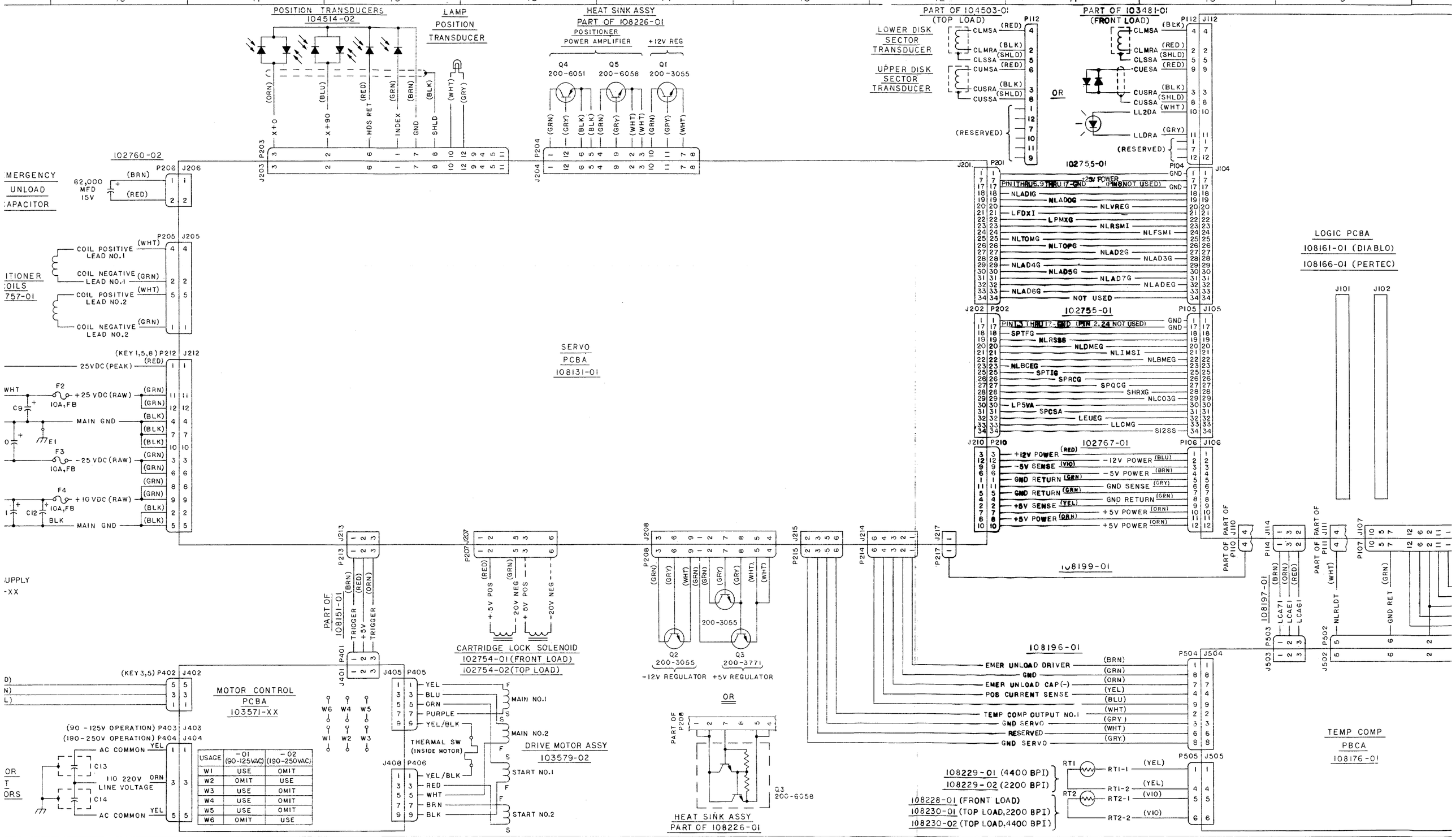
TITLE: D3000 EXT INTERCONNECT DIAGRAM

SIZE J | CODE IDENT NO. 32097 | DWG NO. 108105 | REV C
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 2


POSITION TRANSDUCER
104514-02
(ORN)
(BLU)
(RED)
X+0
X+90
J203 P203
102760-02
EMERGENCY UNLOAD CAPACITOR
62,000 MFD 15V
(BRN)
(RED)
P206 J206
POSITIONER COILS 102757-01
COIL POSITIVE LEAD NO.1
COIL NEGATIVE LEAD NO.1
COIL POSITIVE LEAD NO.2
COIL NEGATIVE LEAD NO.2
(WHT)
(GRN)
P205 J205
TO FAN
FRONT PANEL POWER SWITCH 108192-01 (REF ONLY)
POWER CORD W1
LINE VOLTAGE INPUT
P1
E3
LINE FILTER
F1
LINE
LOAD
P501 J501
J501 P501 (KEY 4,6)
E27
E28
T1
RED
BLK
YEL
ORN
WHT
BLU
BRN
C15
R4
CR1
C9
R1
R2
C10
E1
F2
10A,FB
F3
C16
R5
CR2
R3
C11
C12
F4
25VDC (PEAK)
+25 VDC (RAW)
MAIN GND
-25 VDC (RAW)
+10 VDC (RAW)
(KEY 1,5,8) P212 J212
(RED)
(GRN)
(BLK)
POWER SUPPLY 108151-XX
PART OF 108151-01
TRIGGER
+5V
P213 J213
P401 J401
REFERENCE 8 VAC RMS
AC COMMON
110 220V LINE VOLTAGE
(KEY 3,5) P402 J402
MOTOR CONTROL PCBA 103571-XX
W1
W2
W3
W4
W5
W6
(90 - 125V OPERATION) P403 J403
(190-250V OPERATION) P404 J404
AC MOTOR START CAPACITORS
C13
C14
110 220V LINE VOLTAGE
USAGE
-01 (90-125VAC)
-02 (190-250VAC)
W1 USE OMIT
W2 OMIT USE
W3 USE OMIT
W4 USE OMIT
W5 USE OMIT
W6 OMIT USE



USAGE	-01 (90-125VAC)	-02 (190-250VAC)
W1	USE	OMIT
W2	OMIT	USE
W3	USE	OMIT
W4	USE	OMIT
W5	USE	OMIT
W6	OMIT	USE


POSITION TRANSDUCERS
104514-02
LAMP
POSITION
TRANSDUCER
(ORN)
(BLU)
(RED)
(GRN)
(BRN)
(BLK)
(WHT)
(GRY)
X+0
X+90
HDS RET
INDEX
GND
SHLD
P203
J203
HEAT SINK ASSY
PART OF 108226-01
POSITIONER
POWER AMPLIFIER
+12V REG
Q4
200-6051
Q5
200-6058
Q1
200-3055
P204
J204
PART OF 104503-01
(TOP LOAD)
LOWER DISK
SECTOR
TRANSDUCER
UPPER DISK
SECTOR
TRANSDUCER
CLMSA
CLMRA
CLSSA
CUMSA
CUSRA
CUSSA
(RESERVED)
P112
OR
PART OF 103481-01
(FRONT LOAD)
CUESA
LL2DA
LLDRA
J112
102760-02
MERGENCY
UNLOAD
APACITOR
62,000
MFD
15V
P206
J206
ITIONER
OILS
757-01
COIL POSITIVE
LEAD NO.1
COIL NEGATIVE
LEAD NO.1
COIL POSITIVE
LEAD NO.2
COIL NEGATIVE
LEAD NO.2
P205
J205
SERVO
PCBA
108131-01
102755-01
PIN 1 THRU 17-GND (PIN 2,24 NOT USED)
+22V POWER (PIN 9 NOT USED)
PIN 1 THRU 5,9 THRU 17-GND
NLAD1G
NLAD0G
NLVREG
LFDXI
LPMXG
NLRSMI
NLFSMI
NLTOMG
NLTOPG
NLAD2G
NLAD3G
NLAD4G
NLAD5G
NLAD7G
NLADEG
NLAD6G
NOT USED
P201
J201
P104
J104
P202
J202
P105
J105
SPTFG
NLRSBS
NLDMEG
NLIMSI
NLBMEG
NLBCEG
SPTIG
SPRCG
SPQCG
SHRXG
NLC03G
LP5VA
SPCSA
LEUEG
LLCMG
SI2SS
102767-01
+12V POWER
-5V SENSE
GND RETURN
GND RETURN
+5V SENSE
+5V SENSE
-12V POWER
-5V POWER
GND SENSE
GND RETURN
+5V POWER
+5V POWER
P210
J210
P106
J106
LOGIC PCBA
108161-01 (DIABLO)
108166-01 (PERTEC)
J101
J102
(KEY 1,5,8) P212
J212
25VDC (PEAK)
F2
+25 VDC (RAW)
10A,FB
C9
MAIN GND
E1
F3
-25 VDC (RAW)
10A,FB
F4
+10 VDC (RAW)
10A,FB
C12
BLK
MAIN GND
UPPLY
-XX
PART OF
108151-01
TRIGGER
+5V
TRIGGER
P213
J213
P401
J401
(KEY 3,5) P402
J402
D)
N)
L)
MOTOR CONTROL
PCBA
103571-XX
W6
W4
W5
W1
W2
W3
(90 - 125V OPERATION) P403
J403
(190 - 250V OPERATION) P404
J404
AC COMMON
C13
110 220V
LINE VOLTAGE
C14
AC COMMON
OR
T
ORS
USAGE | -01 (90-125VAC) | -02 (190-250VAC)
W1 | USE | OMIT
W2 | OMIT | USE
W3 | USE | OMIT
W4 | USE | OMIT
W5 | USE | OMIT
W6 | OMIT | USE
P207 J207
+5V POS
-20V NEG
+5V POS
-20V NEG
CARTRIDGE LOCK SOLENOID
102754-01 (FRONT LOAD)
102754-02 (TOP LOAD)
J405 P405
J408 P406
YEL
BLU
ORN
PURPLE
YEL/BLK
THERMAL SW
(INSIDE MOTOR)
YEL/BLK
RED
WHT
BRN
BLK
MAIN NO.1
MAIN NO.2
START NO.1
START NO.2
DRIVE MOTOR ASSY
103579-02
P208 J208
Q2
200-3055
Q3
200-3771
-12V REGULATOR
+5V REGULATOR
OR
PART OF P208
Q3
200-6058
HEAT SINK ASSY
PART OF 108226-01
P215 J215
P214 J214
P217 J217
108199-01
108196-01
EMER UNLOAD DRIVER
GND
EMER UNLOAD CAP(-)
POS CURRENT SENSE
TEMP COMP OUTPUT NO.1
GND SERVO
RESERVED
GND SERVO
P504 J504
TEMP COMP
PBCA
108176-01
108229-01 (4400 BPI)
108229-02 (2200 BPI)
108228-01 (FRONT LOAD)
108230-01 (TOP LOAD,2200 BPI)
108230-02 (TOP LOAD,4400 BPI)
RT1
RT2
RT1-1
RT1-2
RT2-1
RT2-2
P505 J505
PART OF P110 J110
PART OF P111 J111
PART OF P107 J107
P114 J114
108197-01
P503 J503
P502 J502
LCA71
LCAE1
LCA61
NLRLDT
GND RET

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1				

ART OF 103481-01 (FRONT LOAD)

P112 J112

CLMSA	(BLK)	4	4
CLMRA	(RED)	2	2
CLSSA	(SHLD)	5	5
CUESA	(RED)	9	9
CUSRA	(BLK)	3	3
CUSSA	(SHLD)	8	8
LL2DA	(WHT)	10	10
LLDRA	(GRY)	11	11
(RESERVED)		1	1
		7	7
		12	12

5-01

P104 J104

POWER	GND	1	1
		7	7
(PINS NOT USED)	GND	17	17
		18	18
		19	19
NLVREG		20	20
		21	21
NLRSMI		22	22
NLFSMI		23	23
		24	24
NLAD2G		25	25
NLAD3G		26	26
		27	27
NLAD7G		28	28
NLAD8G		29	29
		30	30
USED		31	31
		32	32
		33	33
		34	34

5-01

P105 J105

12,24 NOT USED	GND	1	1
	GND	17	17
		18	18
		19	19
MEG		20	20
NLIMSI		21	21
NLBMEG		22	22
		23	23
		25	25
		26	26
SPQCG		27	27
SHRXG		28	28
NLC03G		29	29
		30	30
		31	31
UEG		32	32
LLCMG		33	33
SI2SS		34	34

02767-01

P106 J106

-12V POWER	(BLU)	1	1
-5V POWER	(BRN)	2	2
GND SENSE	(GRY)	3	3
GND RETURN	(GRN)	4	4
+5V POWER	(ORN)	5	5
+5V POWER	(ORN)	6	6
		7	7
		8	8
		9	9
		10	10
		11	11
		12	12

LOGIC PCBA
108161-01 (DIABLO)
108166-01 (PERTEC)

J101 J102

J108 P108

NCUSRS	(BRN)	1	1
CUPOS	(RED)	2	2
NCUPOS	(ORN)	3	3
NCLSRS	(YEL)	4	4
NCLPOS	(GRN)	5	5
CLPOS	(BLU)	6	6

WRITE PROTECT SWITCH ASSY 102761-02

J109 P109

PART OF 103481-01 (FRONT LOAD)
PART OF 102762-02 (TOP LOAD)

		4	4
		5	5
NCCRIS	(BRN)	1	1
NCCSIS	(RED)	2	2
CCSIS	(ORN)	3	3
		6	6

S1

PART OF J111 / PART OF P111 — 102765-02

NLUPLT	(BRN)	1	1
NLLPLT	(RED)	2	2
LPI2A	(ORN)	3	3
NLSLDT	(GRN)	5	5
		6	6
		7	7
NLRXDT	(GRY)	8	8
NLRLDT	(WHT)	9	9

PROT, PROT, SAFE, RUN/STOP, RDY

PART OF 102773-XX

PART OF J110 / PART OF P110 — 102766-01

		2	2
CRSSS	(RED)	3	3
NCRSRS	(ORN)	1	1
	(BRN)	5	5
NCUSIS	(GRN)	8	8
NCUS2S	(GRY)	9	9
NCUS3S	(WHT)	6	6
NCUS4S	(BLU)	7	7
NCSSRS	(VIO)		

RUN/STOP SWITCH

UNIT SELECT SWITCH

J103 P103 — 102755-04

LEUEG	PIN ITHPUI4 GND NOT USED	16	16
PINS 1 THRU 13 - GND		17	17
NLPMYG	NLRECG	18	18
NRRDSG	NRRCSG	19	19
LDAWG	NLTOPG	20	20
NLTOMG	NLUPSG	21	21
NLUHSG	SPCSA	22	22
NLWDFT	NLWMXG	23	23
NLECEG	RWECG	24	24
NLISMG	NLLPSG	25	25
NLDISG	NLDIDG	26	26
		27	27
		28	28
		29	29
		30	30
		31	31
		32	32
		33	33
		34	34

P305 J305

J107 P107

		10	10
		5	5
		7	7
		12	12
		6	6
		2	2
		11	11
		1	1
		3	3
		9	9
		8	8

108198-01

GND	RETURN (GRN)	1	1
GND	RETURN (GRN)	2	2
+12V	POWER (RED)	6	6
SI2SS	(WHT)	7	7
+5V	POWER (ORN)	9	9
-12V	POWER (BLU)	10	10
-5V	POWER (BRN)	11	11
+5V	POWER (ORN)	12	12

P304 J304

R/W PCBA
(2200 BPI) 108141 } 01 (1500 RPM)
(4400 BPI) 108136 } 02 (2400 RPM)

J503 P503 — 108197-01

LCA7I	(BRN)	1	1
LCAEI	(ORN)	2	2
LCAGI	(RED)	3	3

J502 P502

NLRLDT	(WHT)	5	5
GND RET	(GRN)	6	6
		2	2
		3	3

J504 P504

	(BRN)	1	1
	(GRN)	8	8
	(ORN)	7	7
	(YEL)	4	4
	(BLU)	9	9
	(WHT)	2	2
	(GRY)	3	3
	(WHT)	6	6
	(GRY)	8	8

TEMP COMP PBCA 108176-01

J505 P505

RTI-1	(YEL)	1	1
RTI-2	(YEL)	4	4
RT2-1	(VIO)	5	5
RT2-2	(VIO)	6	6

108194-01

J506 P506

PINS 1 THRU 4 - NOT USED		5	5
NTTREG	NLUPSG	6	6
NLISMG	NLLPSG	7	7
NLDISG	NLDIDG	8	8
GND	PINS 11 THRU 15 - GND	9	9
NLPMYG	+5V	10	10
+5V	+5V	11	11
-5V	-5V	16	16
		17	17
		18	18
		19	19
		20	20

P306 J306

104246-06 (4400 BPI)

J311 P311 — P611 J611

GND		1	1
NLUHSG		2	2
NLUPSG		3	3
LLPSG		4	4
NOT USED		5	5
+25V SWITCHED		6	6
LDAMG		7	7
+ WRITE DRIVE		8	8
- WRITE DRIVE		9	9
ERASE		10	10
+ 5VDC		11	11
+ 5VDC		12	12
NOT USED		13	13
NOT USED		14	14
GND		15	15
MULT HD SEL		16	16

108193-01 (4400 BPI)

J310 P310 — P610 J610

READ SIG 2		1	1
GND		2	2
+12VDC		3	3
SPARE		4	4
+ WRITE		5	5
-6.8VDC		6	6
GND		7	7
GND		8	8
+6.8VDC		9	9
-12V		10	10
NOT USED		11	11
SPARE		12	12
GND		13	13
READ SIG 1		14	14

OR

104246-06 (2200 BPI)

J311 P311 — P611 J611

HEAD SEL 1		1	1
WRT MODE		2	2
MULT HD SEL		3	3
ERASE DRIVER		4	4
GND		5	5
-12 VDC		6	6
PLAT SEL 2		7	7
+12VDC		8	8
+12VDC		9	9
PLAT SEL 1		10	10
-12VDC		11	11
GND		12	12
READ SW		13	13
HEAD SEL 4		14	14
HEAD SEL 3		15	15
HEAD SEL 2		16	16

108193-01 (2200 BPI)

J310 P310 — P610 J610

READ SIG 1		1	1
GND		2	2
NOT USED		3	3
GND		4	4
NOT USED		5	5
-6.8VDC		6	6
GND		7	7
GND		8	8
+6.8VDC		9	9
NOT USED		10	10
NOT USED		11	11
WRT DRIVER 2		12	12
WRT DRIVER 1		13	13
READ SIG 2		14	14

MATRIX PCBA
(2200BPI) 108146
(4400BPI) 108171
} 01 (1500RPM)
02 (2400RPM)

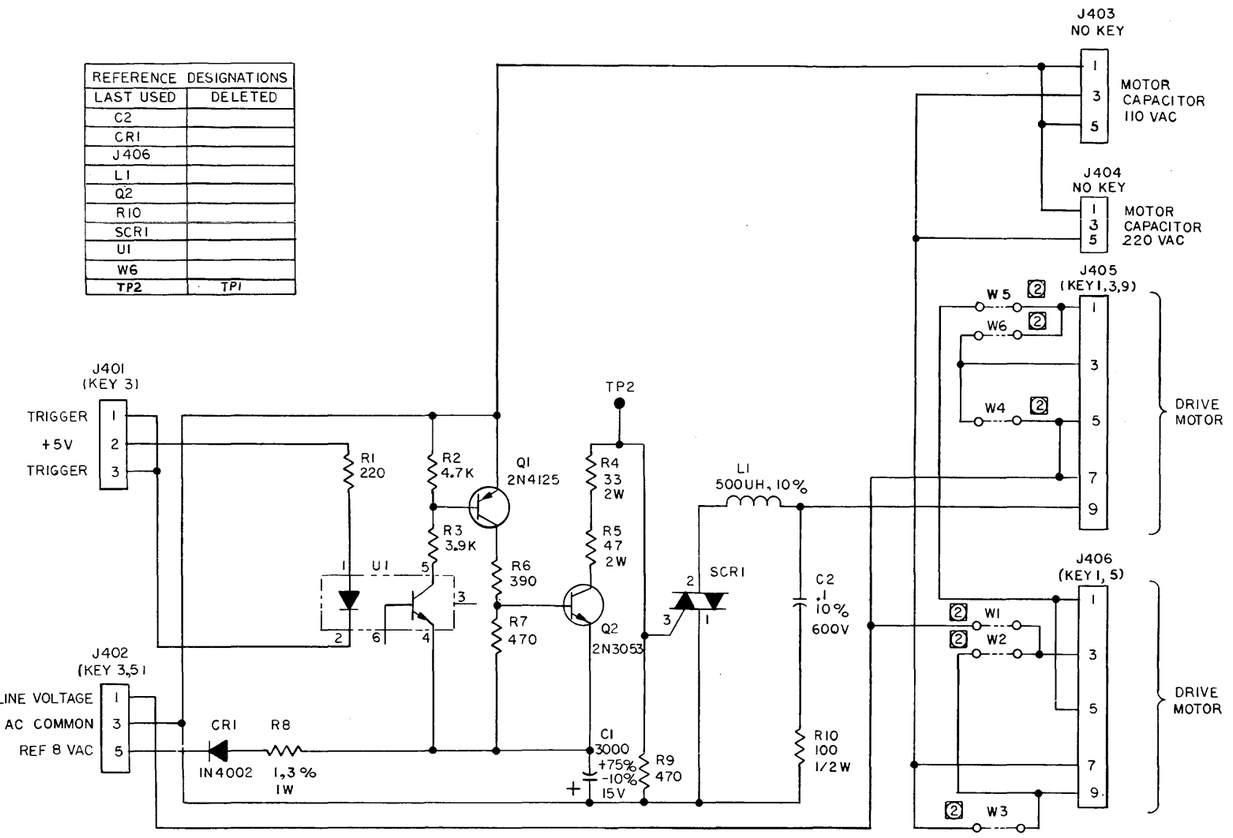
P600 THRU P607 (TYP) J600 THRU J607 (TYP)

	(WHT)	1	1
R/W			
	(BLU)	4	4
R/W			
ERASE	(RED)	5	5
	(GRN)	3	3

SIZE	CODE IDENT NO.	DWG NO.	REV
J		108105	C
SCALE	DO NOT SCALE DWG.	SHEET 2 OF 2	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 6-VA PROD RELEASE	3/4/74	F.L.	[illegible]	[illegible]
B	ECN 12524	7/2/74	L.W.	[illegible]	[illegible]

REFERENCE DESIGNATIONS	
LAST USED	DELETED
C2	
CR1	
J406	
L1	
Q2	
R10	
SCR1	
U1	
W6	
TP2	TP1



[1] TABLE I

PART NO.	REFERENCE DESIG
100-2215	R1
100-3915	R6
100-3925	R3
100-4715	R7,9
100-4725	R2
101-1015	R10
103-3305	R4
103-4705	R5
113-0103	R8
131-1046	C2
134-3000	C1
200-3053	Q2
200-4125	Q1
205-4010	SCR1
300-4002	CR1
403-0001	U1
103585-01	L1

[2] TABLE II

PART NO.	ASSY 103571	
100-0005	-01 (90-125VAC)	-02 (190-250VAC)
W1	USE	OMIT
W2	OMIT	USE
W3	USE	OMIT
W4	USE	OMIT
W5	USE	OMIT
W6	OMIT	USE

4. ALL CAPACITOR VALUES ARE IN MICROFARADS.

3. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

[2] FOR VALUE, PART NO. AND USAGE OF COMPONENTS AFFECTED BY VERSION NO. SEE TABLE II.

[1] FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION NO. SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NO. 103571
SPECIFICATION NO. 103574
REFERENCE DRAWINGS:

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± ANGULAR ± 1/2°
XXX ±
X ±
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR [illegible]	9/4/74
CHK [illegible]	10-16
DES	
ENGR	
PROJ. ENGR [illegible]	9/4/74

PERTEC PERIPHERAL EQUIPMENT

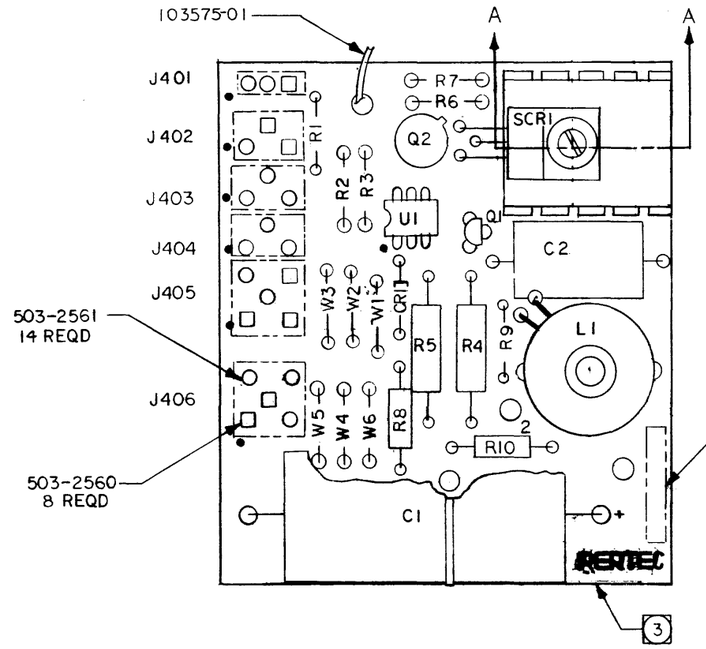
TITLE
SCHEMATIC –
MOTOR CONTROL BOARD

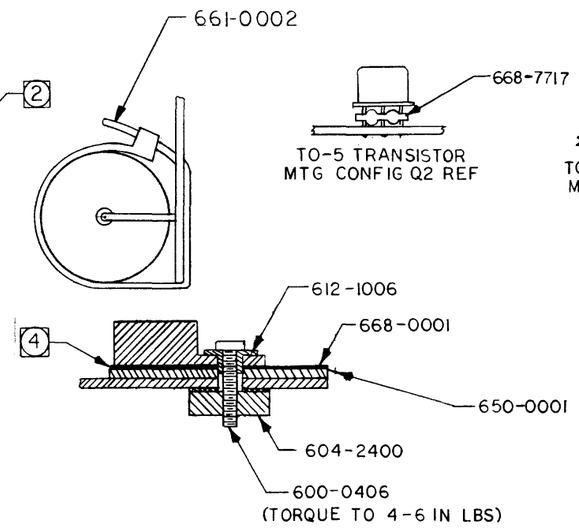
FINISH:
MATL:
NEXT ASSY | 1ST USED ON
APPLICATION

SIZE	CODE IDENT NO.	DWG NO.	REV
F		103570	B
SCALE	DO NOT SCALE DWG	SHEET 1 OF 1	

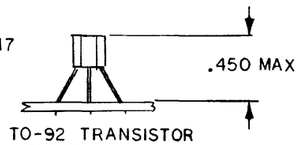
2/72 DIETZGEN-POST CLEARPRINT 1000

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 6-VA PROD RELEASE	9/25/70			
A1	ECN 7066	1-22-75	RN		
B	ECN 7834	4/1/75	G.J.R		
C	ECN 8382	3-17-76	A K		
D	ECN 12524	2/8/79	H M		
D1	ECN 13658	9/5/79			





SECTION A-A
SCALE: NONE



103571 - 01 REV D1

FOR ASSY VERSION INFORMATION SEE SCHEMATIC 103570.

(4) APPLY 665-0001 TO BOTH SIDES OF 668-0001.

(3) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 103572-01 REV. F AND SUBSEQUENT.

(2) MARK PART NO 103571 INCLUDING VERSION NO. AND VERSION ISSUE LETTER. LOCATE APPROX AS SHOWN.

1. ASSEMBLE PER STANDARD MFG METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR	9/26/79
CHK	10-17-79
DES	
ENGR	
PROJ. ENGR	10/21/79

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
MOTOR CONTROL BOARD

NEXT ASSY	1ST USED ON
	D3000
APPLICATION	

FINISH:

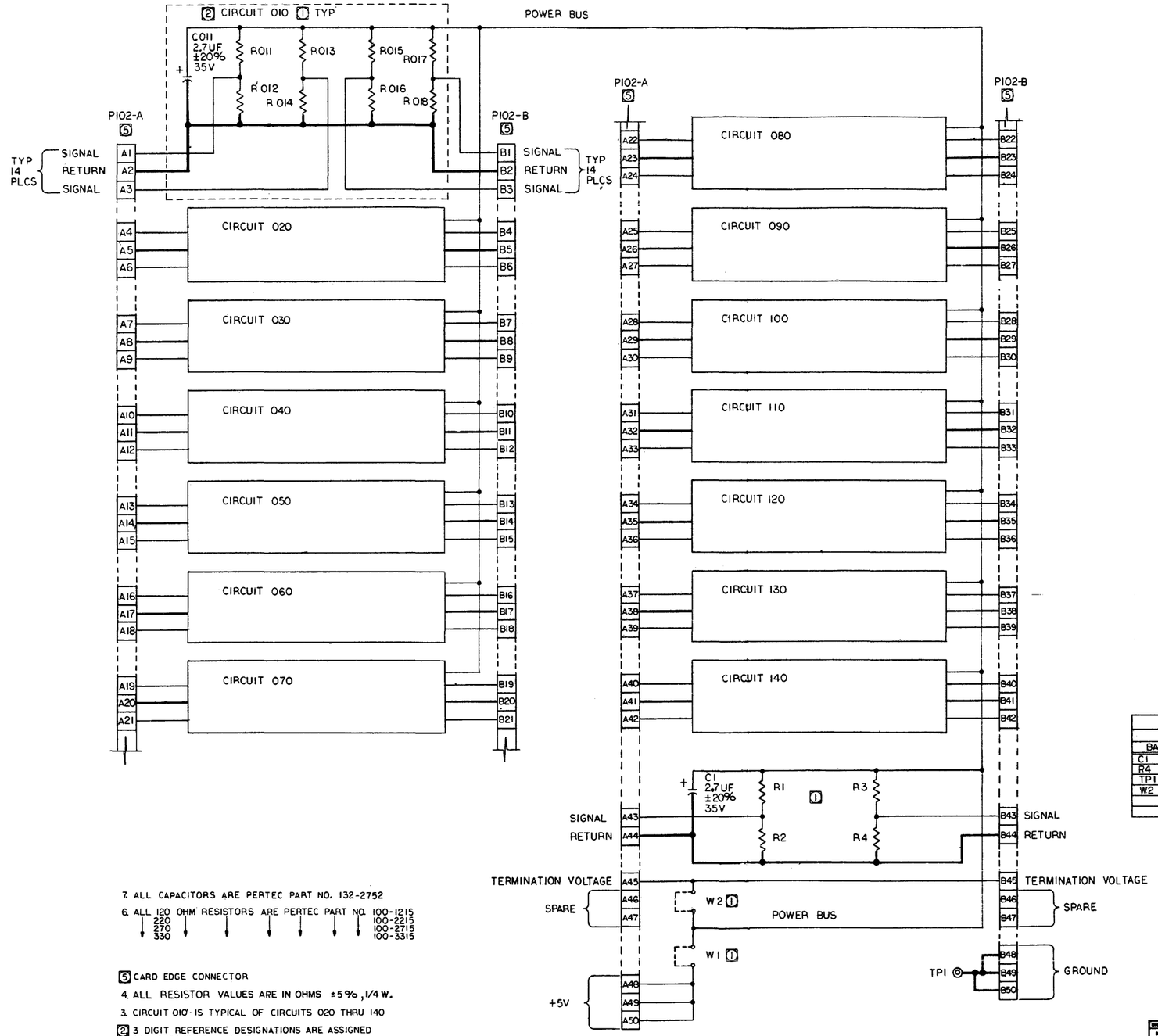
MATL: SEE LM

SIZE	CODE IDENT NO.	DWG NO.	REV
D		103571	D1

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF

103571 D1

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 4-6-W PRE-PRODUCTION RELEASE	4/1/76	RAS	WHS	WH
A1	ERN 4-YH PRODUCTION RELEASE	6/1/76	RAS	WHS	WH
A1	ECN 5906	6/1/76	T.K.	Kar	CH
B	ECN 7722	11/1/76	GLR	WH	WH



REFERENCE DESIGNATIONS			
LAST USED		DELETED	
BASIC	REPETITIVE [2]	BASIC	REPETITIVE
C1	C141		
R4	R148		
TP1			
W2			

7. ALL CAPACITORS ARE PERTEC PART NO. 132-2752
6. ALL 120 OHM RESISTORS ARE PERTEC PART NO. 100-1215, 220 → 100-2215, 270 → 100-2715, 330 → 100-3315

[5] CARD EDGE CONNECTOR
4. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 W.
3. CIRCUIT 010 IS TYPICAL OF CIRCUITS 020 THRU 140
[2] 3 DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO REPETITIVE CIRCUITS
[1] SEE VERSION TABLE, SHEET 2, FOR VALUE OR USAGE.
NOTES: UNLESS OTHERWISE SPECIFIED

PERIPHERAL EQUIPMENT CORPORATION

TITLE: SCHEMATIC, I/Ø TERMINATION BD

102801 | D3000 — NEXT ASSY | 1ST USED ON — APPLICATION

SIZE E | DWG NO. 102800 | REV B | SCALE NONE | SHEET 2 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPD
A	ERN 4-6-M PRE-PRODUCTION RELEASE	4/4/72	RAS	SMS	MM
	ERN 4-17M PRODUCTION RELEASE	4/17/72			
A1	ECN 5906	6/1/72	T.Z.		
B	ECN 7722	10/11/72	GJR	MM	

	-01	-02	-03	-04	-05	-06	-07
R011	OMIT	OMIT	220	120	120	220	120
R012	↑	↑	330	OMIT	OMIT	330	OMIT
R013			220	120	120	220	120
R014			330	OMIT	OMIT	330	OMIT
R015			220	120	120	220	120
R016			330	OMIT	OMIT	330	OMIT
R017			220	120	120	220	120
R018			330	OMIT	OMIT	330	OMIT
R021			220	120	120	220	120
R022			330	OMIT	OMIT	330	OMIT
R023			220	120	120	220	120
R024			330	OMIT	OMIT	330	OMIT
R025			220	120	120	220	120
R026			330	OMIT	OMIT	330	OMIT
R027			220	120	120	220	120
R028			330	OMIT	OMIT	330	OMIT
R031			220	120	120	220	120
R032			330	OMIT	OMIT	330	OMIT
R033			220	120	120	220	120
R034			330	OMIT	OMIT	330	OMIT
R035			220	120	120	220	120
R036			330	OMIT	OMIT	330	OMIT
R037			220	120	120	220	120
R038			330	OMIT	OMIT	330	OMIT
R041			220	120	120	220	120
R042			330	OMIT	OMIT	330	OMIT
R043			220	120	120	220	120
R044			330	OMIT	OMIT	330	OMIT
R045			220	120	120	220	120
R046			330	OMIT	OMIT	330	OMIT
R047			220	120	120	220	120
R048			330	OMIT	OMIT	330	OMIT
R051			220	120	120	220	120
R052			330	OMIT	OMIT	330	OMIT
R053			220	120	120	220	120
R054			330	OMIT	OMIT	330	OMIT
R055			220	120	120	220	120
R056			330	OMIT	OMIT	330	OMIT
R057			220	120	120	220	120
R058			330	OMIT	OMIT	330	OMIT
R061			220	120	120	220	120
R062			330	OMIT	OMIT	330	OMIT
R063			220	120	120	220	120
R064			330	OMIT	OMIT	330	OMIT
R065			220	120	120	220	120
R066			330	OMIT	OMIT	330	OMIT
R067			220	120	120	220	120
R068			330	OMIT	OMIT	330	OMIT
R071			220	120	120	220	120
R072			330	OMIT	OMIT	330	OMIT
R073			220	120	120	220	120
R074			330	OMIT	OMIT	330	OMIT
R075			220	120	120	220	120
R076			330	OMIT	OMIT	330	OMIT
R077	↓	↓	220	120	120	220	120
R078	OMIT	OMIT	330	OMIT	OMIT	330	OMIT

	-01	-02	-03	-04	-05	-06	-07
R081	OMIT		220	220	120	270	220	120
R082	↓		330	330	OMIT	OMIT	330	OMIT
R083			220	220	120	270	220	120
R084			330	330	OMIT	OMIT	330	OMIT
R085			220	220	120	270	220	120
R086			330	330	OMIT	OMIT	330	OMIT
R087			220	220	120	270	220	120
R088			330	330	OMIT	OMIT	330	OMIT
R091			220	220	120	270	220	120
R092			330	330	OMIT	OMIT	330	OMIT
R093			220	220	120	270	220	120
R094			330	330	OMIT	OMIT	330	OMIT
R095			220	220	120	270	220	120
R096			330	330	OMIT	OMIT	330	OMIT
R097			220	220	120	270	220	120
R098			330	330	OMIT	OMIT	330	OMIT
R101			220	220	120	270	220	120
R102			330	330	OMIT	OMIT	330	OMIT
R103			220	220	120	270	220	120
R104			330	330	OMIT	OMIT	330	OMIT
R105			220	220	120	270	220	120
R106			330	330	OMIT	OMIT	330	OMIT
R107			220	220	120	270	220	120
R108			330	330	OMIT	OMIT	330	OMIT
R111			220	220	120	270	220	120
R112			330	330	OMIT	OMIT	330	OMIT
R113			220	220	120	270	220	120
R114			330	330	OMIT	OMIT	330	OMIT
R115			220	220	120	270	220	120
R116			330	330	OMIT	OMIT	330	OMIT
R117			220	220	120	270	220	120
R118			330	330	OMIT	OMIT	330	OMIT
R121			220	220	120	270	220	120
R122			330	330	OMIT	OMIT	330	OMIT
R123			220	220	120	270	220	120
R124			330	330	OMIT	OMIT	330	OMIT
R125			220	220	120	270	220	120
R126			330	330	OMIT	OMIT	330	OMIT
R127			220	220	120	270	220	120
R128			330	330	OMIT	OMIT	330	OMIT
R131			220	220	120	270	220	120
R132			330	330	OMIT	OMIT	330	OMIT
R133			220	220	120	270	220	120
R134			330	330	OMIT	OMIT	330	OMIT
R135			220	220	120	270	220	120
R136			330	330	OMIT	OMIT	330	OMIT
R137			220	220	120	270	220	120
R138			330	330	OMIT	OMIT	330	OMIT
R141			220	220	120	270	220	120
R142			330	330	OMIT	OMIT	330	OMIT
R143			220	220	120	270	220	120
R144			330	330	OMIT	OMIT	330	OMIT
R145			220	220	120	270	220	OMIT
R146			330	330	OMIT	OMIT	330	OMIT
R147			220	220	120	270	220	120
R148			330	330	OMIT	OMIT	330	OMIT
R1			220	220	120	270	220	120
R2			330	330	OMIT	OMIT	330	OMIT
R3			220	220	120	270	220	120
R4			330	330	OMIT	OMIT	330	OMIT
W1	↓		USE	USE	OMIT	OMIT	OMIT	OMIT
W2	OMIT		OMIT	OMIT	USE	USE	USE	USE
C1, C011 THRU C141	USE		USE	USE	USE	USE	USE	USE

REFERENCE DESIGNATIONS			
LAST USED		DELETED	
BASIC	REPETITIVE	BASIC	REPETITIVE
C1	C141		
R4	R148		
TP1			
W2			

TAGE

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPD
	SEE SHT 1				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: .XX ± .05, .XXX ± .005, ANGULAR ±1/2°, ✓. BREAK ALL SHARP EDGES .010 MAX.

THE INFORMATION HEREIN IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UTILIZATION MAY BE MADE EXCEPT AS AUTHORIZED BY CONTRACT OR WRITTEN PERMISSION.

SIGNATURES	DATE
DR Les Nicol	10/6/72
CHK C.Blackman	10/6/72
DES	
ENGR FULTS	6-23-72
ENGR J.F. Fultz	6-23-72
MATL:	

PEC PERIPHERAL EQUIPMENT CORPORATION

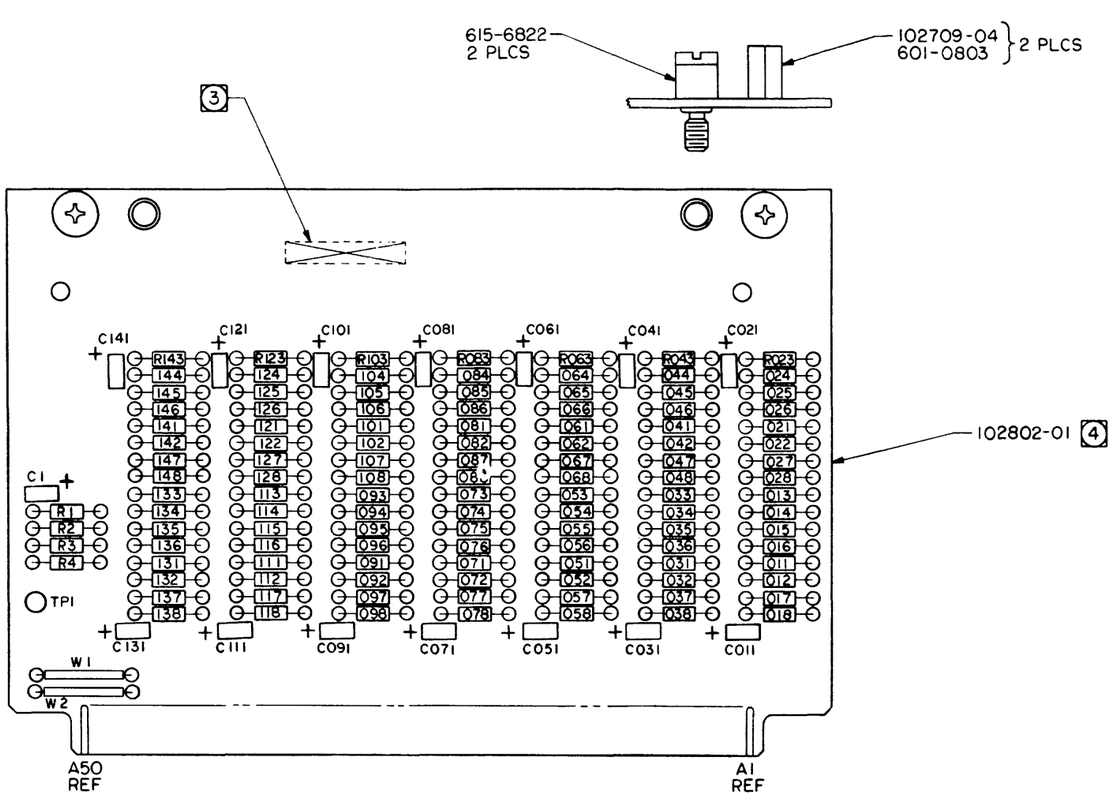
TITLE SCHEMATIC, I/Ø TERMINATION BD

SIZE E | DWG NO. 102800 | REV B | SCALE NONE | DO NOT SCALE DWG | SHEET 2 OF 2

102801 D3000 NEXT ASSY 1ST USED ON APPLICATION

FINISH: MATL:

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 46-W PRE-PRODUCTION RELEASE	5/8/72	RAS	5/11/72	
	ERN 4-YH PRODUCTION RELEASE	7/26/72	RAS	GAS	
B	ECN 7331	8/1/73	MLS		
C	ECN 7941	12/3/73	RV		
D	ECN 9712	7/8/77	SMP		



FOR ASSEMBLY VERSION INFORMATION SEE SCHEMATIC 102800.
FOR LIST OF MATERIALS SEE LM 102801 AND APPLICABLE DASH NO.
PART NO. 102801-03 REV C

(4) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 102802-01 REV E AND SUBSEQUENT.

(3) RUBBER STAMP ASSY PART NO. 102801 INCLUDING VERSION NO. AND VERSION ISSUE LETTER NEARSIDE ORIENTED AS SHOWN.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWING SCHEMATIC 102800.

NOTES: UNLESS OTHERWISE SPECIFIED:

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± —
.XXX ± —
ANGULAR —
X ± —
X ± —
BREAK ALL SHARP CORNERS APPROX .010

SIGNATURES	DATE
DR. R. Ly	5/10/72
CHK	6/1/72
DES	
ENGR FULTZ	6-22-72
PROJ. ENGR	6-22-72

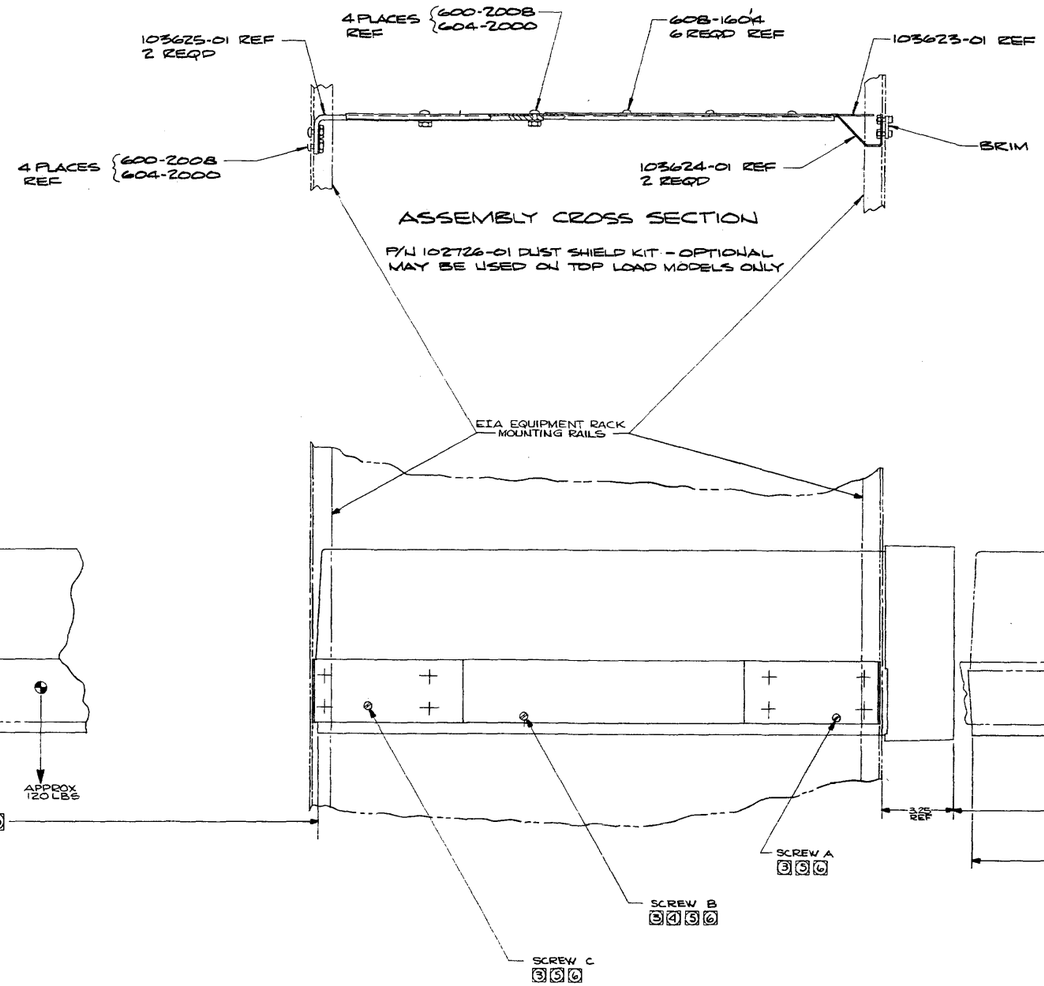
PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
I/O TERMINATION BOARD

NEXT ASSY	1ST USED ON
—	D3000
APPLICATION	

FINISH:
MATL:

SIZE	CODE IDENT NO.	DWG NO.	REV
D		102801	D
SCALE —	DO NOT SCALE DWG	SHEET 1 OF 1	



6 AFTER INSTALLATION OF DRIVE ENSURE THAT SCREWS A, B & C ARE TIGHTENED. (BOTH SIDES)

5 25.00 INCH REAR TRAVEL ON 102731-01 SLIDE ASSEMBLY.
19.00 INCH REAR TRAVEL AS INSTALLED
29.25 INCH REAR TRAVEL WITH SCREW C REMOVED } 103670-01

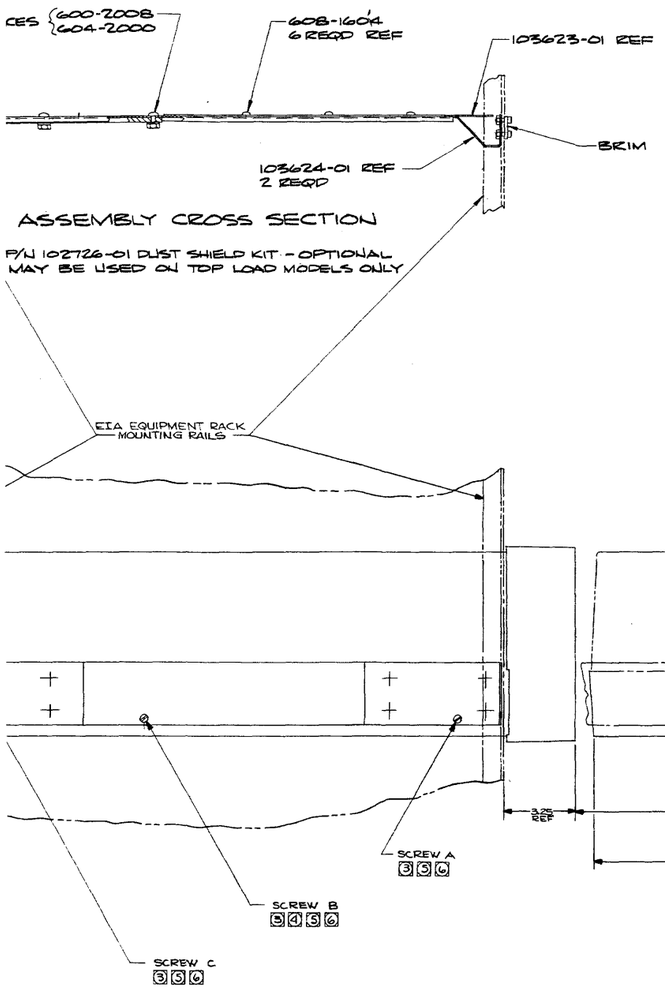
4 SLIDE DISCONNECT ACCOMPLISHED BY REMOVING SCREW B.

3 30.00 INCH FWD TRAVEL ON 102731-01 SLIDE ASSEMBLY.
19.00 INCH FWD TRAVEL AS INSTALLED
31.25 INCH FWD TRAVEL WITH SCREW A REMOVED } 103670-01

2 ALL MOUNTING HARDWARE SHOWN IS SUPPLIED WITH EACH UNIT.

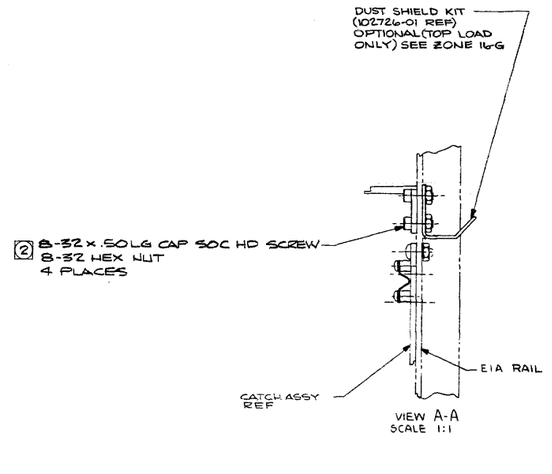
1 ADJUST SLIDES TO 16.100±.030 BEFORE INSTALLING UNIT.

NOTES: UNLESS OTHERWISE SPECIFIED.

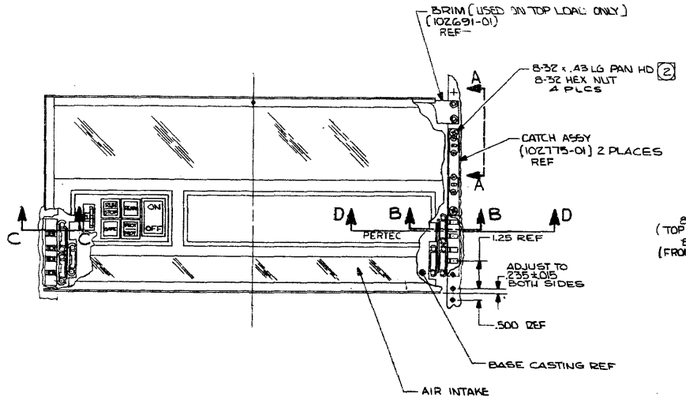


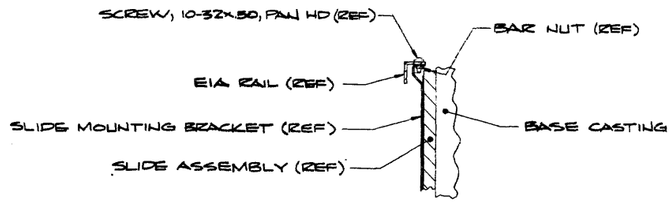
ASSEMBLY CROSS SECTION

P/N 102726-01 DUST SHIELD KIT - OPTIONAL MAY BE USED ON TOP LOAD MODELS ONLY

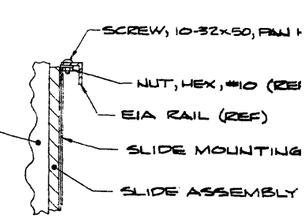


VIEW A-A
SCALE 1:1





SECTION C-C
CHASSIS TRACK SLIDE
(SLIDE P/N 102731-01)



SECTION B-B
ACCURIDE SLIDE
(SLIDE P/N 102731-01)

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ECN 4141 INC 1100 LVC SUBST	3/4/91	EC	[illegible]	[illegible]
B	ECN 4414 PRODUCTION RELEASE	4/24/91	EC	[illegible]	[illegible]
C	ECN 5927	10/23/92	MW	[illegible]	[illegible]
D	ECN 5992	12/3/92	MW	[illegible]	[illegible]
E	ECN 6398	5/17/93	MJ	[illegible]	[illegible]
F	ECN 7719	5/27/94	MJ	[illegible]	[illegible]
G	ECN 9701	11/3/97	TDM	[illegible]	[illegible]

DUST SHIELD KIT (102726-01 REF) OPTIONAL (TOP LOAD ONLY) SEE ZONE 16G

2 8-32 x .50 LG CAP SOC HD SCREW
8-32 HEX NUT
4 PLACES

CATCH ASSY REF

EIA RAIL

VIEW A-A
SCALE 1:1

19.50 MIN

19.00 +.02 -.03 REF

17.75 MIN 102731-01

17.48 MIN 103670-01

9.50 REF

EIA RAIL

3.25 REF

.090 REF

CABLE BOARDS (REF)

INTERFACE CABLE (REF) THREE OR SIX 34 CONDUCTOR FLAT CABLES

FUSES (REF)

℄ DISK

EIA RAIL

CABLE BOARDS

FUSES

.975 REF

NAMEPLATE

.34 REF

POWER CORD 8 FEET LONG

16.100 ±.010 1

1.25

.271 REF TYP 4 PLCS

SLIDE ASSY (102731-01) REF

SLIDE RESTRAINING BLOCK ONE PER SIDE (102716-01) REF (ATTACH TO REAR EIA RAIL USING 10-32 HDW) 2

AIR DISCHARGE AREA

CABLE BOARDS

EXHAUST BLOWER

FUSES

.80 REF

NAMEPLATE

.37 REF

POWER CORD 8 FEET LONG

16.100±.010 1

AIR DISCHARGE AREA

D3000 EXTENSION ONLY

BRIM (USED ON TOP LOAD ONLY) (102691-01) REF

8-32 x .43 LG PAN HD 2
8-32 HEX NUT
4 PLCS

CATCH ASSY (102715-01) 2 PLACES REF

A

A

B

B

C

D

D

PERTEC

1.25 REF

ADJUST TO 2.35±.05 BOTH SIDES

.500 REF

BASE CASTING REF

AIR INTAKE

DISK ℄

8.720±.030 REF

8.433 REF (TOP LOAD)
8.623 REF (FRONT LOAD)

26.00 REF

28.00 REF

EIA RAIL

EIA RAIL

50, PAN HD (REF)

BAR NUT (REF)

RAIL (REF)

ET (REF)

ABLY (REF)

BASE CASTING (REF)

SECTION C-C
CHASSIS TRACK SLIDE
(SLIDE P/N 102731-01)

SCREW, 10-32x50, PAN HD (REF)

NUT, HEX, #10 (REF)

EIA RAIL (REF)

SLIDE MOUNTING BRACKET (REF)

SLIDE ASSEMBLY (REF)

SECTION B-B
ACCURIDE SLIDE
(SLIDE P/N 102731-01)

SCREW, 10-32 x .38 PAN HEAD (REF)

EIA RAIL (REF)

BARNUT (REF) OR NUT, 10-32 W/ PRE ASSEMBLED LOCK WASHER (REF).

SLIDE MOUNTING BKT (REF)

BASE CASTING (REF)

SLIDE ASSY (REF)

SECTION D-D
103670-01 SLIDE
OR 103670-02 SLIDE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

SIGNATURES		DATE
DR	[illegible]	7/6/92
CHK	[illegible]	7/6/92
ENG	[illegible]	7/6/92
MFG. ENGR	[illegible]	7/6/92
MFG. ENGR	[illegible]	7-13-92

PERTEC PERIPHERAL EQUIPMENT

TITLE: INSTALLATION DWG

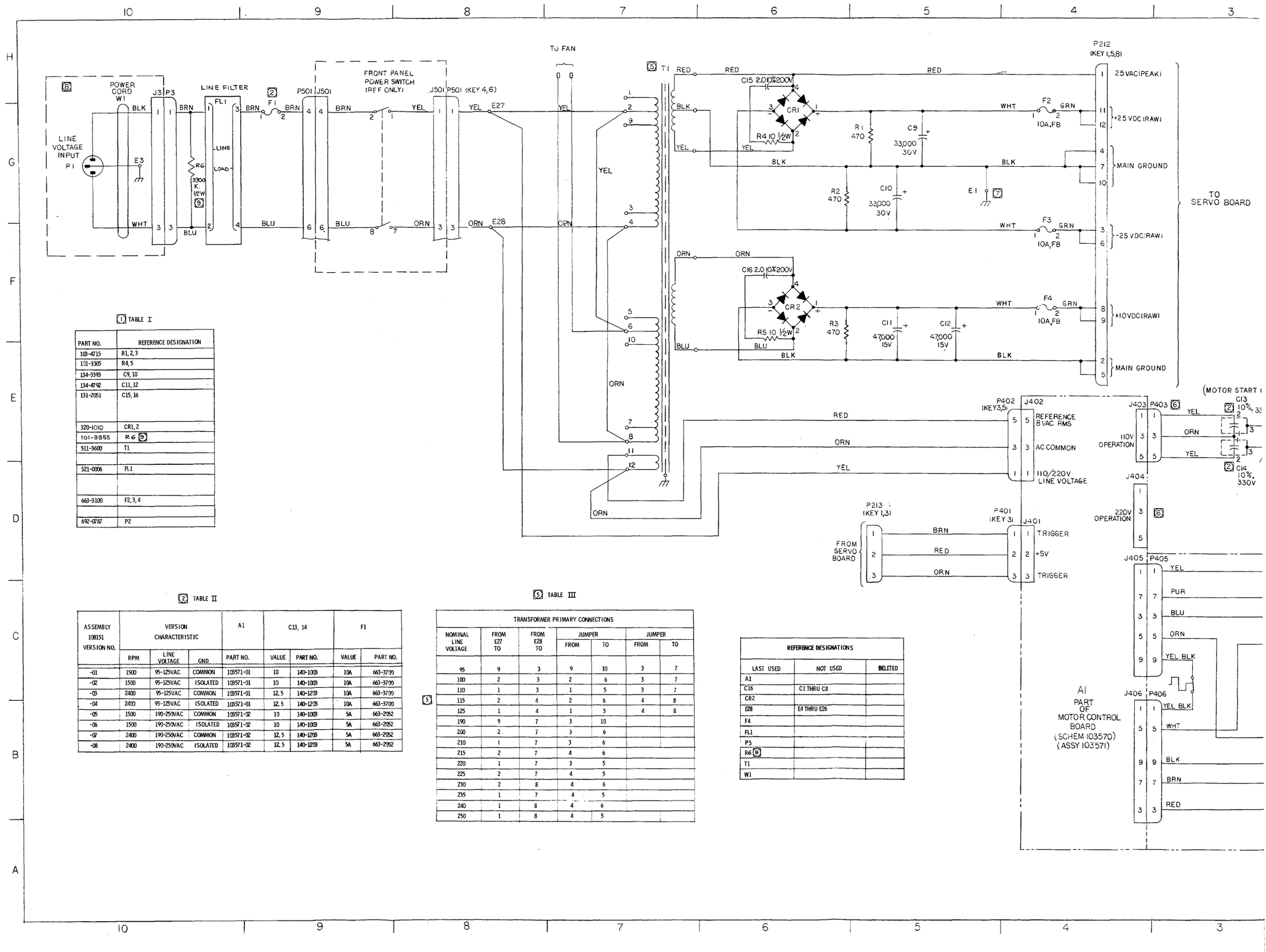
REF DWG D3000
NEXT ASSY — UP USED ON
APPLICATION

FINISH:

MATL:

SIZE J | CODE IDENT NO. | DWG NO. 103597 | REV G

SCALE 1/2 | DO NOT SCALE DWG | SHEET 7 OF 7



[1] TABLE I

PART NO.	REFERENCE DESIGNATION
108-4715	R1, 2, 3
101-1005	R4, 5
134-3393	C9, 10
134-4792	C11, 12
131-2051	C15, 16
320-1010	CR1, 2
101-3355	R6 [9]
511-3600	T1
521-0006	FL1
663-3100	F2, 3, 4
692-0787	P2

[2] TABLE II

ASSEMBLY 108151 VERSION NO.	VERSION CHARACTERISTIC			A1	C13, 14		F1	
	RPM	LINE VOLTAGE	GND	PART NO.	VALUE	PART NO.	VALUE	PART NO.
-01	1500	95-125VAC	COMMON	103571-01	10	140-1003	10A	663-3709
-02	1500	95-125VAC	ISOLATED	103571-01	10	140-1003	10A	663-3709
-03	2400	95-125VAC	COMMON	103571-01	12.5	140-1213	10A	663-3709
-04	2400	95-125VAC	ISOLATED	103571-01	12.5	140-1213	10A	663-3709
-05	1500	190-250VAC	COMMON	103571-02	10	140-1003	5A	663-2052
-06	1500	190-250VAC	ISOLATED	103571-02	10	140-1003	5A	663-2052
-07	2400	190-250VAC	COMMON	103571-02	12.5	140-1213	5A	663-2052
-08	2400	190-250VAC	ISOLATED	103571-02	12.5	140-1213	5A	663-2052

[5] TABLE III

NOMINAL LINE VOLTAGE	TRANSFORMER PRIMARY CONNECTIONS						
	FROM E27 TO	FROM E28 TO	JUMPER FROM	JUMPER TO	JUMPER FROM	JUMPER TO
95	9	3	9	10	3	7
100	2	3	2	6	3	7
110	1	3	1	5	3	7
115	2	4	2	6	4	8
125	1	4	1	5	4	8
190	9	7	3	10		
200	2	7	3	6		
210	1	7	3	6		
215	2	7	4	6		
220	1	7	3	5		
225	2	7	4	5		
230	2	8	4	6		
235	1	7	4	5		
240	1	8	4	6		
250	1	8	4	5		

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
A1		
C16	C1 THRU C8	
CR2		
E28	E4 THRU E26	
F4		
FL1		
P3		
R6 [9]		
T1		
W1		

REVISIONS				
REV	DESCRIPTION	DATE	DR.	CHK.	APPR.
A	ERN 8-FC PRE PROD. RELEASE	7/4/78	SW	DTC	
B	ECN 9570	7/27/78	SW	DTC	
C	ECN 9713	10/4/78	DR	DTC	
D	ECN 10575 ERN 10-CW PRODUCTION RELEASE	3/4/79 3/27/79	LB LL	KT KT	
E	ECN 11538	10/19/79	MP	KT	
F	ECN 14985	8-6-81	L.S.	RCC	

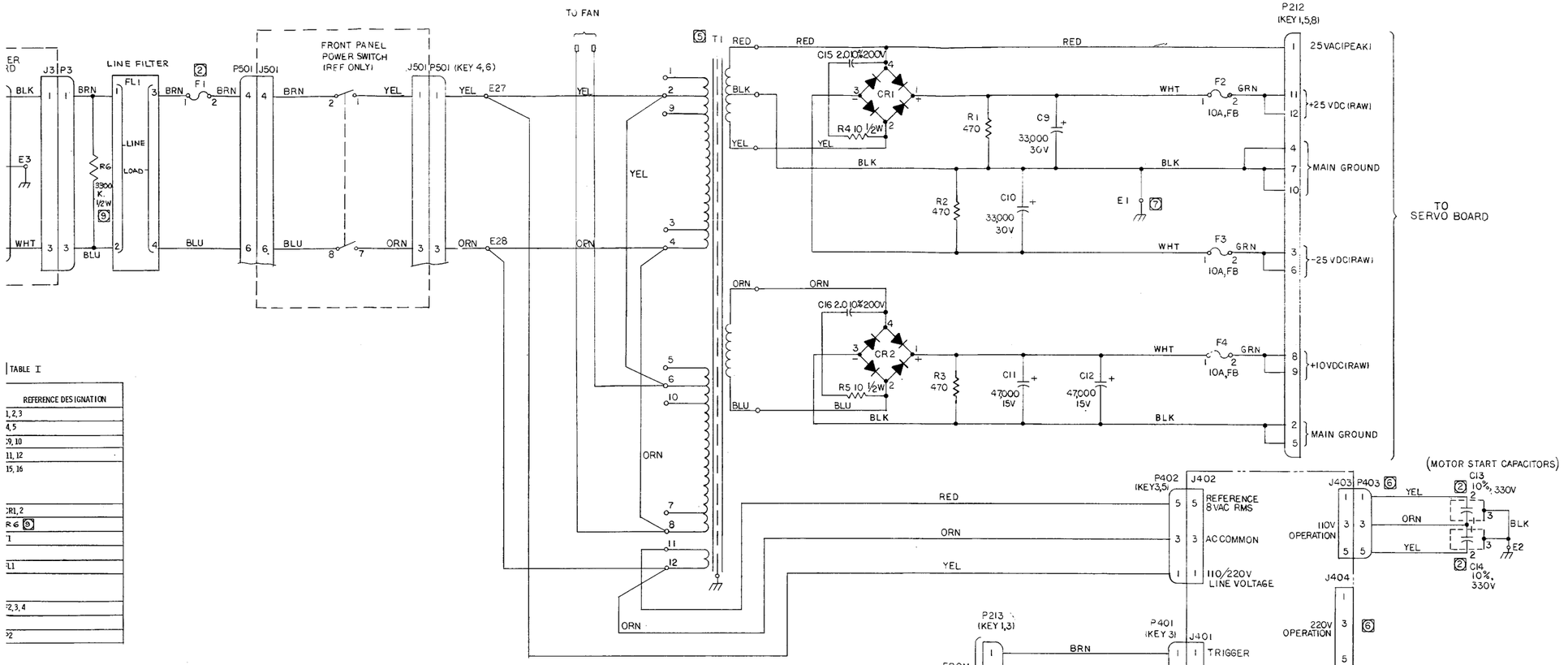


TABLE I

REFERENCE DESIGNATION
1, 2, 3
4, 5
9, 10
11, 12
15, 16
CR1, 2
R6 [9]
T1
FL1
E1, 2, 3, 4
P2

[2] TABLE II

VERSION CHARACTERISTIC			A1	C13, 14		F1	
RPM	LINE VOLTAGE	GND	PART NO.	VALUE	PART NO.	VALUE	PART NO.
1500	95-125VAC	COMMON	103571-01	10	140-1003	10A	663-3700
1500	95-125VAC	ISOLATED	103571-01	10	140-1003	10A	663-3700
2400	95-125VAC	COMMON	103571-01	12.5	140-1213	10A	663-3700
2400	95-125VAC	ISOLATED	103571-01	12.5	140-1213	10A	663-3700
1500	190-250VAC	COMMON	103571-02	10	140-1003	5A	663-2052
1500	190-250VAC	ISOLATED	103571-02	10	140-1003	5A	663-2052
2400	190-250VAC	COMMON	103571-02	12.5	140-1213	5A	663-2052
2400	190-250VAC	ISOLATED	103571-02	12.5	140-1213	5A	663-2052

[5] TABLE III

TRANSFORMER PRIMARY CONNECTIONS						
NOMINAL LINE VOLTAGE	FROM E27 TO	FROM E28 TO	JUMPER FROM	JUMPER TO	JUMPER FROM	JUMPER TO
95	9	3	9	10	3	7
100	2	3	2	6	3	7
110	1	3	1	5	3	7
115	2	4	2	6	4	8
125	1	4	1	5	4	8
190	9	7	3	10		
200	2	7	3	6		
210	1	7	3	6		
215	2	7	4	6		
220	1	7	3	5		
225	2	7	4	5		
230	2	8	4	6		
235	1	7	4	5		
240	1	8	4	6		
250	1	8	4	5		

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
A1		
C16	C1 THRU C8	
CR2		
E28	E4 THRU E26	
F4		
FL1		
P3		
R6 [9]		
T1		
W1		

[9] R6 TO BE INSTALLED ONLY WHEN FILTER (FL1) PART NO. 521-0006 IS USED.

[8] SEE TOP ASSEMBLY FOR PART NO. AND USAGE.

[7] FOR-02-04-06-08 VERSION (GROUND ISOLATION) DELETE THIS CONNECTION, E1 (MAIN GROUND TO CHASSIS GROUND).

[6] P403 IS SHOWN FOR NOMINAL LINE VOLTAGE OF 95 TO 125 VOLTS. CONNECT P403 TO J404 FOR NOMINAL LINE VOLTAGE OF 190 TO 250 VOLTS.

(*FOR 190 TO 250 VOLTS OPERATION P403 TO BE IDENTIFIED AS P404, REF.)

[5] WIRING OF TRANSFORMER PRIMARY SHOWN FOR NOMINAL LINE VOLTAGE OF 115 VOLTS; SEE TABLE III FOR CONNECTIONS UTILIZED FOR OTHER NOMINAL LINE VOLTAGES.

4. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 2W.

3. ALL CAPACITOR VALUES ARE IN MICROFARADS +75%, -10%.

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NO. 108151

WIRE LIST 108152

REFERENCE DRAWINGS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

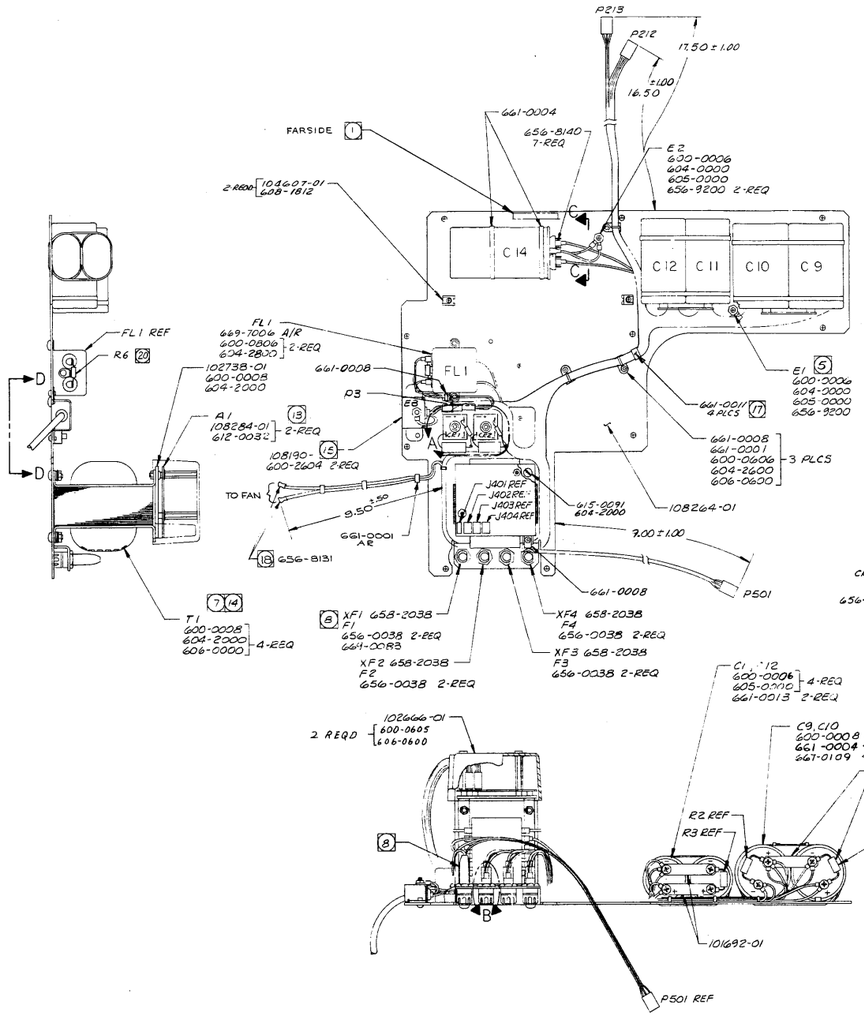
SIGNATURES	DATE
DR. T. Walker	9/6/78
CHK. [illegible]	9/7/78
ENGR. [illegible]	10/4/78
PROJ. ENGR. [illegible]	9/20/78

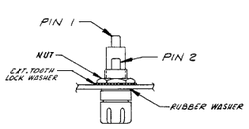
PERTEC PERIPHERAL EQUIPMENT DIVISION

TITLE SCHEMATIC POWER SUPPLY

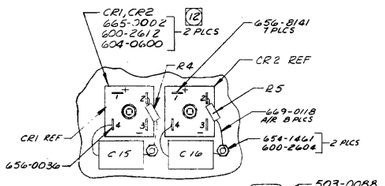
108151	D3600EXT	FINISH:	MATL:	SIZE	CODE IDENT NO.	DWG. NO.	REV
NEXT ASSY	IF USED ON			J		108150	F
APPLICATION				SCALE ——		DO NOT SCALE DWG.	SHEET OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8C PRE-PRODUCTION RELEASE	11/74	[illegible]	[illegible]	[illegible]
B	ECN 9713	2/75	[illegible]	[illegible]	[illegible]
C	ECN 10399	8-5-77	[illegible]	[illegible]	[illegible]
D	ECN 10575	12/77	[illegible]	[illegible]	[illegible]
	ERN 10-CW PRODUCTION RELEASE	12/77	[illegible]	[illegible]	[illegible]
E	ECN 10790	4/78	[illegible]	[illegible]	[illegible]
F	ECN 11538	7/78	[illegible]	[illegible]	[illegible]
G	ECN 11586	9-8-78	[illegible]	[illegible]	[illegible]
G1	ECN 12128	8-18-79	[illegible]	[illegible]	[illegible]
H	ECN 12508	10/29/79	[illegible]	[illegible]	[illegible]
J	ECN 13717	10-7	[illegible]	[illegible]	[illegible]
K	ECN 14985A	12-6-80	[illegible]	[illegible]	[illegible]

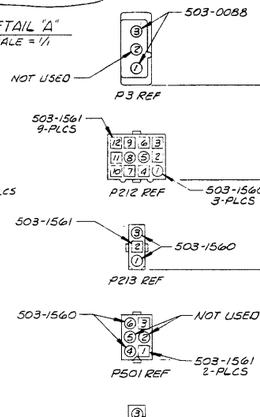




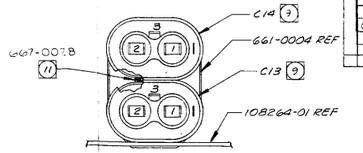
DETAIL B
SCALE = 1/1
USE VENDOR SUPPLIES HARDWARE
TYP 4-PLCS



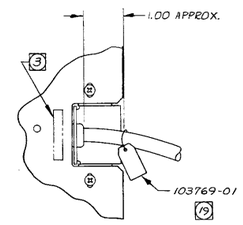
DETAIL 'A'
SCALE = 1/1



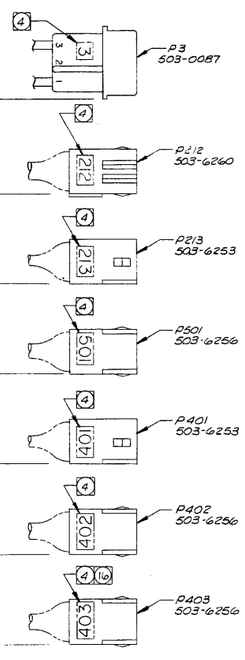
PIN INSERTION END VIEWS
SCALE = 2/1



VIEW C-C
SCALE = 1/1



VIEW D-D
SCALE = 1/1



11. USE 2 STRIPS OF 667-0028 BETWEEN C13 & C14.
10. TIE WRAP HARNESS ASSEMBLIES AT 2.5" MAX INTERVALS.
9. SHRINK SLEEVING 669-0038 OVER UNUSED TERMINALS (C13 & C14).
8. AFTER WIRING FUSEHOLDER, SHRINK 669-0083 IN PLACE OVER FUSEHOLDER AS SHOWN (XF1 ONLY).
7. AFTER WIRING TRANSFORMER TERMINALS COVER ALL TERMINALS BY SHRINKING 669-0038 IN PLACE OVER TERMINAL. USE TAPE 667-0549 IF NECESSARY TO COVER ALL EXPOSED PORTIONS OF THE TERMINAL.
6. TO ASSURE REQUIRED CLEARANCE FOR NEXT ASSY, INSPECT WITH BASE CASTING SIMULATOR TOOL.
5. FOR -02, -04, -06 & -08 VERSIONS (GND ISOLATION) DELETE CONNECTION FROM E1 TO C10 (+) (MAIN GND TO CHASSIS GND).
4. MARK REFERENCE DESIGNATION AS INDICATED ON RECEPTACLE, ORIENT AS SHOWN.
3. MARK NEXT TO SLOTTED HOLES FOR GND SCREW, DO NOT REMOVE.
2. REFERENCE DESIGNATIONS MAY NOT APPEAR ON ACTUAL COMPONENTS.
1. MARK ASSY WITH PN 108151, APPROPRIATE VERSION NUMBER, AND PERTEC ISSUE LETTER APPROX. WHERE SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

20. R6 TO BE INSTALLED ONLY WHEN FILTER PART NO. 521-0006 IS USED. WHEN INSTALLING R6, RESISTOR LEADS MUST BE KEPT .118 ± .050 AWAY FROM METAL BODY OF FILTER.
19. RECORD VOLTAGE AND FREQUENCY WITH INK. SEE SALES ORDER FOR APPROPRIATE INFORMATION.
18. SHRINK SLEEVING 669-7006 OVER ENTIRE TERMINAL
17. LOCATIONS TO BE DETERMINED BY MANUFACTURING.
16. FOR 190 TO 250 VOLTS OPERATION, IDENTIFY AS 434.
15. SEE TOP ASSY FOR APPROPRIATE POWER CORD ASSY
14. FOR TRANSFORMER TAP CHANGES ASSOCIATED WITH DIFFERENT LINE VOLTAGES SEE SCHEMATIC 108150.
13. USE 667-0109 SPARINGLY ON MILLE THREADS OF STAND-OFF 108284-01 AND 600-0008.
12. DURING INSTALLATION, CARE MUST BE TAKEN TO SEE THAT CONTAMINATION HAS BEEN REMOVED FROM ALL MOUNTING SURFACES AND THAT THESE SURFACES DO NOT TRAP CONTAMINATION. COAT MOUNTING SURFACE OF 320-1010 WITH A THIN FILM OF 665-0002 COMPOUND (90% MINIMUM COVERAGE) PRIOR TO MOUNTING. TORQUE SCREWS TO 10 ± 2 INCH POUNDS. WIPE EXCESS 665-0002 COMPOUND FROM COMPLETED ASSY.

SCHEMATIC 108150
WIRE LIST 108152
REF DWGS
PART NO. 108151-01 REV J

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± ANGULAR, XXX ± 1/2°, X ± √
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. [illegible]	12/6
CK. [illegible]	12/6
ENGR. [illegible]	12/6
PROJ. ENGR. [illegible]	12/6

PERTEC PERIPHERAL EQUIPMENT

TITLE: POWER SUPPLY ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.	REV
E		108151	K

SCALE 1/2 ENLARGED | DO NOT SCALE DWG | SHEET 1 OF 1

MATL: SEE L/M
FINISH:
FOR ASSY USED ON NEXT ASSY
APPLICATION
MANUFACTURED

108151 K

9600 Irondale Avenue
Chatsworth
California 91311
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